IEEE VLSI WORKSHOP

ON TEST STRUCTURES

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UNITED STATES DEPARTMENT OF COMMERCE
National Bureau of Standards
Gaithersburg, Maryland 20899

Welcome to the second IEEE VLSI Workshop on Test Structures. The increasing complexity of modern large-scale integrated circuits drives the development of well-understood and uniformly accepted measurement tools to evaluate and characterize both the circuits being manufactured and the processes used to produce these products. Integrated circuit test structures and the methods used to test them, coupled with computer-controlled automatic test systems and data analysis techniques, provide a means for meeting this challenge. The increasing use of test structures has resulted in many different designs, measurement methods, implementation approaches, and applications. The objective of this Workshop is to increase the effectiveness of test structure programs by bringing together the designers and users of test chips in an environment where recent developments, past problems, and future directions can be discussed. During the next two days, papers on topics such as material, process, device, and circuit characterization; yield and reliability assessment; test structure utilization; data analysis; and data management will be presented. In this time I hope you will take the opportunity to meet, discuss, and share information with others on topics of mutual interest. On behalf of the Program Committee, I would like to thank you for coming and hope that the Workshop will be professionally rewarding and that your participation will be stimulating. I would also like to thank the members of the Program Committee for their help in organizing this Workshop and the speakers for their contributions.

Loren W. Linholm
Technical Chairman
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As General Chairman, I wish to welcome you to the 1986 IEEE VLSI Workshop of Test Structures. It is gratifying to know that this Workshop has received the enthusiastic support from the IEEE Advisory Committee on Electron Devices.

The technical committee made a significant effort to invite the international engineering community and judging by the list of registrants from abroad, we have been successful. This is gratifying for the technical effort required to develop the plethora of test methods requires an international effort. An instrumentation display has been included this year with the intent of accelerating the availability of the equipment needed to make test structure measurements a routine and relatively simple matter.

As I look to the future, two issues need our attention if we are to bring our profession to a mature state. First, there is a serious deficiency in the availability of textural material and university-level courses in test structure design and analysis. For example, the terms Kelvin contact, van der Pauw sheet resistance, five-terminal capacitance measurements, and the statistical design of experiments are rarely mentioned in the university curriculum. Second, the commercial use of test structures is well established in the foundry business but the usage is very limited. More sophisticated use is required for the reliability assessment of VLSI circuits where part stressing is either impractical or impossible. It is time for us to formalize some 30 years of microelectronic measurement technology into a systematic and well thought-out text, course, and wafer acceptance procedure.

I wish to thank the members of the technical committee for their efforts in paper selection and session organization, the Technical Chairman, Loren Linholm, who managed the paper selection process, and the conference coordinator, Sandra Grawet, especially for organizing the exhibitors.

I hope the time you spend at the workshop is both enjoyable and informative and that you develop a number of relationships that spawn new test structure ideas. It is my feeling that as a community of test structure engineers, we have just begun to exploit this field.

Sincerely,

Martin G. Buehler

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General Chairman
IEEE VLSI Workshop
on Test Structures

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