PRESENTATIONS OF THE

IEEE VLSI WORKSHOP ON TEST STRUCTURES

February 20-21, 1984

San Diego, California

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Co-Chairman: D. E. Nelson, DEC

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PREFACE

The objective of the IEEE VLSI Workshop on Test Structures was to bring together the designers and users of test chips to discuss recent developments and future directions. The workshop was held on February 20 and 21, 1984, at the Vacation Village Hotel, San Diego, California. General topics covered were Material and Process Characterization, Test Structure Utilization, Yield and Reliability Assessment, and Device and Circuit Characterization.

At the meeting, several attendees requested copies of the speakers' slides or vugraphs. Following are the visual materials supplied by speakers responding to this request, the Schedule of Events, and listings of the Program Chairmen and of the attendees.

Loren W. Linholm
Co-Technical Chairman
1984 IEEE VLSI Workshop on Test Structures

PROGRAM CHAIRMEN

Co-General Chairmen:

M. M. Beguwala, Rockwell
K. F. Galloway, NBS

Co-Technical Chairmen:

M. G. Buehler, JPL
L. W. Linholm, NBS

Local Arrangements:

D. N. Pattanayak, Rockwell

Program Committee:

J. M. Aitken, IBM
C. N. Berglund, Intel
D. D. Buss, TI
E. B. Hakim, ERADCOM
A. C. Ipri, RCA
C. S. Meyer, Motorola
D. E. Nelson, DEC
M. C. Peckerar, NRL
J. F. Skalski, AFWAL
R. E. Tremain, Xerox
V. C. Tyree, USC/ISI

Schedule of Events

IEEE VLSI WORKSHOP ON TEST STRUCTURES

Vacation Village Hotel
San Diego, CA

Sunday, February 19, 1984

7:00 - 9:00 p.m.	Registration
Conference Suite	Reception

Monday, February 20

7:45 - 8:30 a.m.	Registration Continental Breakfast
8:30 - 9:00	Welcome & Introduction

SESSION I Material and Process Characterization

Chairman: J. M. Aitken, IBM
Co-Chairman: D. E. Nelson, DEC

9:00 - 9:25 a.m.	The Application of Microelectronic Test Structures for Linewidth Measurement in the Near and Submicron Linewidth Region L. W. Linholm, D. Yen, NBS, and M. W. Cresswell, Westinghouse
9:25 - 9:50	Integrated-Circuit Test Structure Which Uses a Vernier to Electrically Measure Mask Misalignment B. Henderson, Burroughs
9:50 - 10:15	Lifetime Interpretation from Silicon Test Structures D. K. Schroder, Arizona State University
10:15 - 10:35	COFFEE BREAK
10:35 - 11:00	Electrical Characterization of Epitaxial Silicon K. P. Roenker and T. J. Morthorst, University of Cincinnati, and C. Baylis, Cincinnati Milacron
11:00 - 11:25	Test Structures for GaAs Integrated Circuits R. Zucca, D. Hou, S. J. Lee, and R. Vahrenkamp, Rockwell

11:25 - 11:50	Layer to Layer Interconnections in VLSI Circuits, Models and Measurement Considerations G. K. Reeves, Telecom Australia Research Labs. and H. B. Harrison and G. Sai-Halasz, Royal Melbourne Institute of Technology
11:50 - 12:15	Isolation Test Structures for CMOS J. Y. Chen, Hughes Research Laboratories
12:15 - 1:30	LUNCH

SESSION II Test Structure Utilization

Chairman: R. E. Tremain, Xerox
Co-Chairman: M. C. Peckerar, NRL

1:30 - 1:55 p.m.	Test Device for CMOS/SOS Parameter Testing J. H. Nelson and H. L. Chew, Rockwell
1:55 - 2:20	An Integrated Approach to Technology Characterization R. E. Tremain, P. J. Martin, T. J. Oki, M. Y. T. Young, and D. L. Scharfetter, Xerox Palo Alto Research Center
2:20 - 2:45	Test Chip Strategy for a High Volume VLSI Design Laboratory M. E. Potter, Bell Labs
7:00 p.m.	BANQUET

Tuesday, February 21

SESSION III Yield and Reliability Assessment

Chairman: A. C. Ipri, RCA
Co-Chairman: E. B. Hakim, ERADCOM

8:30 - 8:55 a.m.	Pinhole Array Capacitor for Oxide Integrity Analysis M. G. Buehler, B. R. Blaes, C. A. Pina, and T. W. Griswold, JPL
8:55 - 9:20	A VLSI Electrical Defect Monitor C. Alcorn and W. Neiderer, IBM
9:20 - 9:45	Defect Characterization - A Functional Test Site Approach L. Bentson, IBM
9:45 - 10:10	Dynamic Self-Checking Microelectronic Test Structure P. F. Harris, ERADCOM

10:10 - 10:30	COFFEE BREAK
10:30 - 10:55	Test Structures for Examining Electromigration Failure H. A. Schafft, NBS, and A. N. Saxena and C.-Y. Kao, AMI
10:55 - 11:20	Electromigration-Induced Short Circuit and Open Circuit Failure Times in Multi-Layer Technologies J. R. Lloyd and J. A. Knight, IBM
11:20 - 11:45	A 2 Layer Metal Test Pattern for Fault Detection and Layout Rule Verification J. Rugg, Motorola
11:45 - 1:00	LUNCH

SESSION IV Device and Circuit Characterization

Chairman: V. C. Tyree, USC/ISI
Co-Chairman: J. F. Skalski, AFWAL

1:00 - 1:25 p.m.	Latch-Up Test Structures and Their Characterization W. J. Craig, IBM
1:25 - 1:50	An Integrated Optimization Approach for Compact MOS Device Modeling K. Doganis, Xerox Palo Alto Research Center and Stanford University, and R. E. Tremain and D. L. Scharfetter, Xerox Palo Alto Research Center
1:50 - 2:15	Modelling and Parameter Characterisation of Small-Dimension MOSFETS for SPICE G. T. Wright and H. Gaffur, University of Birmingham, U.K.
2:15 - 2:40	Small Geometry MOS Intrinsic and Extrinsic Capacitance Measurement Test Structures for VLSI J. Oristian, H. Iwai, T. Walker, and R. Dutton, Stanford University
2:40 - 3:05	An Automated MOS Statistical Analysis Modeling System (AMSAM) P. Yang and P. K. Chatterjee, Texas Instruments
3:05 - 3:30	A New CCD Test Structure for Measuring Silicon Defects - CCD Transient Spectroscopy (CCD TS) M. M. Mojaradi and K. L. Wang, University of California at Los Angeles
3:30 - 4:00	Discussion and Closing Remarks

A Microelectronic Test Chip Perspective

Martin G. Buehler
Jet Propulsion Laboratory

A MICROELECTRONIC TEST CHIP PERSPECTIVE

JPL

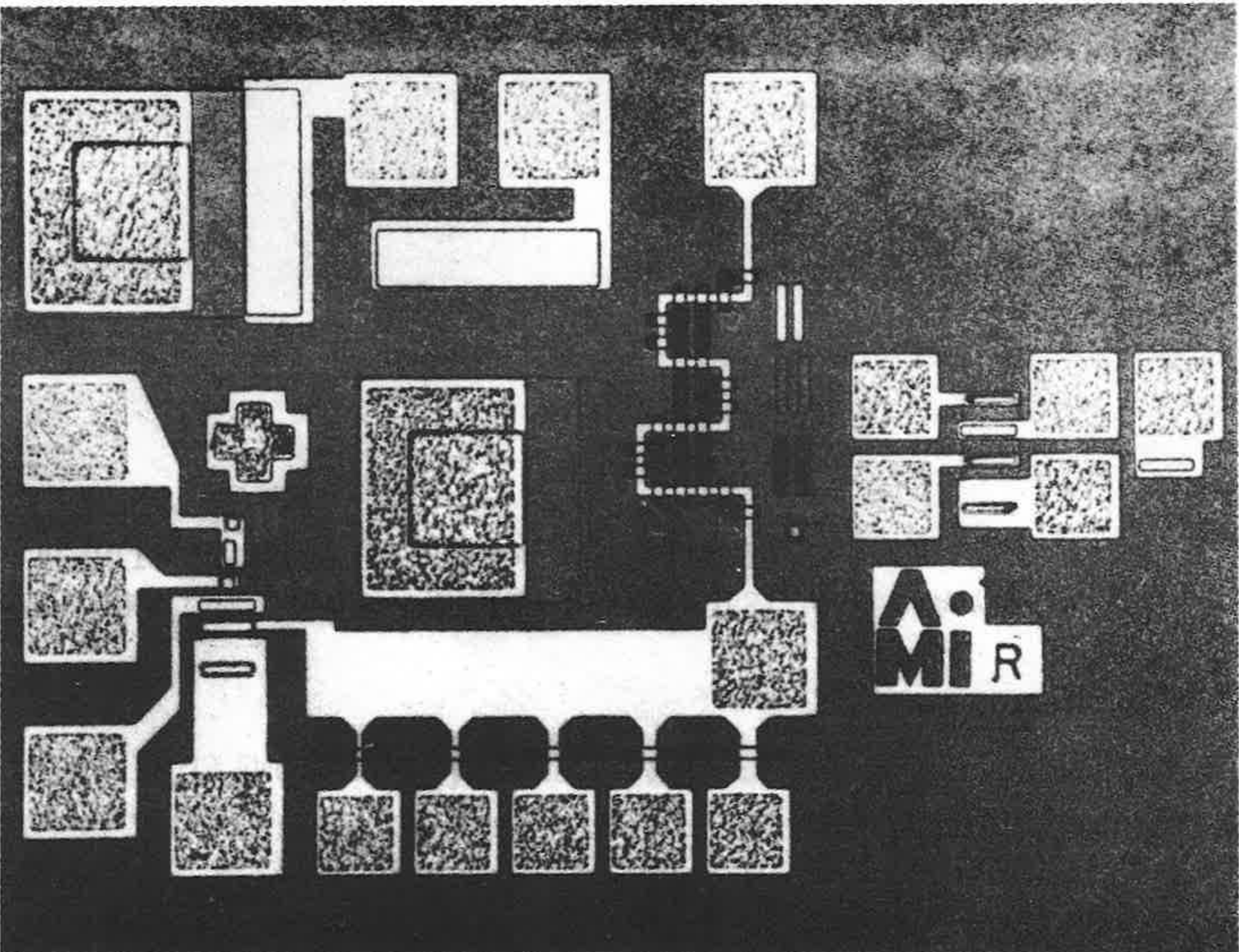
Martin Buehler

Jet Propulsion Laboratory

MGB-1
2-21-84

JPL

PROBE PAD DESIGN AND LAYOUT



REFERENCE PENNEY AND LAU (1972)

MGB-2
2-21-84

JPL

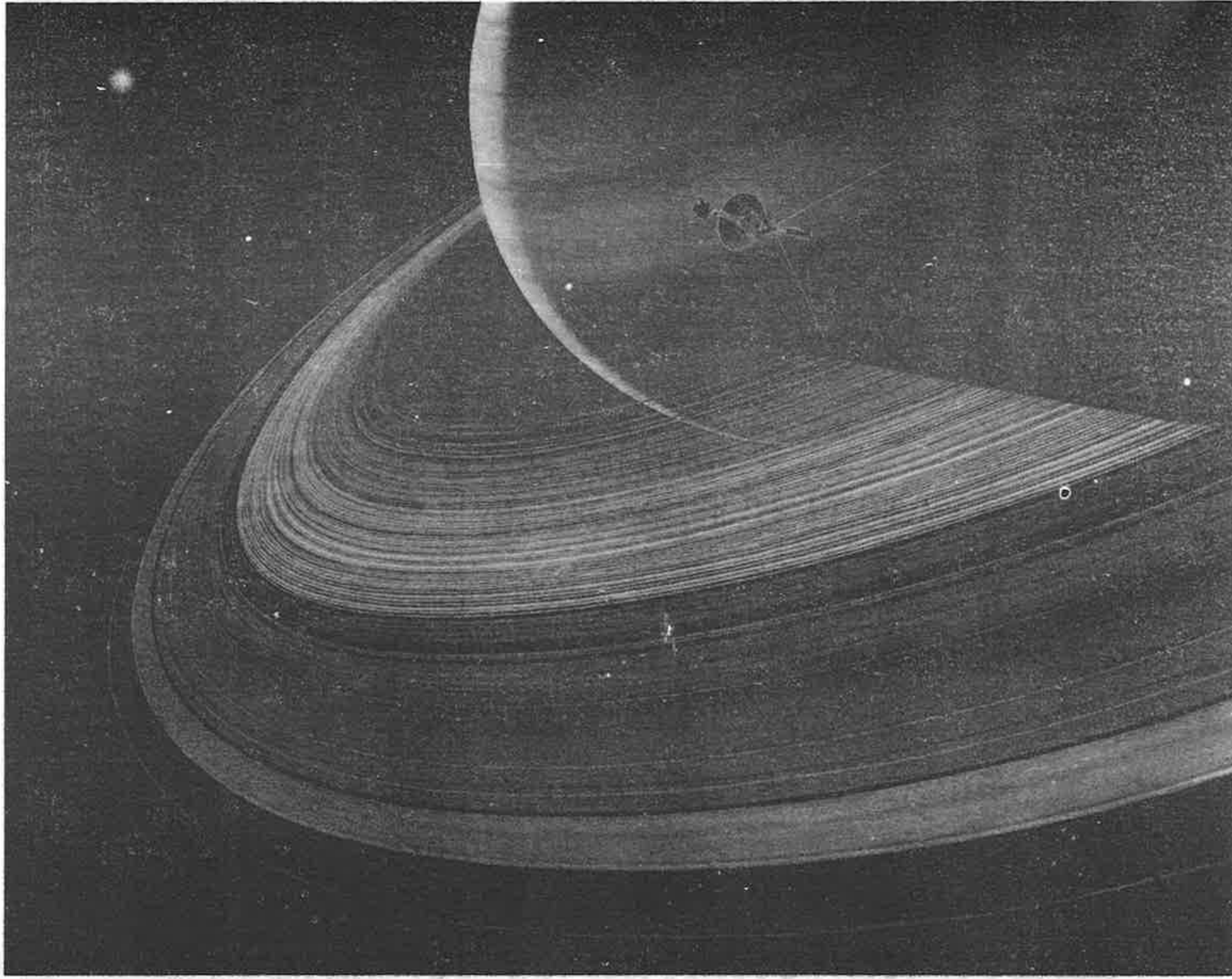
THE CHALLENGE TO THE TEST CHIP ENGINEER

- ALL THE INFORMATION NECESSARY FOR A THOROUGH CHARACTERIZATION OF A WAFER IS ENCODED ON PROPERLY DESIGNED AND PLACED TEST CHIP

- THE CHALLENGE IS TO PROPERLY DESIGN, TEST, AND ANALYZE TEST RESULTS SO AS TO UNLOCK THE INFORMATION

MGB-3
2-21-84

JPL



MGB-4
2-21-84

JPL

TEST CHIPS AS AN INFORMATION GATHER

- TEST CHIPS SAMPLE THE LOCAL ENVIRONMENT ON A WAFER
- THE EXTENT OF SAMPLING DEPENDS ON THE NATURE OF THE PARAMETER
- SAMPLING PLANS ARE RESTRICTED TO THE WAFER LEVEL AND NOT THE LOT LEVEL

MGB-5
2-21-84

JPL

TEST CHIP AS A DIAGNOSTICIAN

- THE ABILITY OF ONE TO USE TEST CHIPS TO DIAGNOSE A PROBLEM, IS LIMITED BY STATISTICAL INFERENCE IN MOST CASES

- A TEST CHIP CAN NOT BE USED TO GUARANTEE THAT AN ADJACENT CIRCUIT WILL BE FULLY FUNCTIONAL AND RELIABLE

MGB-6
2-21-84

JPL

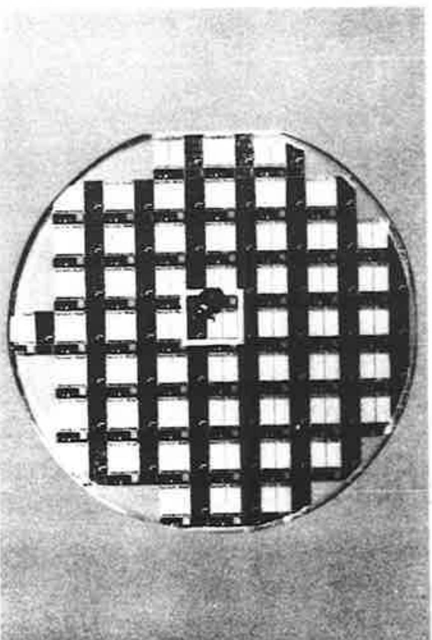
OBJECTIONS TO THE USE OF TEST CHIPS

- TEST CHIPS REPRESENT A CIRCUIT YIELD LOSS
- TEST CHIPS DIVERT ATTENTION FROM MAKING CIRCUITS
- TEST CHIP ANALYSIS REQUIRES TOO MUCH ENGINEERING TIME
- TEST CHIPS REVEAL TOO MUCH PROPRIETARY INFORMATION
- TEST CHIP MEASUREMENTS REQUIRE SPECIAL TEST EQUIPMENT

MGB-7
2-21-84

JPL

TEST CHIP USEAGE IN DEVELOPING A 64K STATIC RAM



THREE-INCH DIAMETER SILICON WAFER

AFTER: TEXAS INSTRUMENTS (1983)

MGB-8
2-21-84

JPL

POTENTIAL BENEFITS OF USING TEST CHIPS

- TEST CHIPS HOLD THE PROMISE OF REDUCING THE COST PER BIT IN QUALIFYING RELIABLE, CUSTOM LSI/VLSI CIRCUITS

- WHAT IS REQUIRED TO FULFILL THIS PROMISE IS AN INDUSTRY-WIDE EFFORT INTO TEST STRUCTURE RESEARCH AND QUALITY ASSURANCE PROCEDURES

MGB-9
2-21-84

Introduction

L. W. Linholm
National Bureau of Standards
Semiconductor Devices and Circuits Division
Washington, DC

IEEE VLSI WORKSHOP
ON TEST STRUCTURES

Session I - Material and process characterization

Session II - Test structure utilization

Session III - Yield and reliability assessment

Session IV - Device and circuit characterization

AN INTEGRATED CIRCUIT TEST STRUCTURE IS A MICROELECTRONIC DEVICE WHICH IS

- Used to measure selected device or process parameters by means of electrical tests
- Fabricated by same process and design rules used for integrated circuits

WELL CHARACTERIZED TEST STRUCTURES, TEST METHODS, AND ANALYSIS TECHNIQUES CAN BE USED FOR

- Process characterization
- Semiconductor equipment evaluation
- Process and device model input parameter determination
- Product acceptance

CURRENT/FUTURE MEASUREMENT PROBLEMS

- Scaling
- Product performance prediction
- Yield prediction
- Data management

BARRIERS TO
TEST STRUCTURE EFFECTIVENESS

- Common measurements methods
- Coherent test plan
- Proper utilization and application

SESSION I MATERIAL AND PROCESS CHARACTERIZATION

The Application of Microelectronic Test Structures for Linewidth Measurement in the Near and Submicron Linewidth Region

L. W. Linholm and D. Yen
National Bureau of Standards
Semiconductor Devices and Circuits Division
Washington, DC

M. W. Cresswell
Westinghouse Electric Corporation
Solid State Sciences Division
Pittsburgh, PA

THE APPLICATION OF MICROELECTRONIC TEST STRUCTURES FOR LINEWIDTH MEASUREMENT IN THE NEAR AND SUBMICRON LINEWIDTH REGION

L.W Linholm and D. Yen
National Bureau of Standards
Semiconductor Devices and Circuits Division
Washington, D.C.

M.W. Cresswell
Westinghouse Electric Corporation
Solid State Sciences Division
Pittsburgh, Pa.

OBJECTIVE

- To evaluate measurement accuracy of the cross bridge test structure
- To compare electrical measurement method to other techniques
- To identify linewidth measurement uncertainties

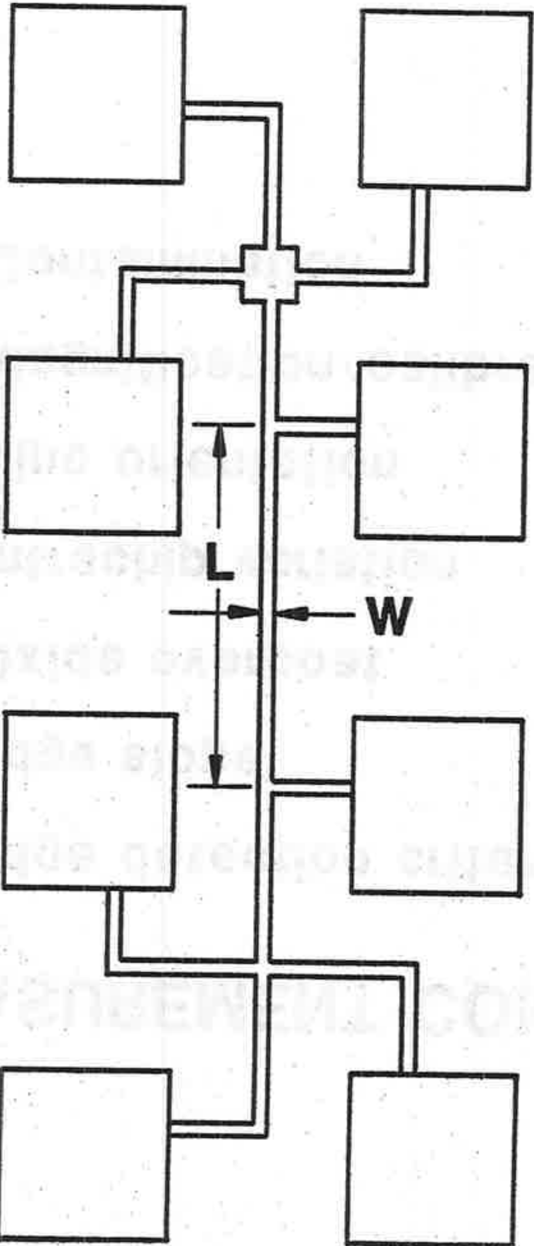
OUTLINE

- Objective
- Linewidth measurement considerations
- Electrical test structure
- Design and fabrication
- Results
- Discussion
- Summary

LINEWIDTH MEASUREMENT CONSIDERATIONS

- Edge detection criteria
- Edge slope
- Oxide overcoat
- Intrachip variation
- Line orientation
- Magnification/calibration
- Contamination

DOUBLE CROSS-BRIDGE RESISTOR

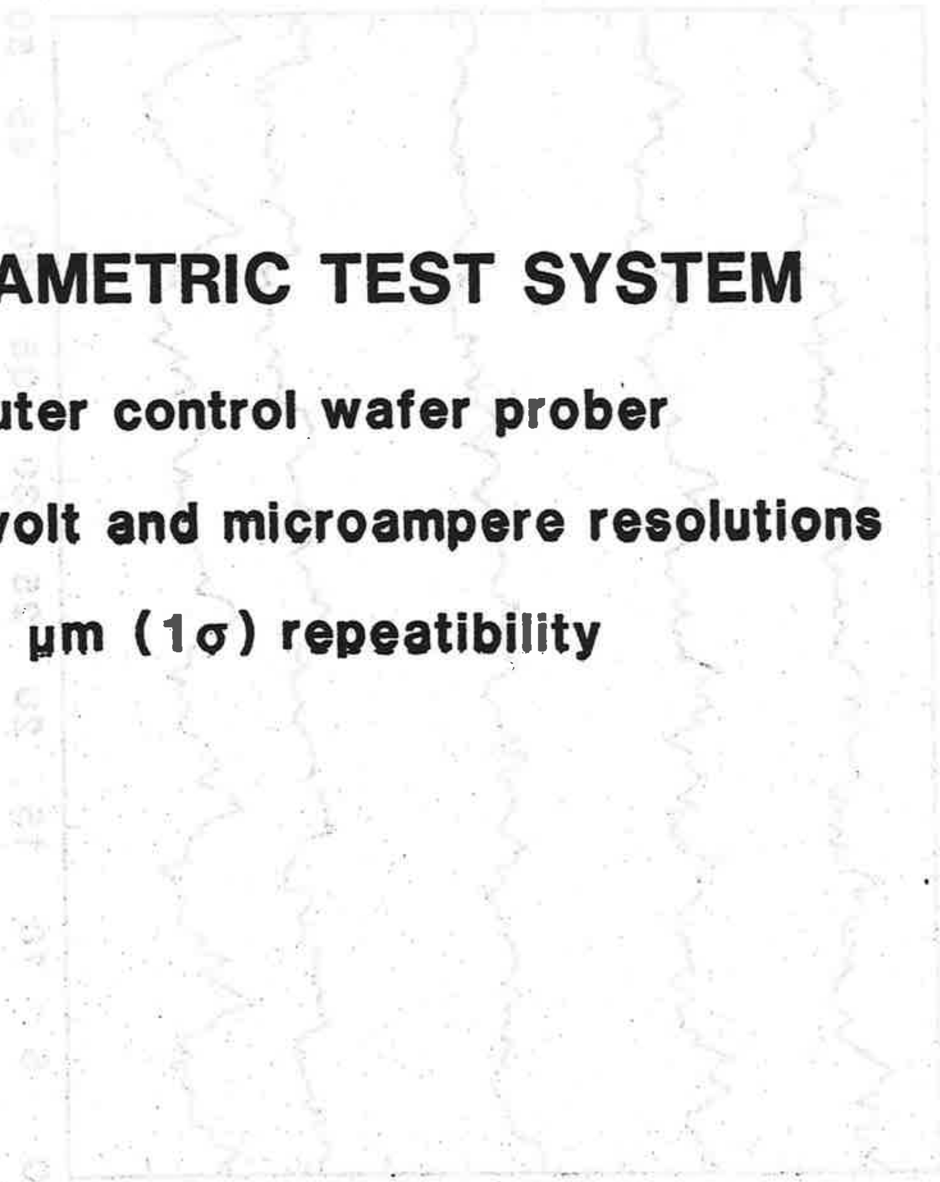


TEST CHIP LAYOUT

- Array size 13 x 26
- Design linewidth 0.6 μm - 1.6 μm
- Chip dimensions 8.64 mm x 8.96 mm

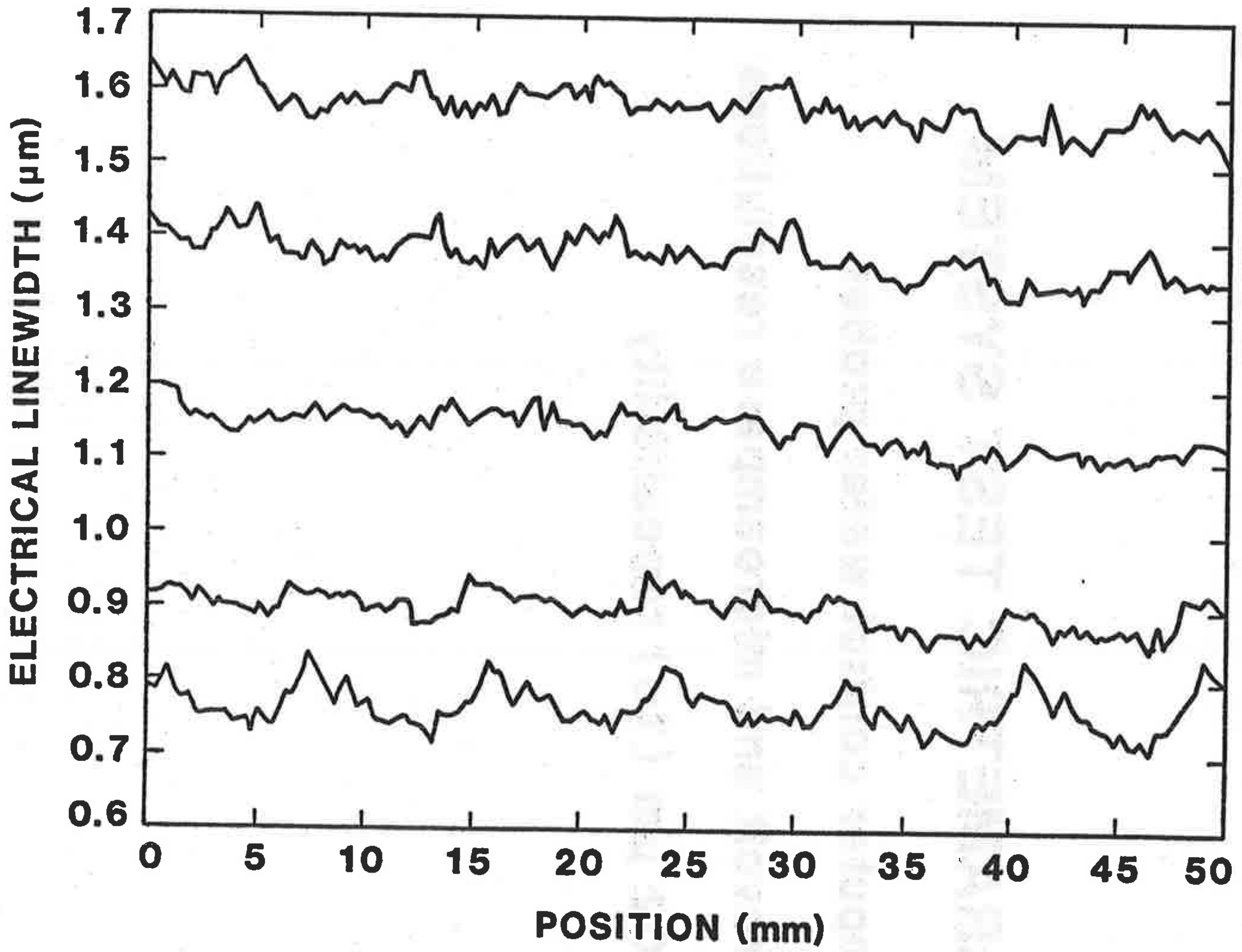
WAFER FABRICATION

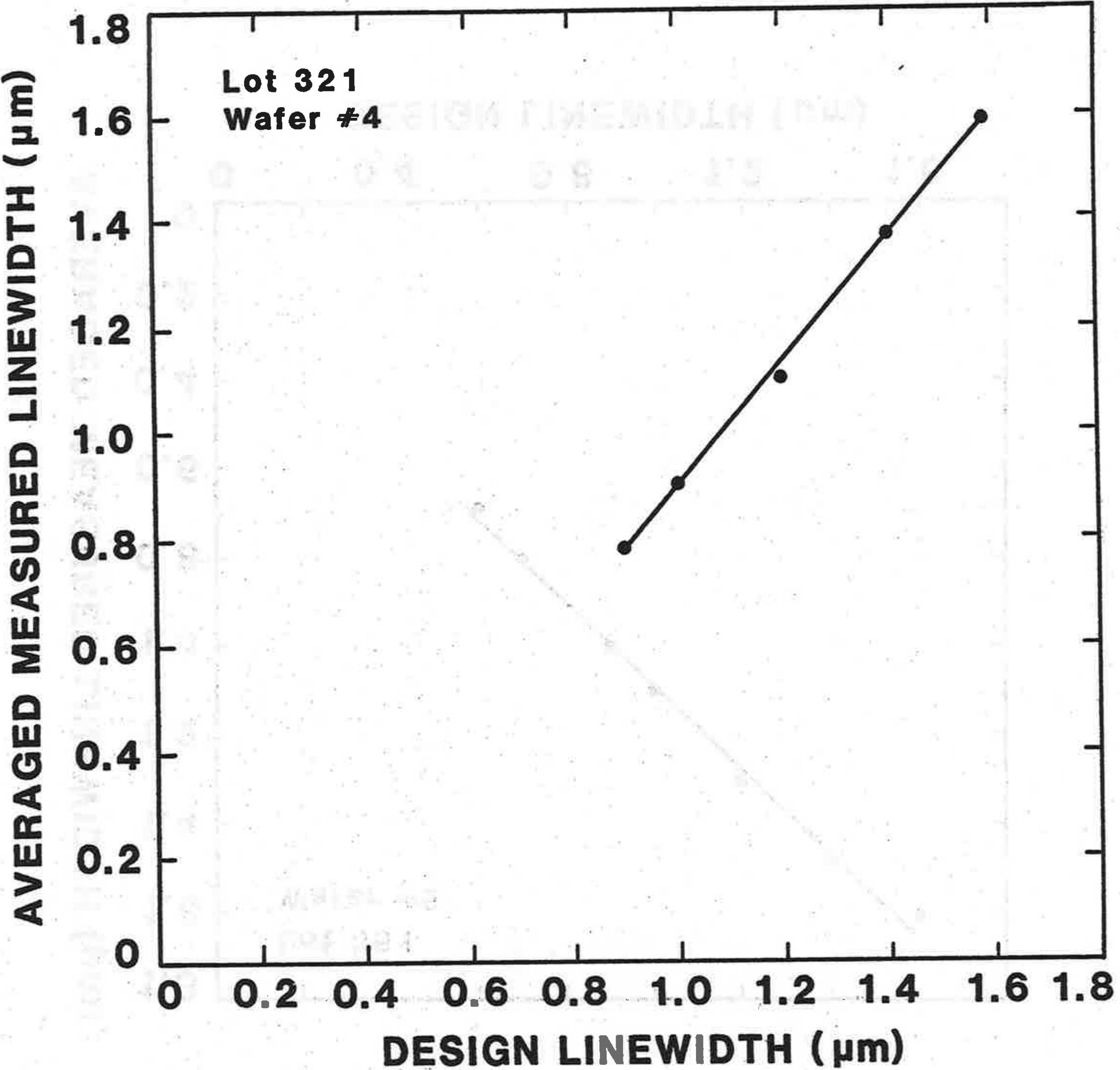
- Thermal oxide
- LPCVD polysilicon
- Phosphorus diffusion
- Direct step exposure
- RIE

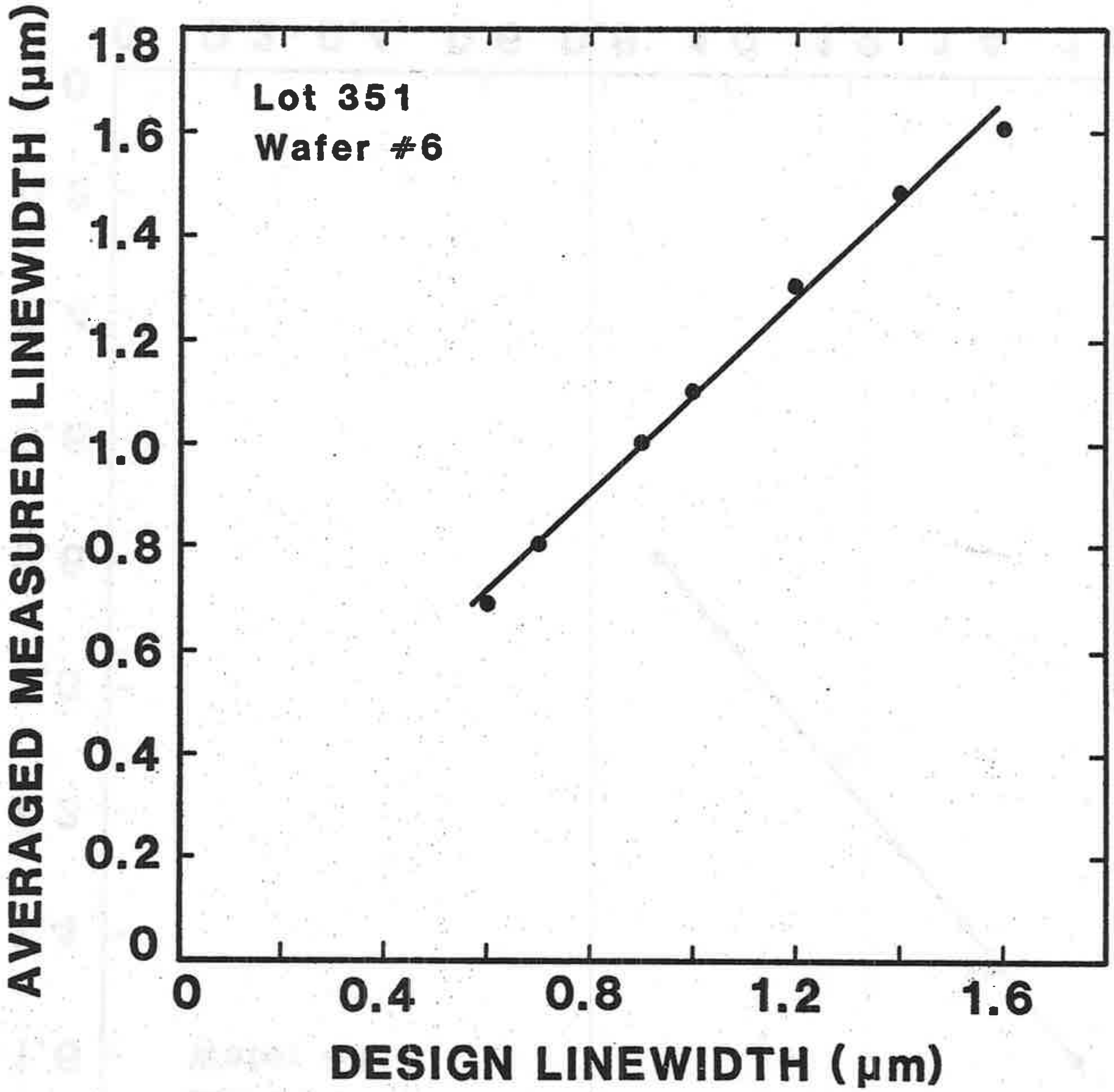


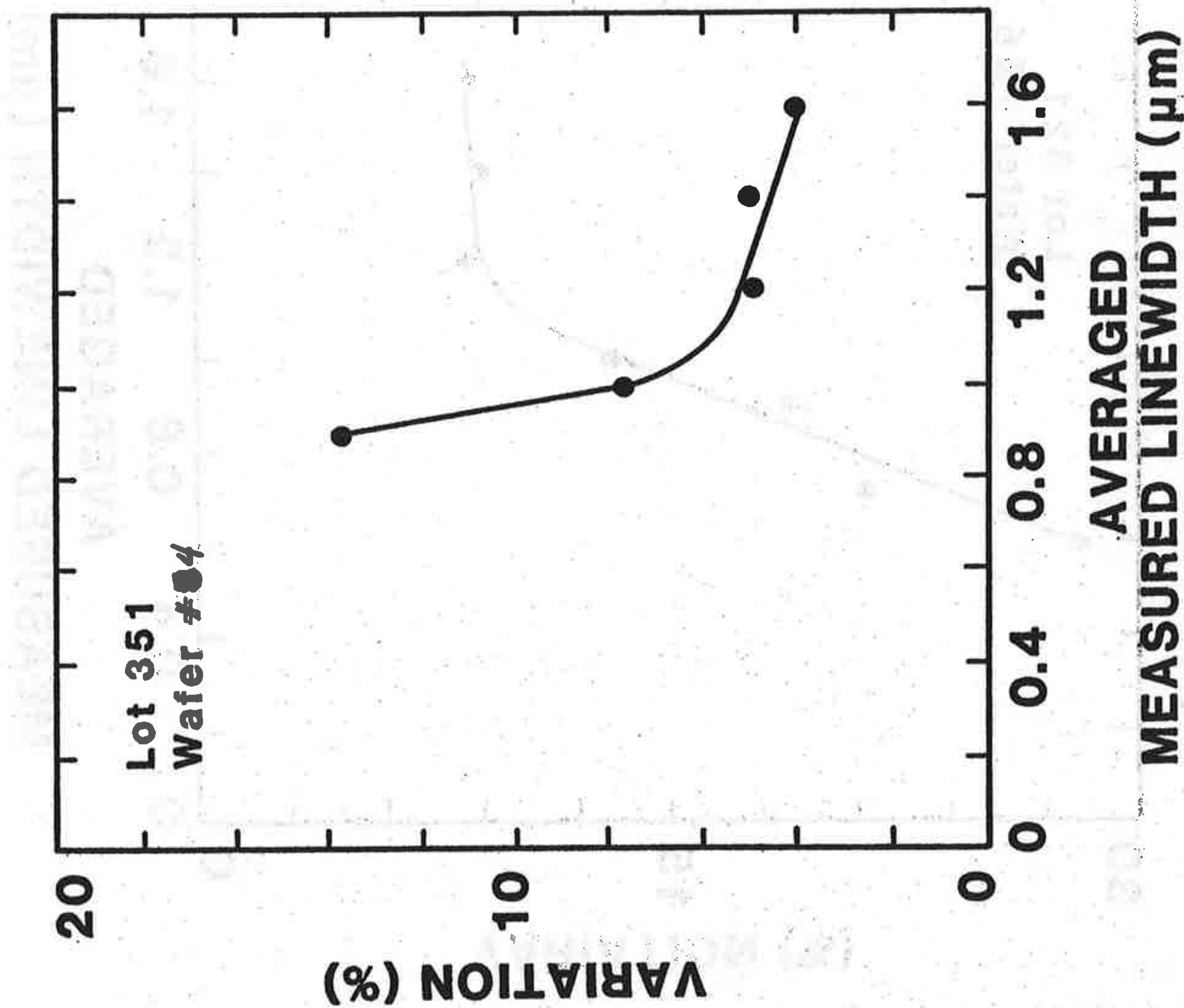
PARAMETRIC TEST SYSTEM

- Computer control wafer prober
- Microvolt and microampere resolutions
- 0.002 μm (1σ) repeatibility

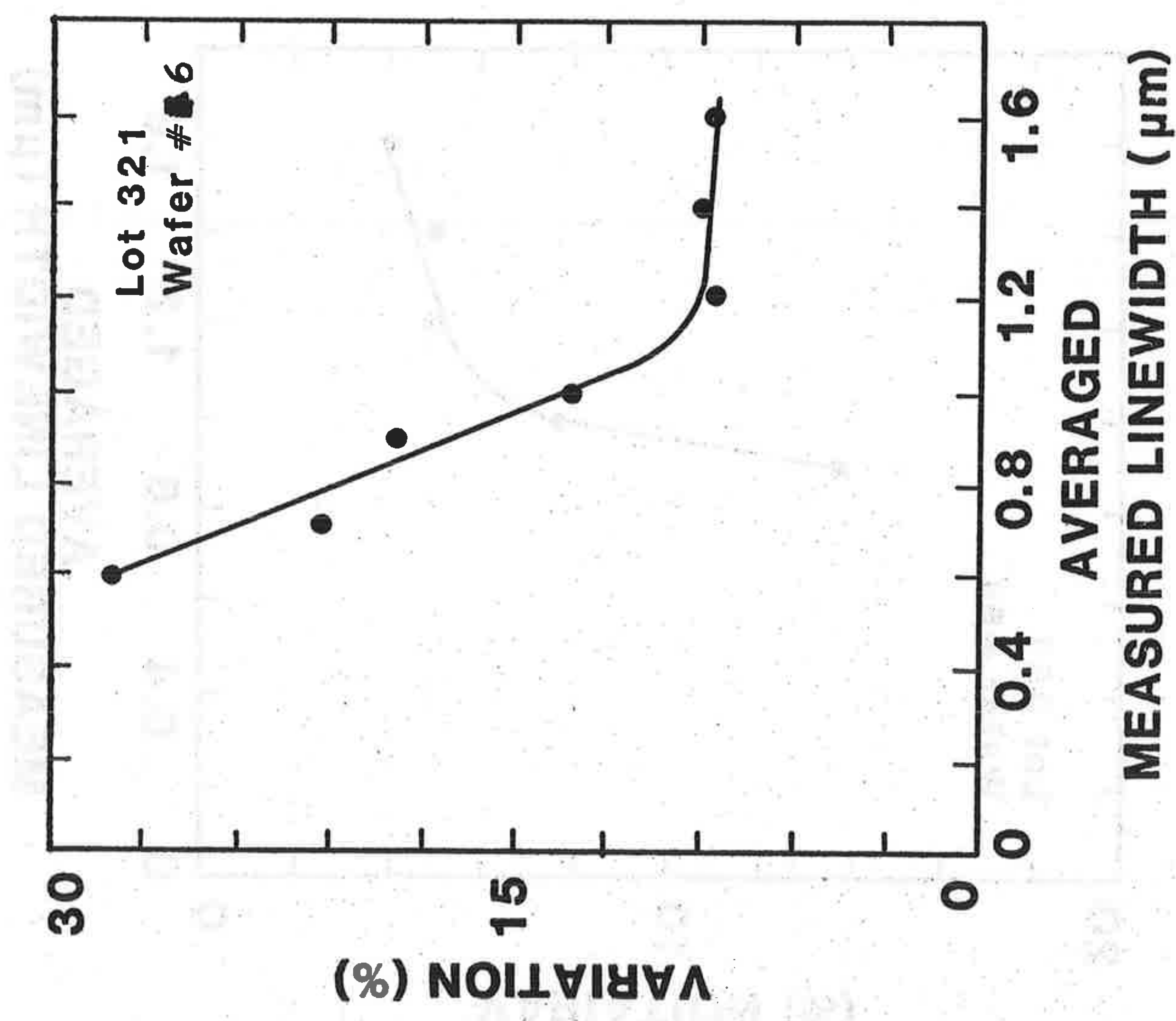

ELECTRICAL LINEWIDTH (µm)
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0
5
10
15
20
25
30
35
40
45
50
POSITION (mm)


Lot 321
Wafer #4
AVERAGED MEASURED LINEWIDTH (µm)
DESIGN LINEWIDTH (µm)
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8


AVERAGED MEASURED LINEWIDTH (μm)
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
Lot 351
Wafer #6
0
0.4
0.8
1.2
1.6
DESIGN LINEWIDTH (μm)



Lot 351
Wafer #4
VARIATION (%)
20
10
0
0
0.4
0.8
1.2
1.6
AVERAGED
MEASURED LINEWIDTH (μm)



Lot 321
Wafer # 6
VARIATION (%)
30
15
0
0
0.4
0.8
1.2
1.6
AVERAGED
MEASURED LINEWIDTH (μm)

LINEWIDTH COMPARISON

Electrical	**1.14 µm**
Optical **(Nyyssonen - NBS)**	**1.10 µm**
SEM **(Kerry - NBS)**	**1.00 µm**

Lot #351
Wafer #6
Die 5,5
Device 3,16

SUMMARY

- Precise and accurate linewidth measurement critical for near/sub. micron process
- Microelectronic test structures provide rapid measurement capability
- Uncertainties comparable to other methods

Integrated Circuit Test Structure for Measuring Mask/Reticle Misalignment

Brian Henderson
Burroughs Micro Components Group

MOS DIGITAL VERNIER

1. TEST STRUCTURE USED TO MEASURE MISALIGNMENT BETWEEN TWO PROCESSED LEVELS.
2. ELECTRICALLY MEASURED USING A D.C. TYPE PARAMETRIC TESTER. THEREFORE SUITABLE FOR MAPPING ALONG WITH OTHER PARAMETRIC TEST STRUCTURES.
3. DESIGN AUTOMATICALLY COMPENSATES FOR OVERETCHING OCCURRING DURING PROCESSING.
4. RANGE AND RESOLUTION IS PRE-DETERMINED TO SUIT A SPECIFIC PROCESS.
5. SAME BASIC DESIGN MAY BE USED IN MEASURING MISALIGNMENT BETWEEN MANY LEVELS.
6. HORIZONTAL AND VERTICAL VERNIERS ARE INCLUDED IN THE SAME STRUCTURE.
7. SIZE 40 MILS X 8 MILS
   1000 μm 200μm

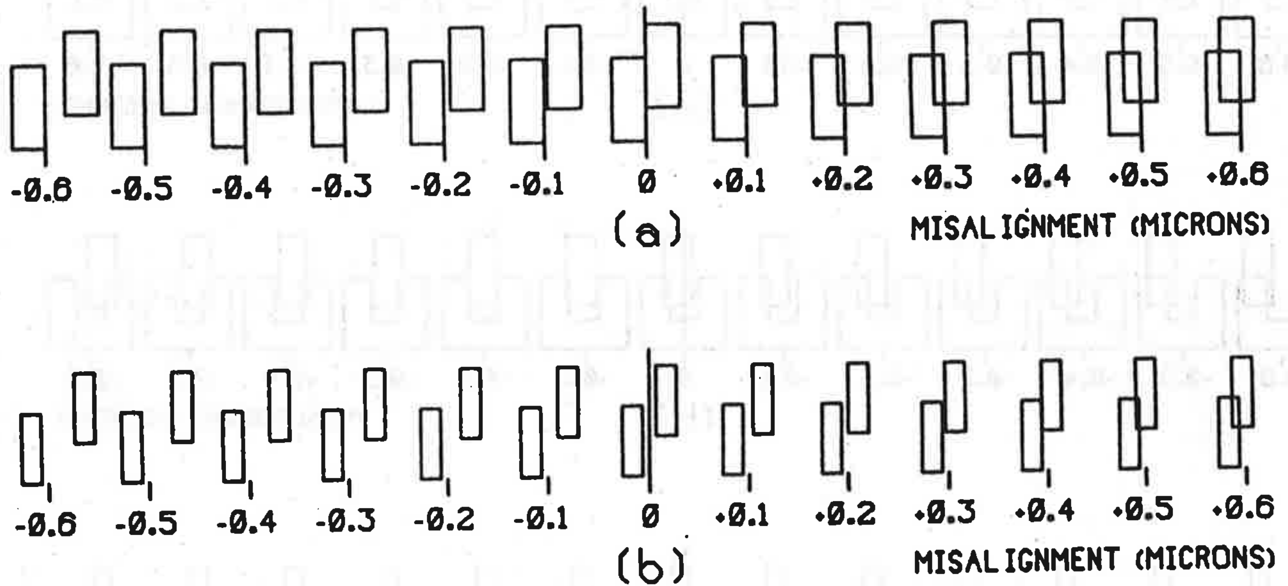
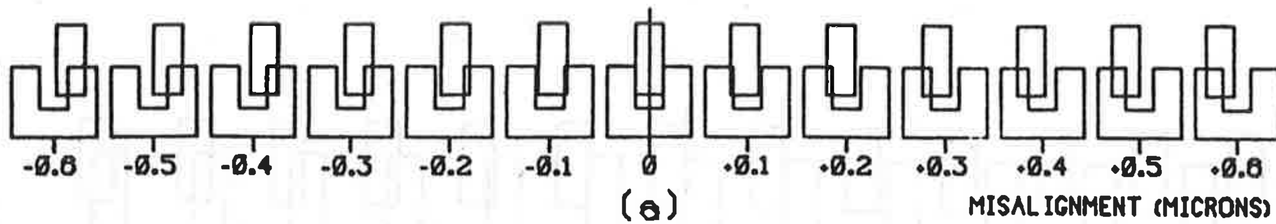
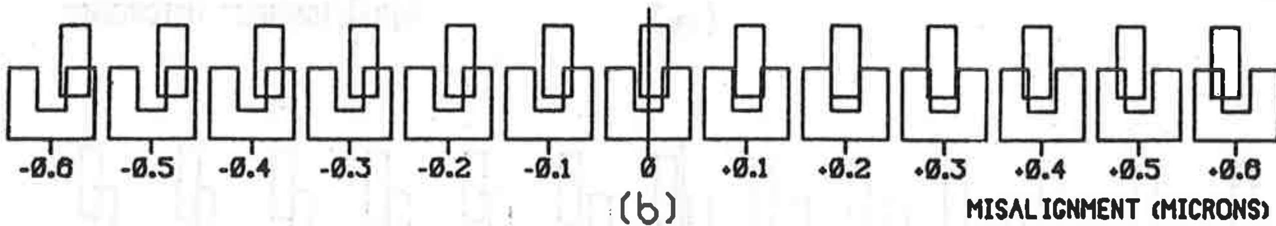


Figure 1: Conventional Vernier (a) no overetching with zero misalignment

(b) 0.2µm over etch on both layers with zero misalignment





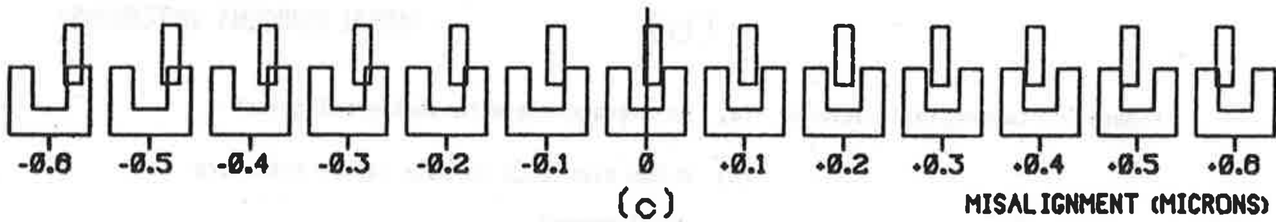
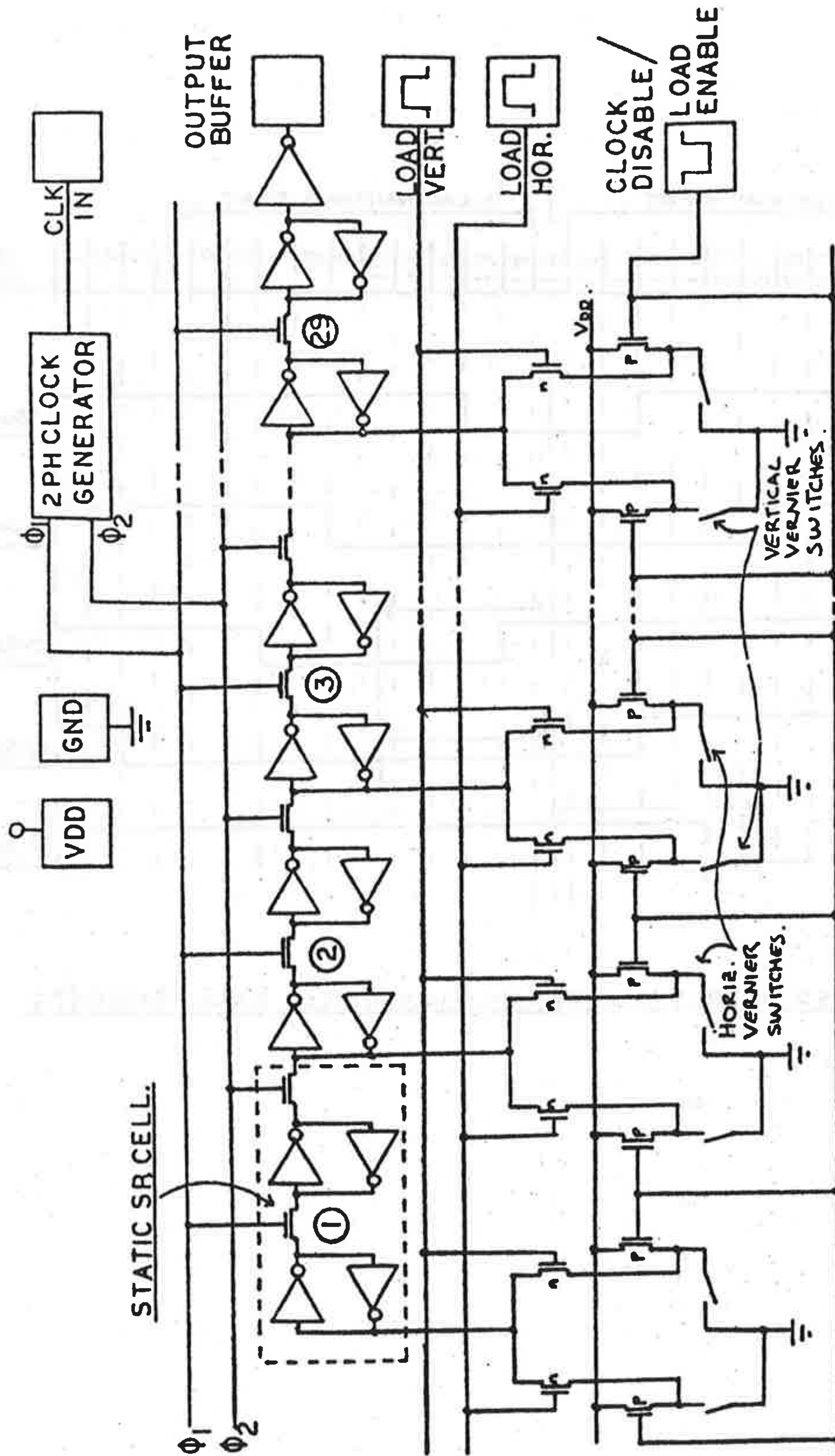
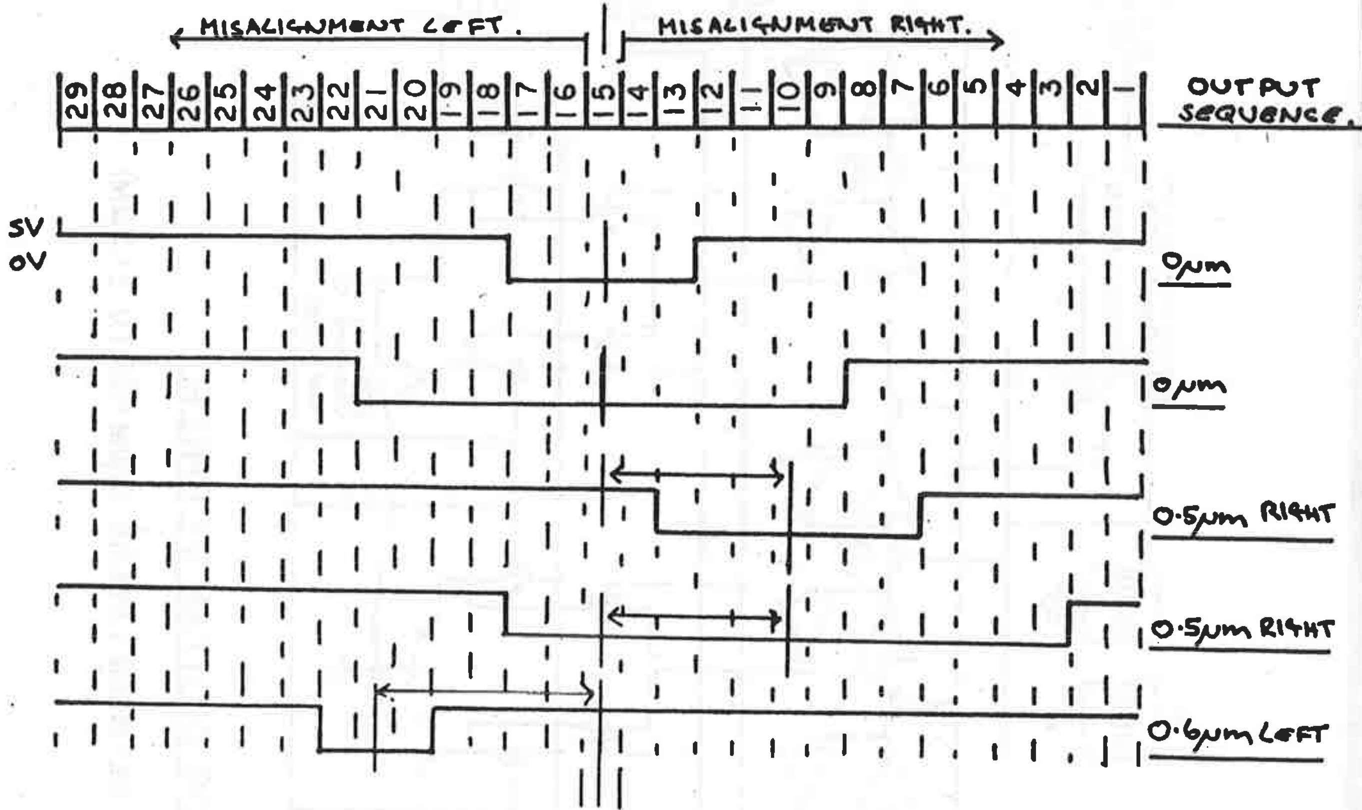


Figure 2: Vernier which compensates for over etching (a) no over etch with zero misalignment
(b) no over etch with +0.2μm misalignment
(c) 0.3μm over etch with +0.2μm misalignment



CMOS DIGITAL VERNIER

(MISALIGNMENT BETWEEN LAYERS. 0.1μM RES. TO ±1.5μM)



VERNIER OUTPUT WAVEFORMS FOR SEVERAL MISALIGNMENTS

LOT# 026004 WAFER# 4

ROW 1 COL 2
HORIZONTAL: 000000000000000000000000000000 VERTICAL: 000000000000000000000000000000-999 -999

ROW 1 COL 3
HORIZONTAL: 111111110011111111111111111111 VERTICAL: 111111110011111111111111111111 .55 .55

ROW 1 COL 4
HORIZONTAL: 111111111100000011111111111111 VERTICAL: 111111111100000011111111111111 .15 .15

ROW 1 COL 5
HORIZONTAL: 111111111100001111111111111111 VERTICAL: 111111111000000111111111111111 .25 .25

ROW 1 COL 6
HORIZONTAL: 111111111000011111111111111111 VERTICAL: 111111111110000011111111111111 .35 .1

ROW 1 COL 7
HORIZONTAL: 111111111111111111111111111111 VERTICAL: 111111111111111111111111111111 888 888

ROW 1 COL 8
HORIZONTAL: 111111111111111111111111111111 VERTICAL: 111111111111111111111111111111 888 888

ROW 2 COL 1
HORIZONTAL: 111111110000001111111111111111 VERTICAL: 111111111110000001111111111111 .35 .05

ROW 2 COL 2
HORIZONTAL: 111111110000001011111111111111 VERTICAL: 111111111100000001111111111111 777 .1

ROW 2 COL 3
HORIZONTAL: 111111111000000001111111111111 VERTICAL: 111111111100000001111111111111 .15 .1

ROW 2 COL 4
HORIZONTAL: 111111111100000011111111111111 VERTICAL: 111111111110000001111111111111 .15 .05

ROW 2 COL 5
HORIZONTAL: 111111111000001111111111111111 VERTICAL: 111111111110000001111111111111 .3 .05

ROW 2 COL 6
HORIZONTAL: 111111111110000111111111111111 VERTICAL: 111111111100001111111111111111 .15 .25

ROW 2 COL 7
HORIZONTAL: 111111111000001111111111111111 VERTICAL: 111111111000011111111111111111 .3 .35

ROW 2 COL 8
HORIZONTAL: 111111111101111111111111111111 VERTICAL: 111111100111111111111111111111 .5 .65

ROW 2 COL 9
HORIZONTAL: 111111111111111111111111111111 VERTICAL: 111111111111111111111111111111 888 888

ROW 3 COL 1
HORIZONTAL: 111111111110000011111111111111 VERTICAL: 111111111100000011111111111111 .1 .15

ROW 3 COL 2
HORIZONTAL: 111111111110000001111111111111 VERTICAL: 111111111100000111111111111111 .05 .2

ROW 3 COL 3
HORIZONTAL: 111111111100000011111111111111 VERTICAL: 111111111100000111111111111111 .15 .2

ROW 3 COL 4
HORIZONTAL: 111111111100001111111111111111 VERTICAL: 111111111100011111111111111111 .25 .3

ROW 3 COL 5

RAW DATA

8446-3031H PARAMETRIC TESTING

LOT: 026004, WAFER: 4, PRODUCT: 3031, TESTED ON: 2-16-84, BY: CONNIE
TO DATA DISK: 51, WITH PROGRAM: TESTVERN.446, REV A, 2-15-84 LIMIT FILE:
86700 DISK FILENAME: 8446/3031H/026004/4

PARAMETER: BH001 H MISALGN CNT-DIF DATA UNITS: MICRONS

COL.#	1	2	3	4	5	6	7	8	9
R 1		LO	0.350	0.150	0.250	0.350	HI	HI	
R 2	0.350	HI	0.150	0.150	0.300	0.150	0.300	0.500	HI
R 3	0.100	0.050	0.150	0.250	0.000	0.100	HI	HI	HI
R 4		HI	HI	HI	0.150	HI	HI	HI	

```
LOW        X                    3.1%
  -1.500                        0.0%
  -1.400                        0.0%
  -1.300                        0.0%
  -1.200                        0.0%
  -1.100                        0.0%
  -1.000                        0.0%
  -0.900                        0.0%
  -0.800                        0.0%
  -0.700                        0.0%
  -0.600                        0.0%
  -0.500                        0.0%
  -0.400                        0.0%
  -0.300                        0.0%
  -0.200                        0.0%
  -0.100   X                    3.1%
 2.9E-11   XXX  •               9.4%
   0.100   XXXXXX•   • OPTICAL 18.8%
   0.200   XXXX •              12.5%
   0.300   *X                   6.3%
   0.400   X                    3.1%
   0.500   X                    3.1%
   0.600                        0.0%
   0.700                        0.0%
   0.800                        0.0%
   0.900                        0.0%
   1.000                        0.0%
   1.100                        0.0%
   1.200                        0.0%
   1.300                        0.0%
   1.400                        0.0%
HI         XXXXXXXXXXXXX       40.6%
```

MEAN: 0.222 SIGMA: 0.144
SAMPLE SIZE: MEAN BASED ON 18 DATA POINTS

STATISTICAL LIMITS: MINIMUM=-1.5, MAXIMUM=1.5

LOT: 026004, WAFER: 4, PRODUCT: 3021, TESTED ON: 2-16-84, BY: CONNI
TO DATA DISK: 317, WITH PROGRAM: TESTVERN.446, REV A, 2-15-84 LIMIT
B6700 DISK FILENAME: 3445/3021H/026004/4

PARAMETER: 3H001 V MISALGN CNT-DIF DATA UNITS: MICRONS

COL.#	1	2	3	4	5	6	7	8	
R 1		LO	0.550	0.150	0.250	0.100	HI	HI	
R 2	0.050	0.100	0.100	0.050	0.050	0.250	0.350	0.650	HI
R 3	0.150	0.200	0.200	0.300	0.100	0.200	HI	HI	HI
R 4		0.300	HI	HI	0.150	HI	HI	HI	

LOW	X	3.1%
-1.500		0.0%
-1.400		0.0%
-1.300		0.0%
-1.200		0.0%
-1.100		0.0%
-1.000		0.0%
-0.900		0.0%
-0.800		0.0%
-0.700		0.0%
-0.600		0.0%
-0.500		0.0%
-0.400		0.0%
-0.300		0.0%
-0.200		0.0%
-0.100		0.0%
2.9E-11	XXXXX*X	21.9%
0.100	XXXXXX	18.8%
0.200	XX*X	12.5%
0.300	*	3.1%
0.400		0.0%
0.500	X	3.1%
0.600	X	3.1%
0.700		0.0%
0.800		0.0%
0.900		0.0%
1.000		0.0%
1.100		0.0%
1.200		0.0%
1.300		0.0%
1.400		0.0%
HI	XXXXXXXXXXX	34.4%

• OPTICAL.

MEAN: 0.213 SIGMA: 0.156
SAMPLE SIZE: MEAN BASED ON 20 DATA POINTS

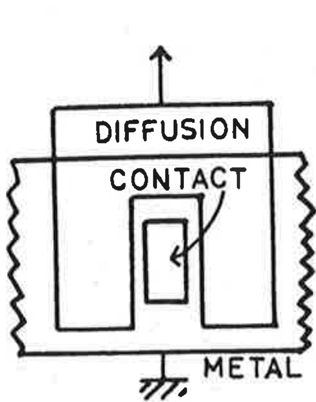
STATISTICAL LIMITS: MINIMUM=-1.5, MAXIMUM=1.5

47

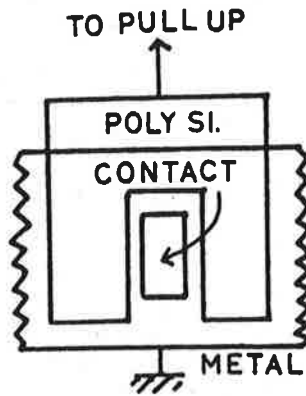
DIGITAL ±0·05μ.	OPTICAL±?
·15	·2
·25	·1
−·10	−·1
·05	0
·10	·1
·10	0
−·05	0
−·55	−·3
·20	0
−·30	−·1
·15	·1
·10	·1
−·65	−·3
·30	·2

COMPARISON OF DIGITAL AND OPTICAL DATA

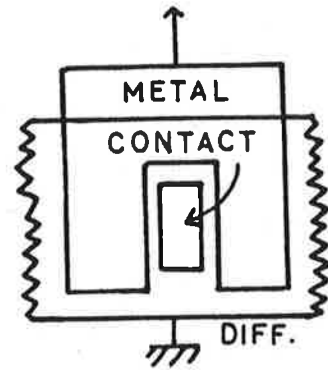
STRUCTURES FOR VARIOUS LAYERS.



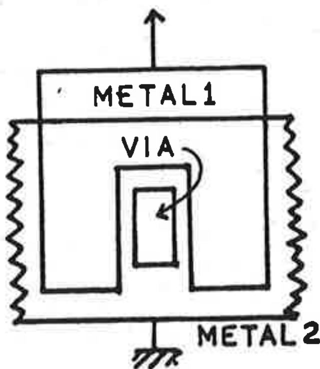
CONTACT TO DIFFUSION.



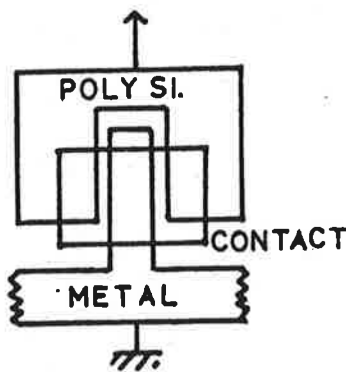
CONTACT TO POLYSI



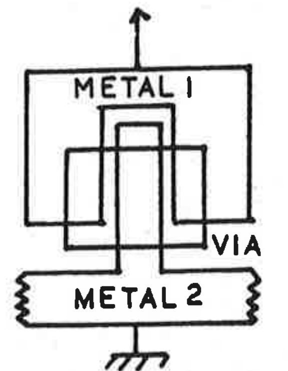
CONTACT TO METAL.



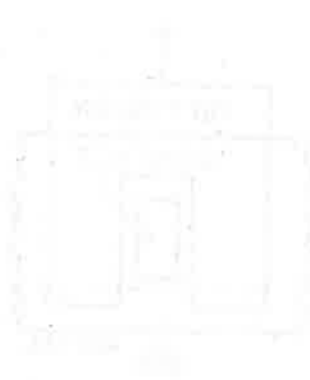
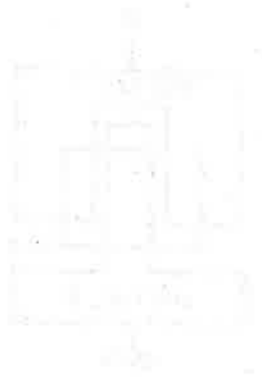
METAL 1 TO VIA.

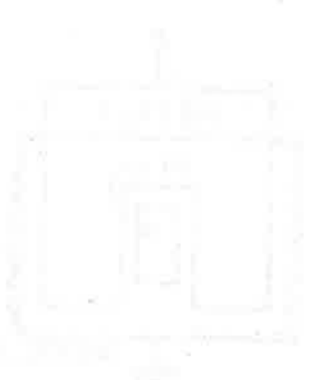


METAL TO POLY Si.



METAL 1 TO METAL 2.



Lifetime Interpretation from Silicon Test Structures

Dieter K. Schroder
Arizona State University
EE Dept.

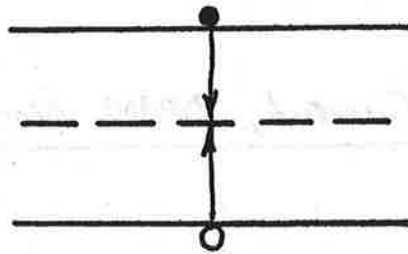
- Concept of Recombination and Generation Lifetimes

- Measurement Test Structures

- Interpretation of Experimental Data

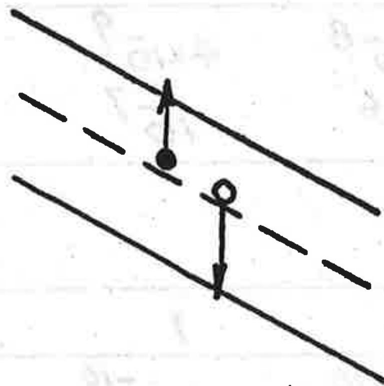
- Summary

Recombination:



$$\tau_r = \frac{1}{\sigma_n v_{th} N_T} = \frac{1}{10^{-15} \times 10^{7} \times 10^{13}} = \underline{10\ \mu s}$$

Generation:



$$\tau_g = \frac{e^{(E_T - E_i)/kT}}{\sigma_p v_{th} N_T} + \frac{e^{-(E_T - E_i)/kT}}{\sigma_n v_{th} N_T} \simeq \tau_r e^{|(E_T - E_i)/kT|}$$

$$\simeq \underline{500\ \mu s} \text{ for } E_T = E_i \pm 4kT$$

For same N_T!

Junction Leakage Current, DRAM Discharge Current:

$$J = \frac{q n_i W}{\tau_g} + \frac{q n_i^2 \sqrt{D_n}}{N_A \sqrt{\tau_r}} = J_{scr} + J_{bulk}$$

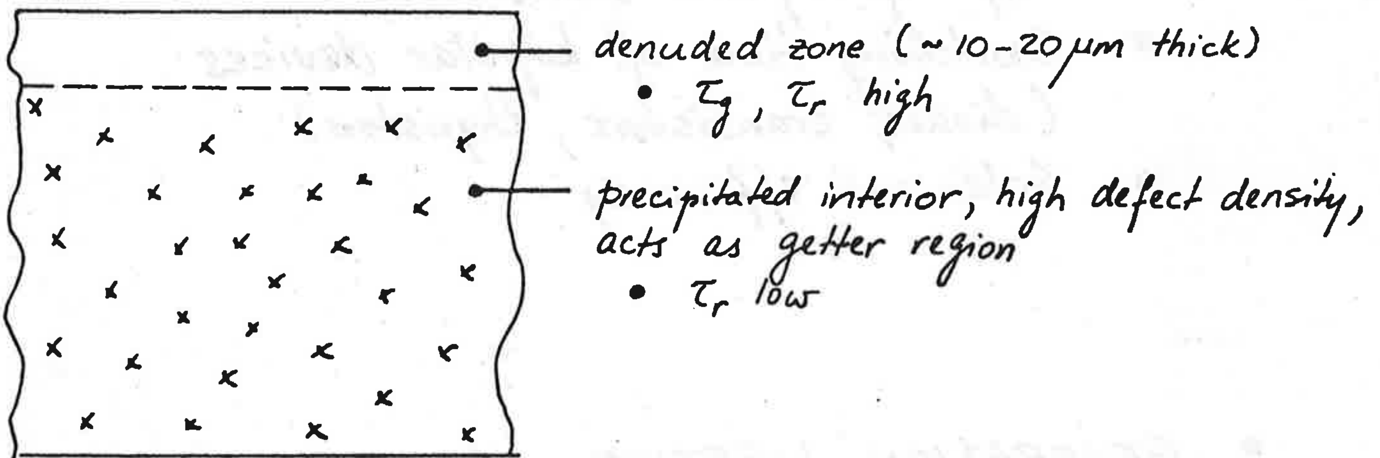
τ_g (μs)	10	100	1000	
J_{scr} (A/cm^2)	4×10^{-8}	4×10^{-9}	4×10^{-10}	27°C
	10^{-6}	10^{-7}	10^{-8}	70°C

τ_r (μs)	0.1	1	10	
J_{bulk} (A/cm^2)	5×10^{-10}	2×10^{-10}	5×10^{-11}	27°C
	3×10^{-7}	9×10^{-8}	3×10^{-8}	70°C

Intrinsic Gettering: $\tau_g \uparrow$, $\tau_r \downarrow$

EXAMPLE : Intrinsic Gettering

- Certain anneals cause oxygen to outdiffuse in a surface layer (denuded zone) and precipitate in the bulk.



- τ_g measurement characterizes high quality "denuded zone"

- τ_r measurement is a combination of high "denuded zone" value and low "precipitated interior" value.

- RECOMBINATION LIFETIME

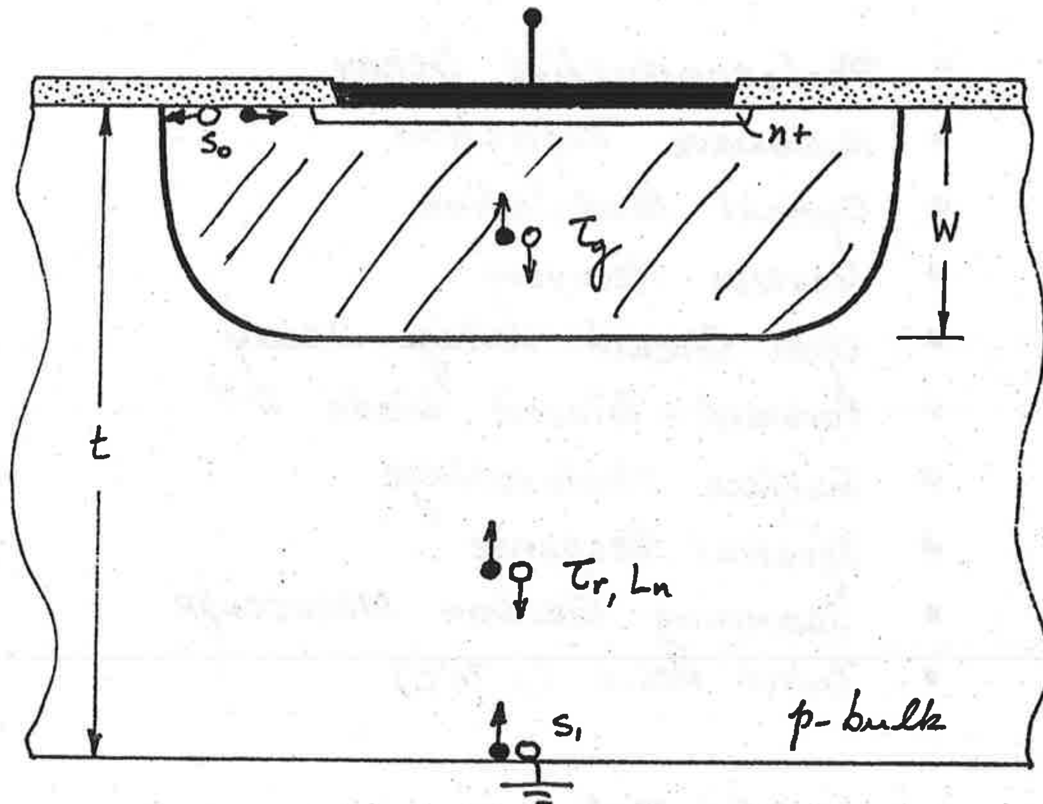
    - Diode forward voltage drop
    - α, β of bipolar transistors
    - Switching time of bipolar devices (diodes, transistors, thyristors)
    - Solar cell efficiency

- GENERATION LIFETIME

    - Junction diode leakage current
    - MOS capacitor holding time (dynamic RAM refresh time)
    - CMOS leakage current
    - CCD dark current, noise, dynamic range

LIFETIME

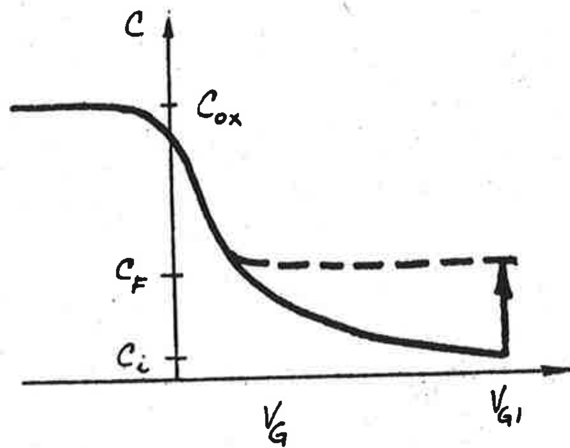
- Recombination Lifetime
  - Photoconductive Decay
  - Microwave Reflection
  - Optical Modulation
  - Reverse Recovery
  - Open Circuit Voltage Decay
  - Forward - Biased Diode I-V
  - Surface Photovoltage
  - Spectral Response
  - Scanning Electron Microscope
  - Pulsed MOS-C (~70°C)
- Generation Lifetime
  - Pulsed MOS Capacitor
  - Reverse - Biased Diode I-V

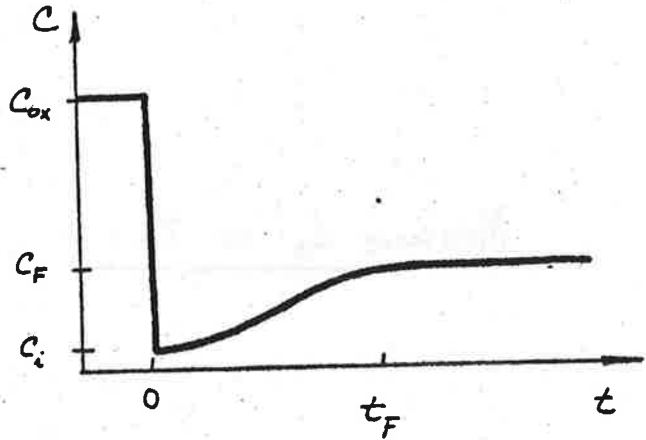


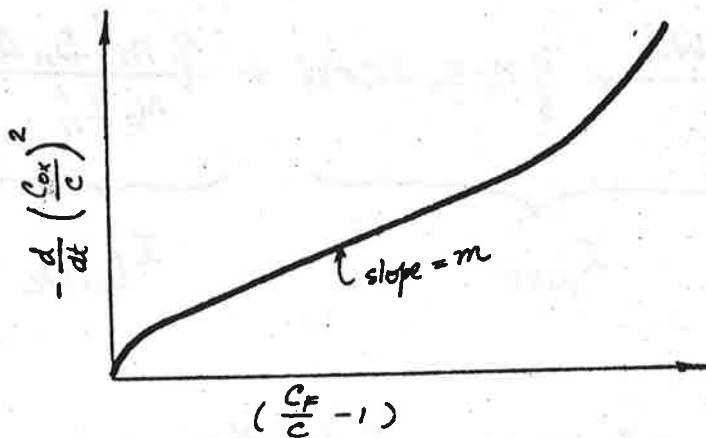
$$I = q\frac{n_i W A}{\tau_g} + q n_i s_0 A_s + q\frac{n_i^2 D_n A}{N_A L_n'}$$

$$(L_n' = f(L_n, s_1, t/L_n))$$

PULSED MOS-C ('Zerbst')







$$\tau_g = \frac{2\, n_i\, C_{ox}}{m\, N_A\, C_F}$$

or

$$\tau_g \simeq \frac{n_i}{8 N_D} \frac{C_F\, t_F}{C_{ox}} \left(1 + C_i/C_F\right)^2 \quad \text{(rough approx.)}$$

D.K. Schroder and J. Guldberg, "Interpretation of Surface and Bulk Effects Using the Pulsed MIS Capacitor", Solid-State Elect. 14, 1285-1297, 1971.

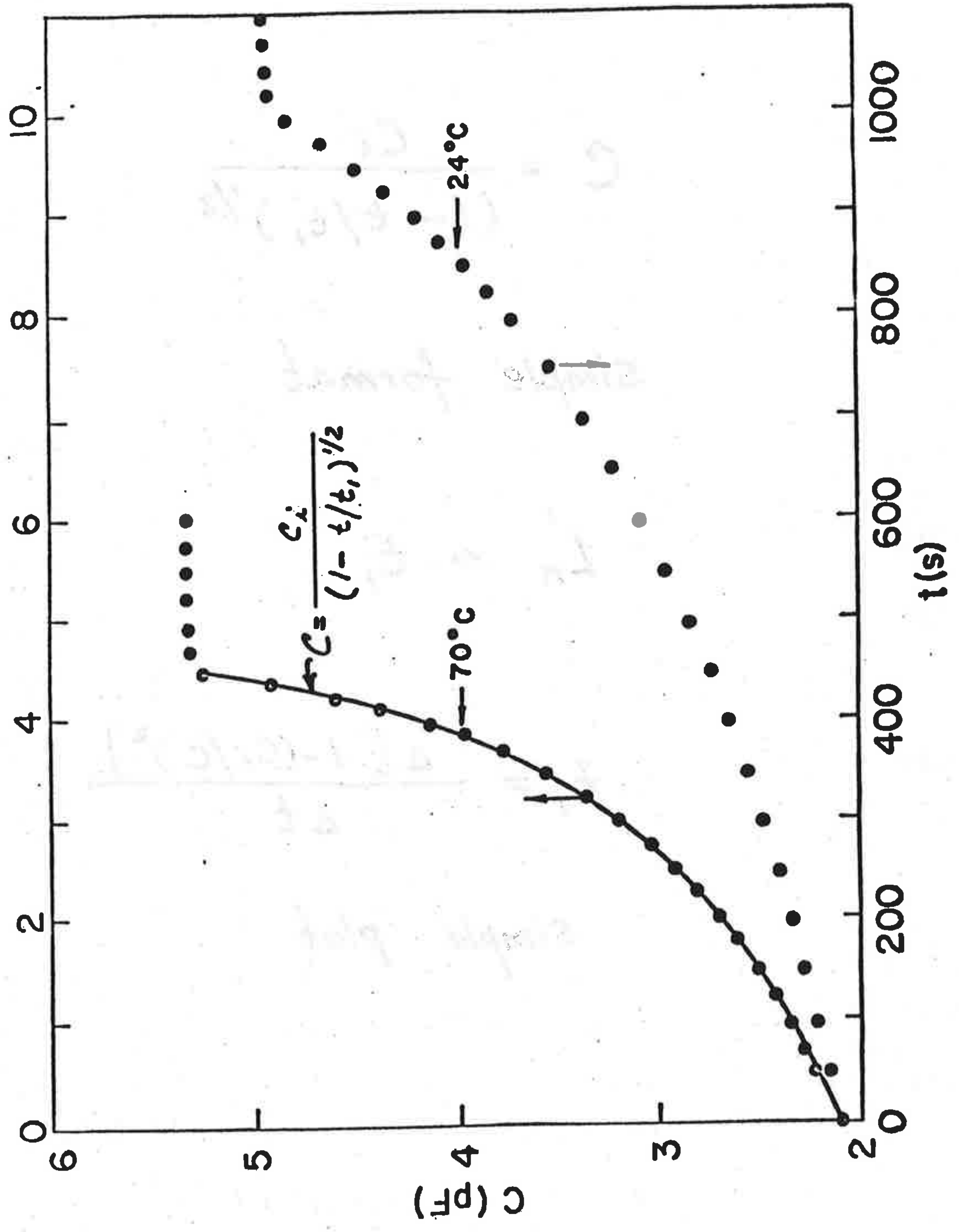
Measure L_n' or τ_r :

$$I = \underbrace{\frac{q n_i W A}{\tau_g} + q n_i s_0 2\pi r W}_{I_{per}} + \underbrace{\frac{q n_i^2 D_n A}{N_A L_n'}}_{I_{bulk}}$$

$T \uparrow$ n_i^2 increases faster than n_i

$$\therefore \quad I \simeq \frac{q n_i^2 D_n A}{N_A L_n'}$$

$$\Rightarrow \quad \boxed{C(t) = \frac{C_i}{\sqrt{1 - t/t_1}}}$$



C (pF)
t(s)
24°C
70°C
$C = \frac{C_i}{(1 - t/t_1)^{1/2}}$

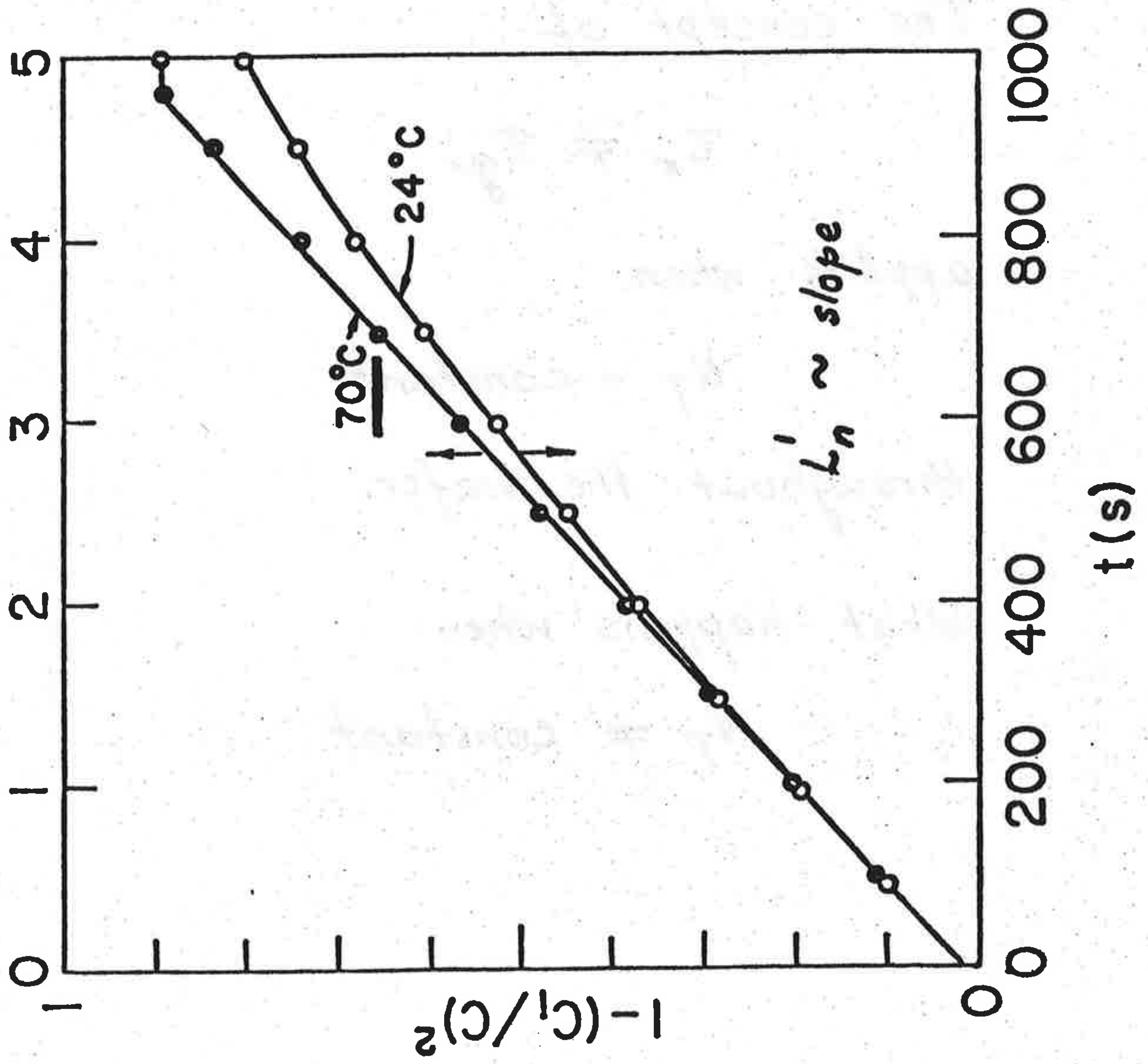
$$C = \frac{C_i}{(1 - t/t_1)^{1/2}}$$

simple format

$$L_n' \sim t_1$$

$$t_1 = \frac{\Delta\left[1 - (C_i/C)^2\right]}{\Delta t}$$

simple plot


0
1
2
3
4
5
70°C
24°C
L'n ~ slope
0
200
400
600
800
1000
t (s)
0
1
1 - (C1/C)2

The concept of

$$\tau_r \neq \tau_g$$

applies when

$$N_T = \text{constant}$$

throughout the wafer.

What happens when

$$N_T \neq \text{constant}$$

Room Temperature C-t:

- space-charge region generation dominant

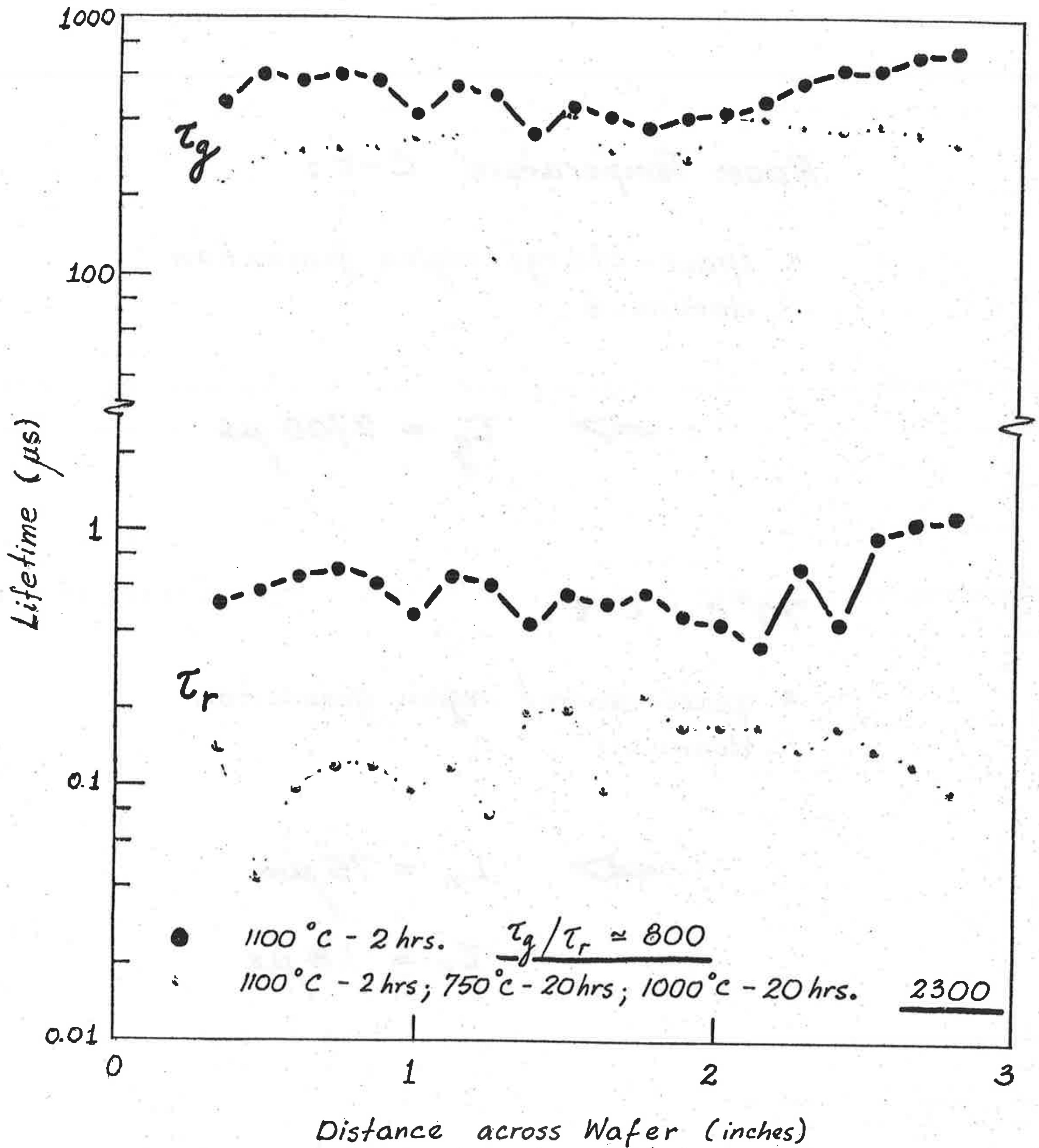
⇨ $\tau_g = 2700\,\mu s$

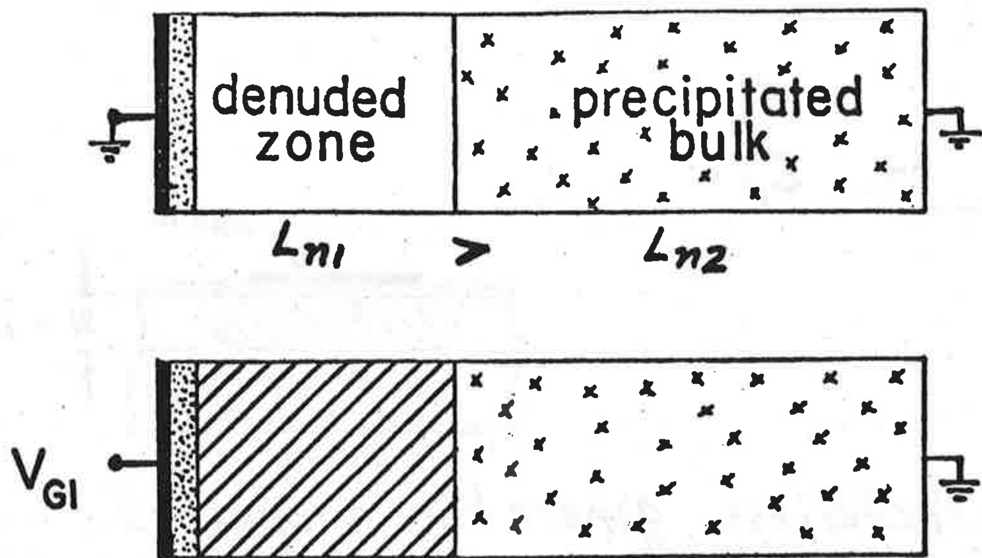
70°C C-t:

- quasi-neutral region generation dominant

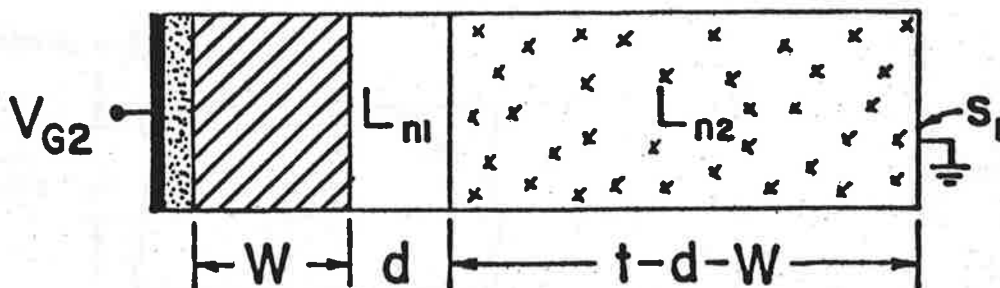
⇨ $L_n = 75\,\mu m$

$\tau_r = 1.8\,\mu s$


1000
100
1
0.1
0.01
Lifetime (μs)
τg
τr
1100 °C - 2 hrs.
τg / τr ≃ 800
1100 °C - 2 hrs; 750 °C - 20 hrs; 1000 °C - 20 hrs.
2300
0
1
2
3
Distance across Wafer (inches)



(a)

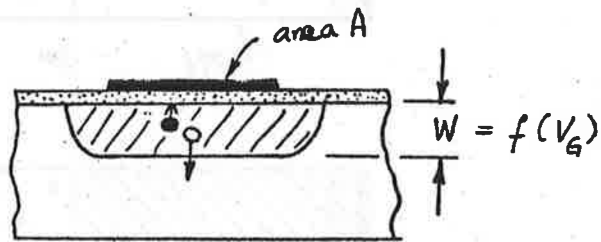


(b)

$$L_n'' \simeq \frac{d + L_{n2}}{1 + L_{n2}/L_{n1}} \simeq d + L_{n2}$$

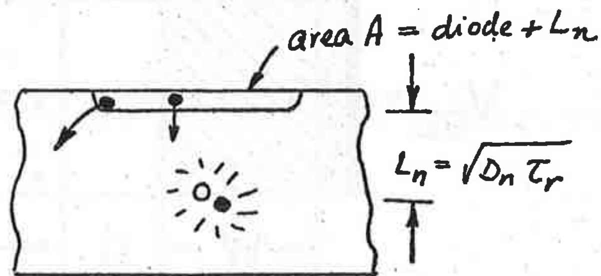
τ_g vs. τ_r

τ_g:



- characterizes generation properties
- volume ($W \times A$) under operator's control
- characterizes semiconductor locally ($W \approx 1\,\mu m$)
- characterizes the active part of MOS devices

τ_r:



- characterizes recombination properties
- volume ($L_n \times A$) not under operator's control
- characterizes semiconductor globally (for $\tau_r = 10\,\mu s$, $L_n = 150\,\mu m$)
- characterizes interior of wafer, not important for MOS devices (for intrinsically gettered material, measures poor interior)

Summary:

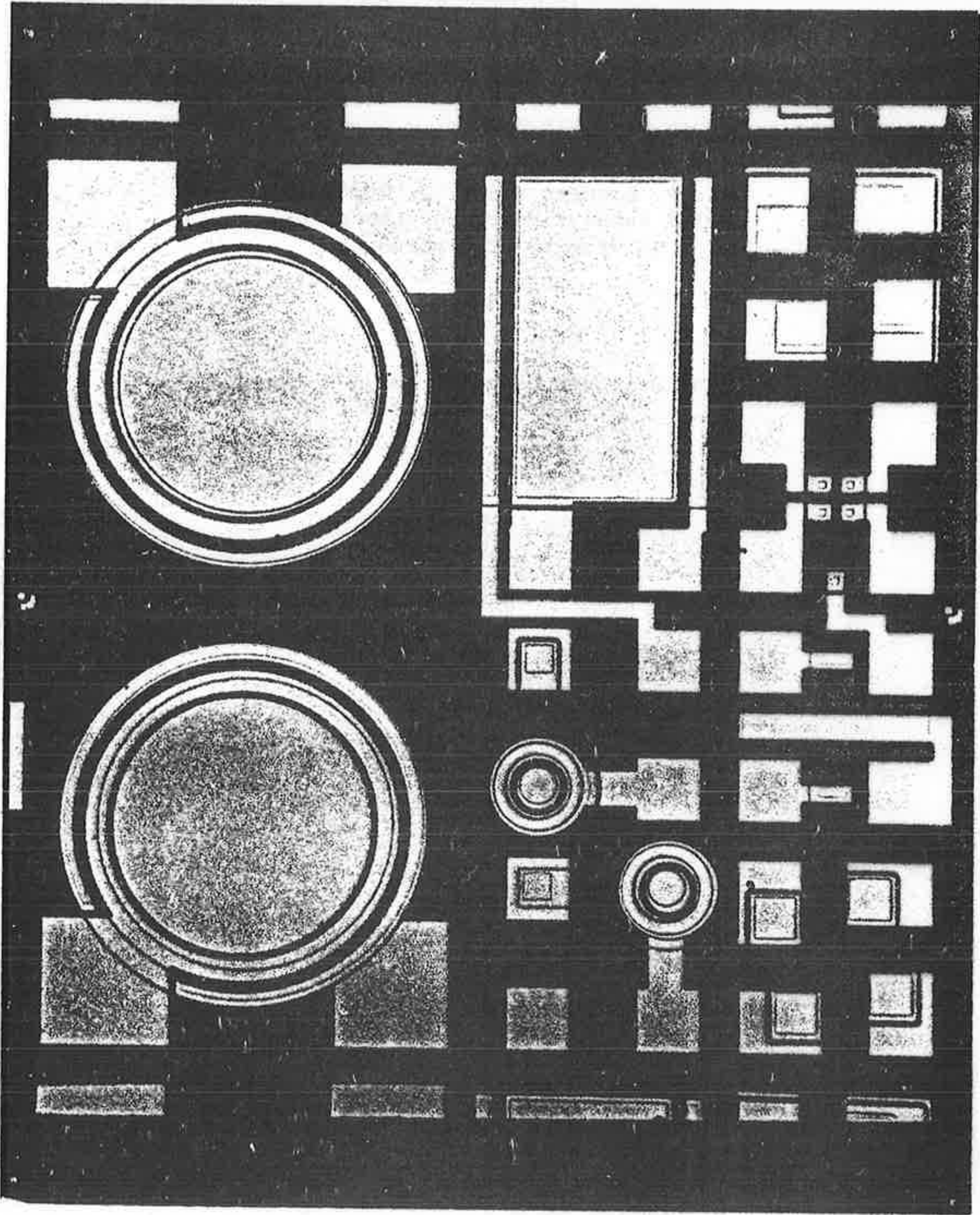
- Concept of τ_g and τ_r
- Useful parameters to
  - know for device predictors
  - use as process monitors
- MOS-C as test structure
- Example: intrinsic gettering

Electrical Characterization of Epitaxial Silicon

K. P. Roenker and T. J. Morthorst
Solid State Electronics Laboratory
University of Cincinnati

and

C. Baylis
Applied Sciences Research and Development
Cincinnati Milacron



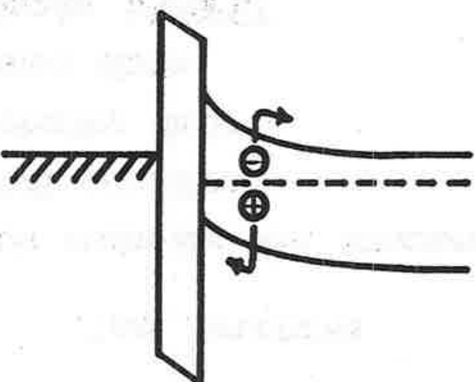
EPI-1 TEST CHIP

Test Structures	Electrical Parameters
bulk resistivity test structure	resistivity or sheet resistance
MOS capacitor	dopant density
Schottky diode	generation lifetime
gated diode	mobility (majority carrier)
circular MOSFET	
JFET	
deep depletion MOSFET	

Generation Lifetime Measurement

(Modified Linear Sweep Technique – Pierret+)

MOS Capacitor

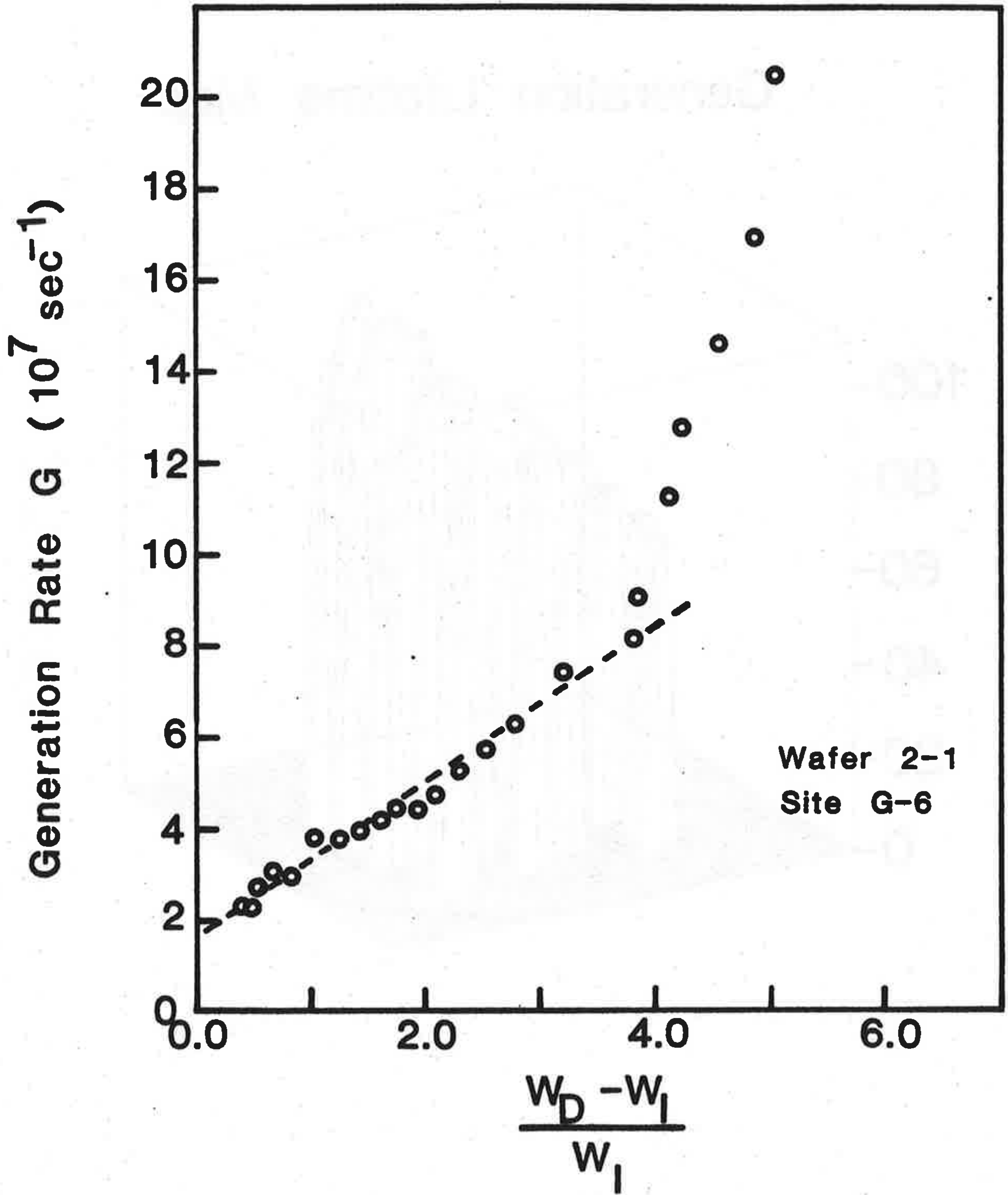


Technique: Pulse into deep depletion and adjust bias to hold capacitance constant.

$$I_G = \frac{q n_i A_G (W_D - W_I)}{\tau_G} = C_{ox} \frac{dV_G}{dt}$$

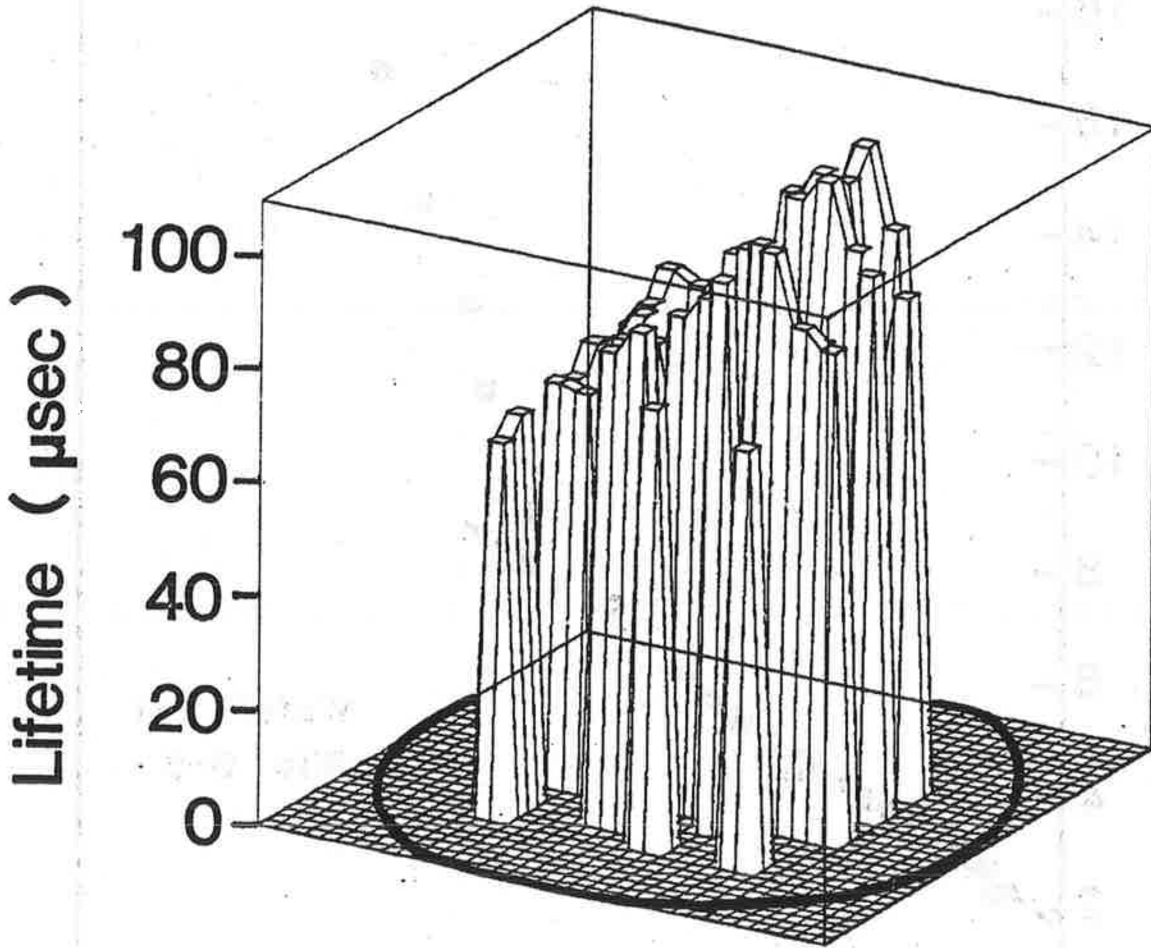
$$\tau_G = \frac{q n_i A_G (W_D - W_I)}{C_{ox} \frac{dV_G}{dt}}$$

+IEEE Trans. Electr. Dev. ED-22, 1975, p1051.

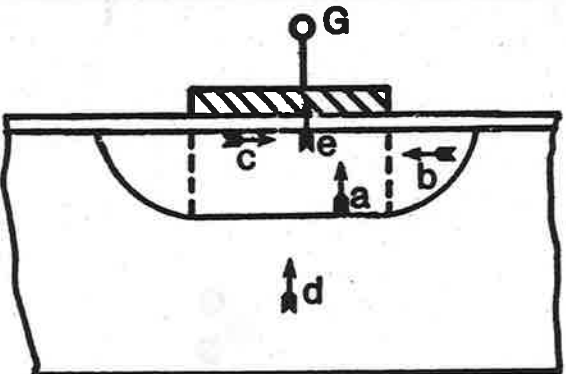


Generation Rate vs Depth
Generation Rate G (10^7 sec^{-1})
20
18
16
14
12
10
8
6
4
2
0
0.0
2.0
4.0
6.0
$\frac{W_D - W_I}{W_I}$
Wafer 2-1
Site G-6

Generation Lifetime Map



Refinements in τ_G Determination[+]



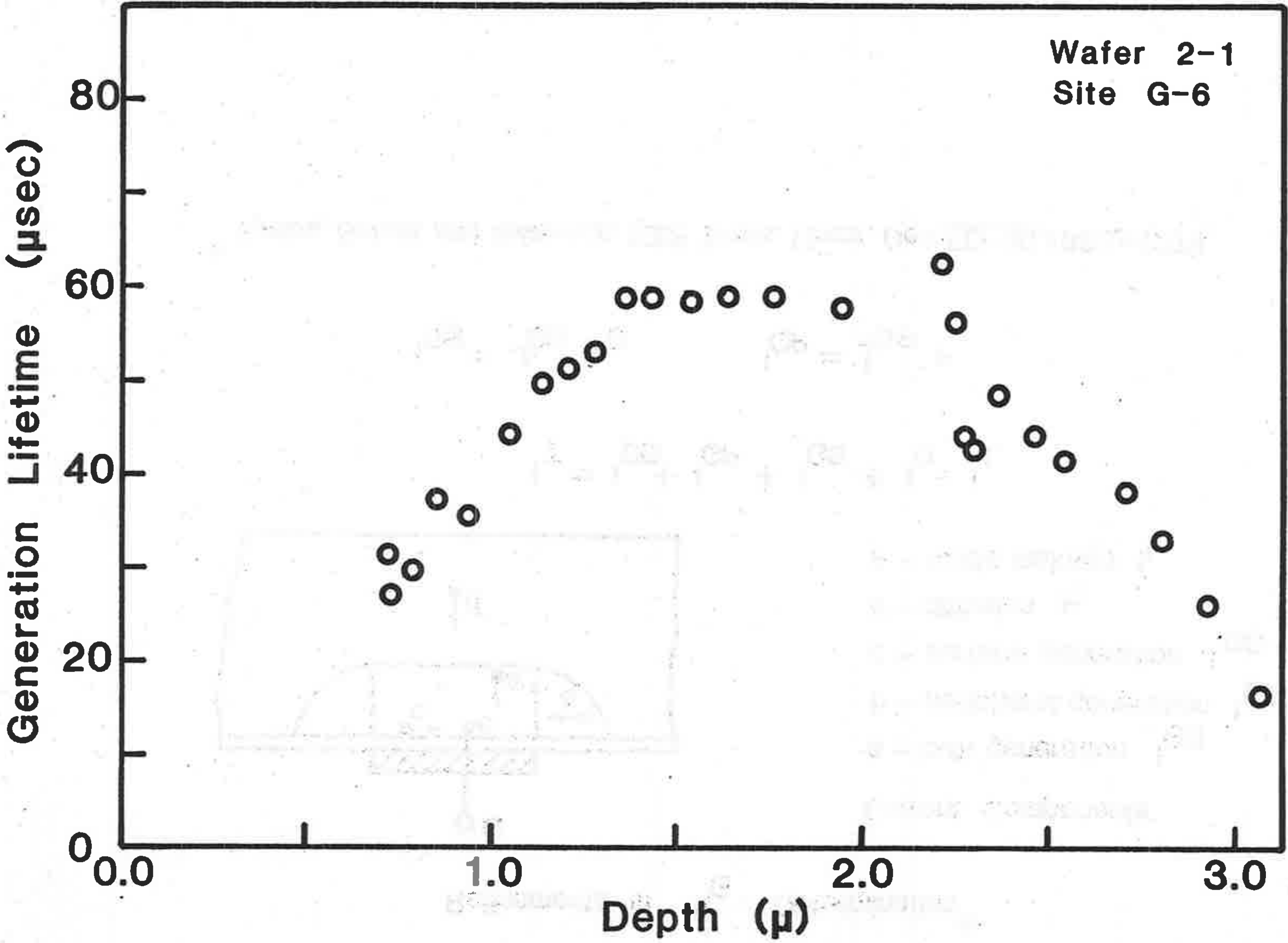
Current Components

a – bulk generation I_{GB}
b – peripheral generation I_{GP}
c – surface generation I_{GS}
d – diffusion I_D
e – oxide leakage I_L

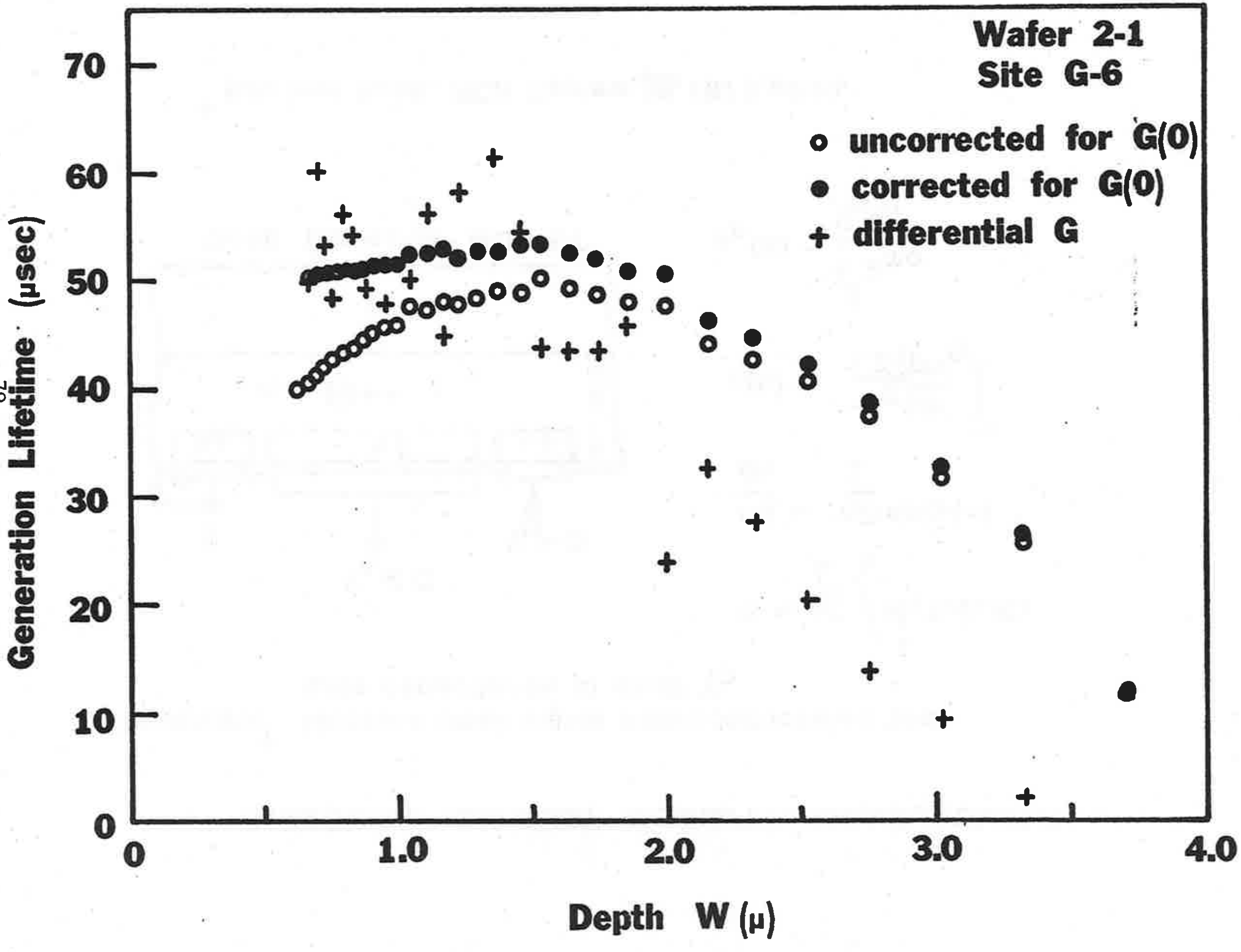
$$I_T = I_{GB} + I_{GP} + I_{GS} + I_D - I_L$$

$$I_{GB} = J_{GB} A_G \qquad I_{GP} = J_{GP} P$$

[+] Eades, Schott and Swanson, IEEE Trans. Electr. Dev., ED-30, 1983, p1274.

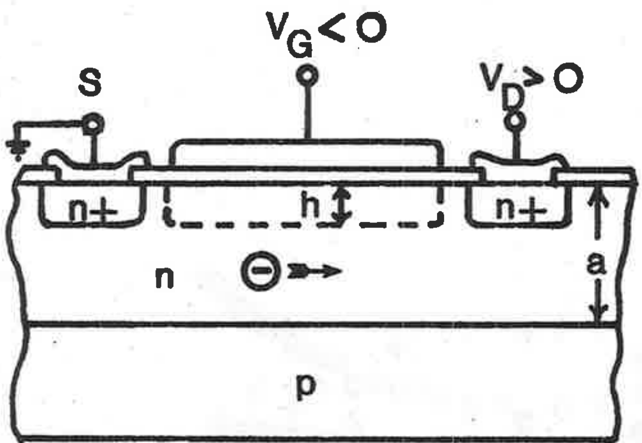


Generation Lifetime Profile
Wafer 2-1
Site G-6
Generation Lifetime (μsec)
Depth (μ)
0.0
1.0
2.0
3.0
0
20
40
60
80


GENERATION LIFETIME PROFILE
Wafer 2-1
Site G-6
uncorrected for G(0)
corrected for G(0)
differential G
Generation Lifetime (μsec)
Depth W (μ)
0
10
20
30
40
50
60
70
1.0
2.0
3.0
4.0

MAJORITY CARRIER MOBILITY MEASUREMENT

Technique[+]: Measure small signal transconductance and gate capacitance at small V_D



Deep Depletion MOSFET

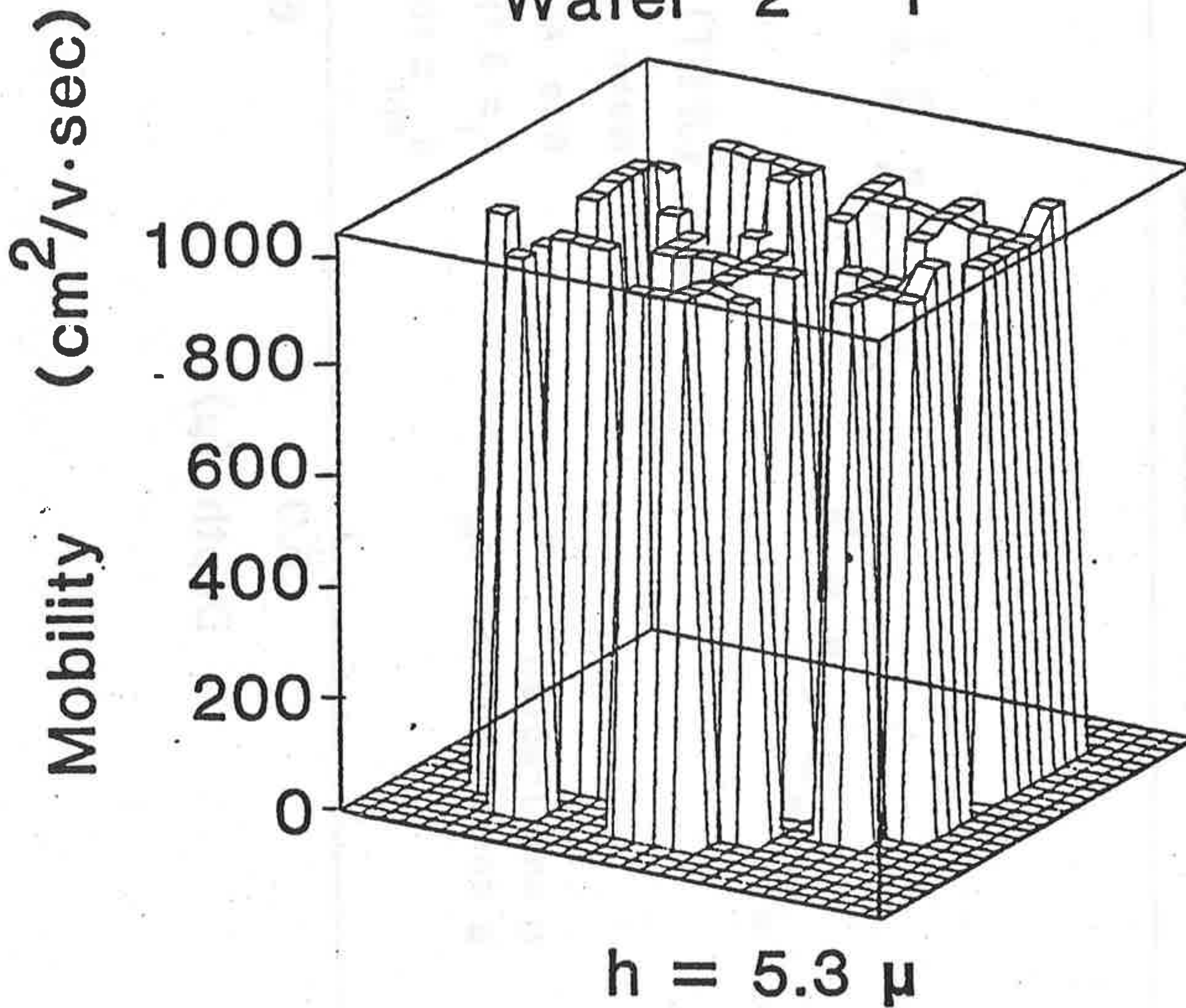
$$G = \frac{qZ}{L}\int_h^a n(y)\mu(y)dy$$

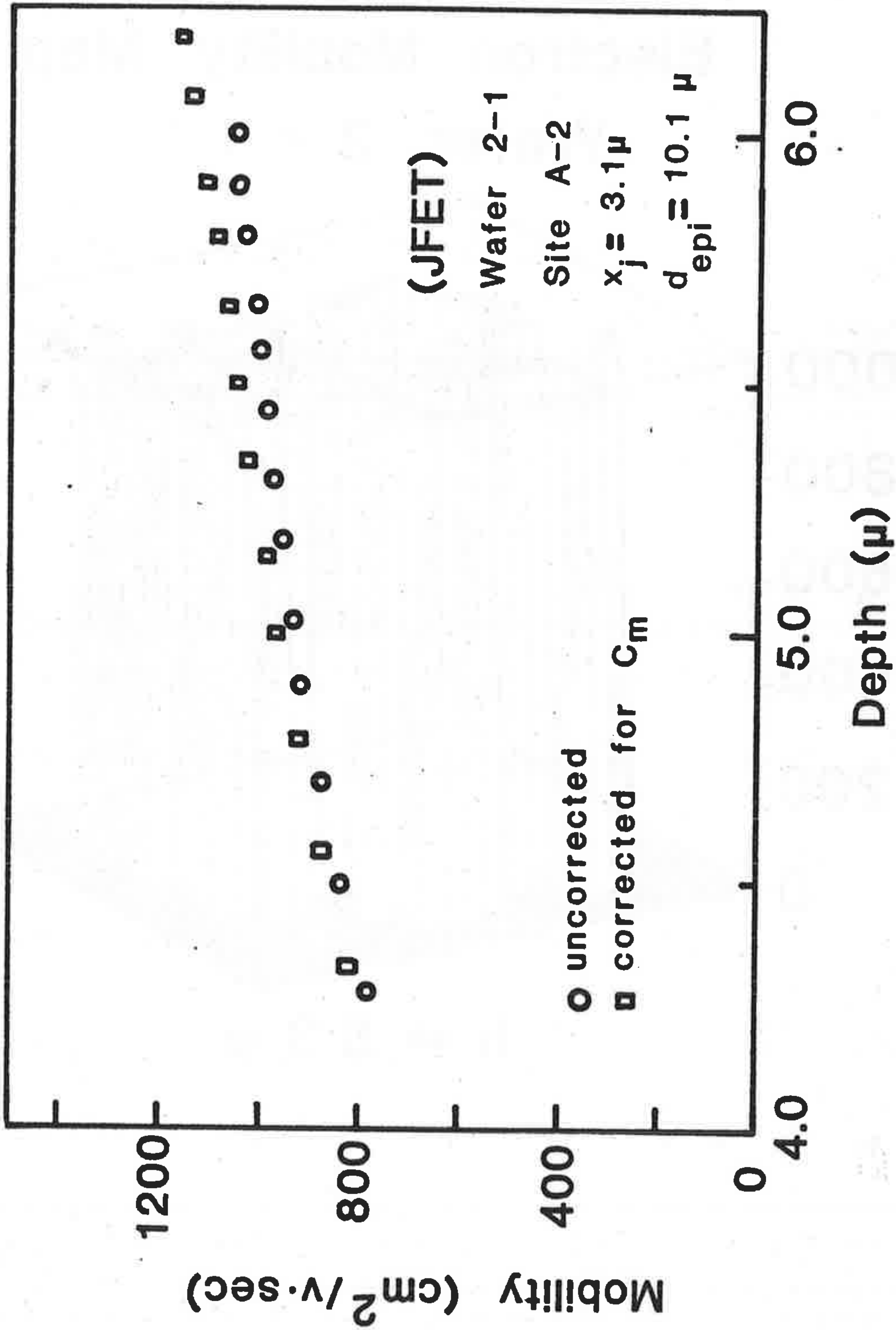
$$\frac{dG}{dh} = \frac{-qZn(h)\mu(h)}{L}$$

$$n(h) = \frac{-C_G}{LZq}\left(\frac{dh}{dV_G}\right)^{-1}$$

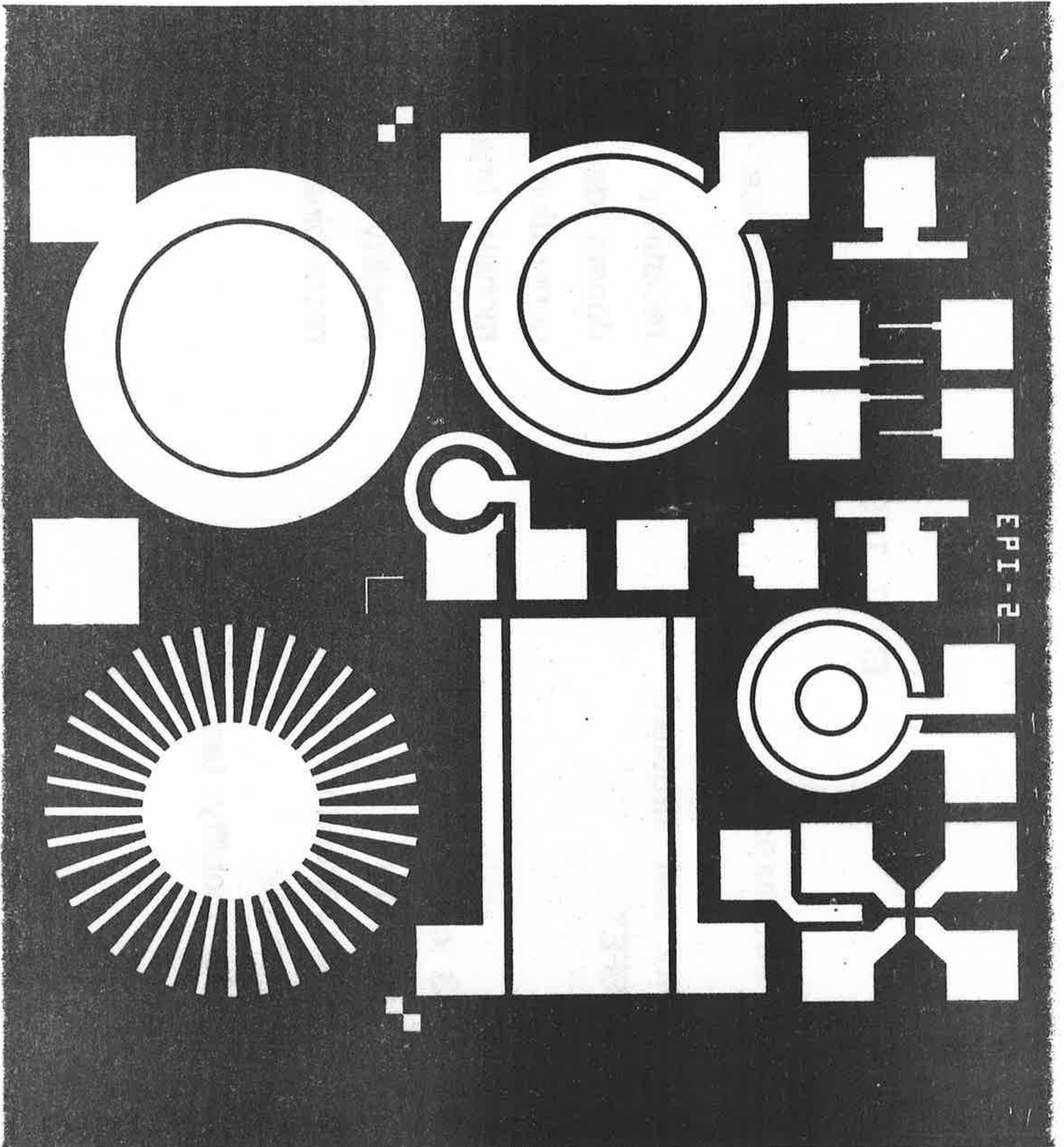
$$\mu_n(h) = \frac{L^2 g_{mo}}{C_G V_D}$$

[+] Hsu and Scott, RCA Review, 36, 1975, p240.


Electron Mobility Map
Wafer 2 - 1
Mobility (cm²/v·sec)
1000
800
600
400
200
0
h = 5.3 µ



Electron Mobility Profile
Mobility (cm²/v·sec)
0
400
800
1200
4.0
5.0
6.0
Depth (µ)
(JFET)
Wafer 2–1
Site A–2
x_j = 3.1µ
d_{epi} = 10.1 µ
uncorrected
corrected for C_m


EPI-2

EPI-2 TEST CHIP

Test Structures

- bulk resistivity test structure
- circular MOSFET
- gated diode
- JFET
- circular MOS capacitor
- ring MOS capacitor
- starburst MOS capacitor
- P-N junction diode
- minority carrier mobility test structure

Electrical Parameters

- resistivity
- dopant density
- generation lifetime
- mobility (majority carrier)
- diffusion length
- mobility (minority carrier)
- recombination lifetime

Layer to Layer Interconnections in VLSI Circuits

G. K. Reeves
Telecom Australia, Melbourne

H. B. Harrison and G. Sai-Halasz
Microelectronics Tech. Centre
RMIT, Melbourne
Australia

LAYER TO LAYER INTERCONNECTIONS IN VLSI CIRCUITS

G.K.Reeves – Telecom Aust.,Melb.

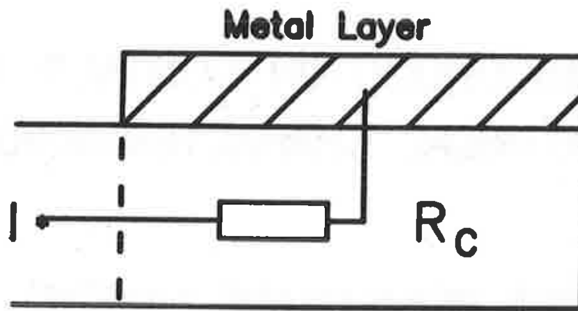
H.B.Harrison
G.Sai–Halasz
} Microelectronics Tech. Centre,RMIT,Melb. Australia.

—METAL—SEMICONDUCTOR CONTACT: MODEL
& ELECTRICAL CHARACTERIZATION

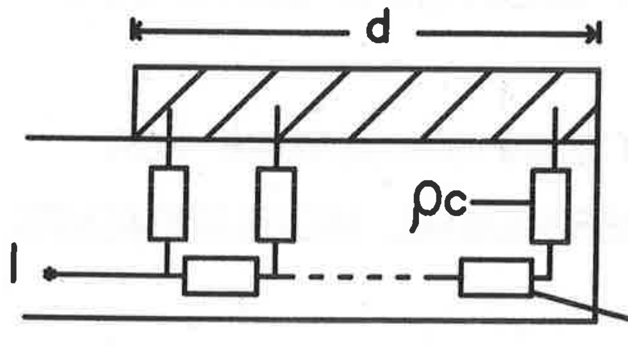
—FINITE SHEET RESISTANCE LAYERS: MODEL
& ELECTRICAL BEHAVIOUR

—TEST PATTERN STRUCTURE FOR
EXPERIMENTAL MEASUREMENTS

—RESULTS OF EXPERIMENTAL MEASUREMENTS



Contact Resistance Rc of a planar contact.



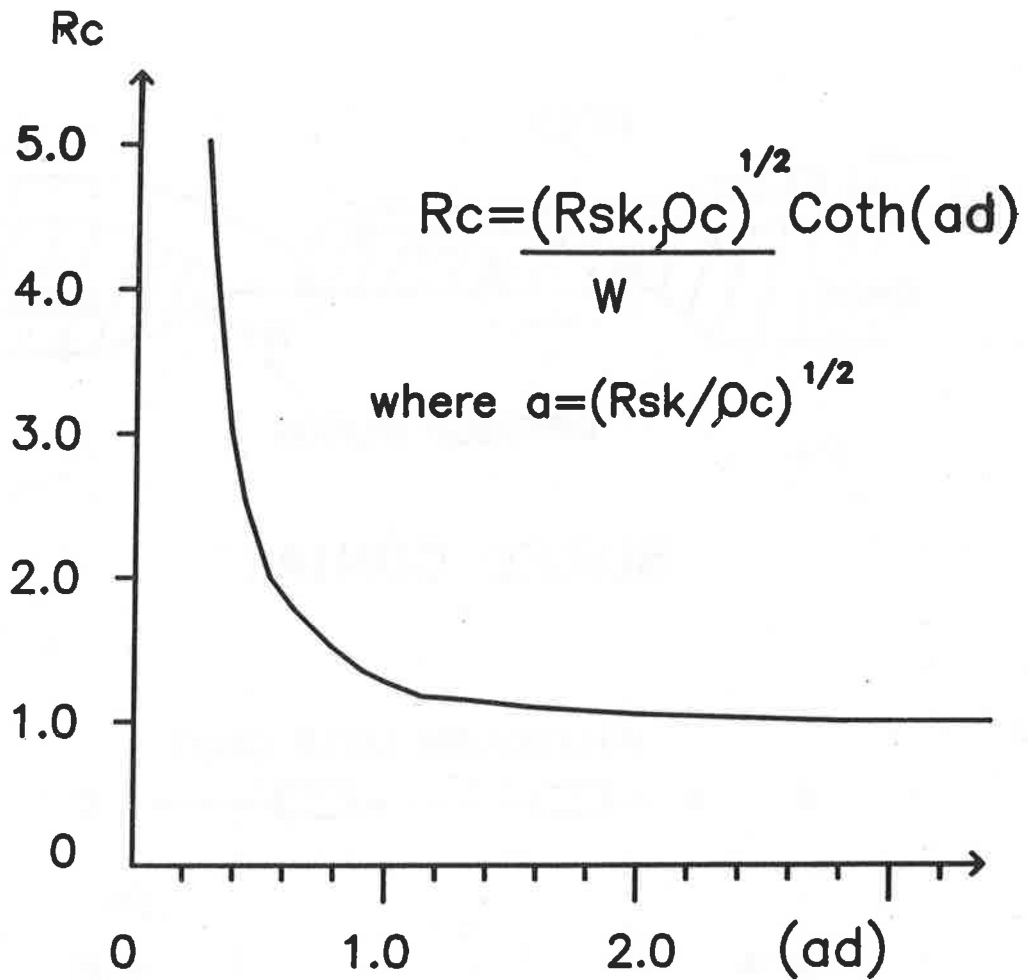
Electrical network for modelling planar ohmic contact.

Rsk.

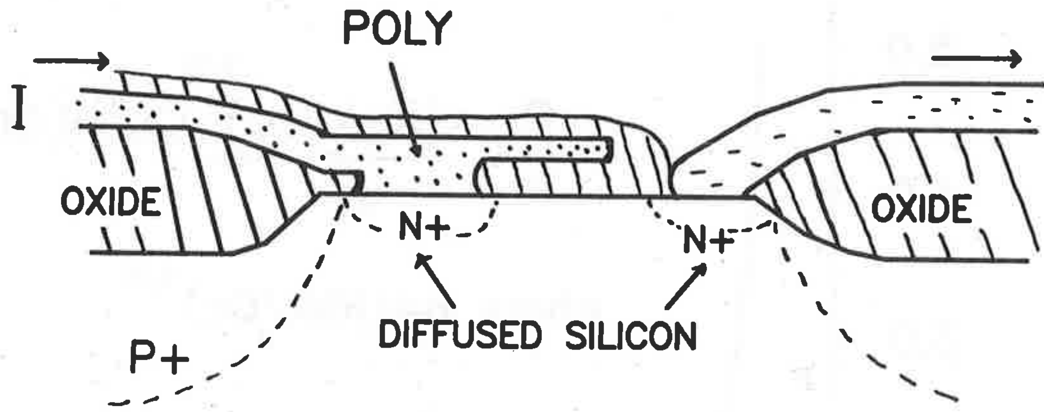
ρc= SPECIFIC CONTACT RESISTANCE (Ohm.cm^2)

Rsk= SHEET RESISTANCE UNDER CONTACT (Ohm/sq.)

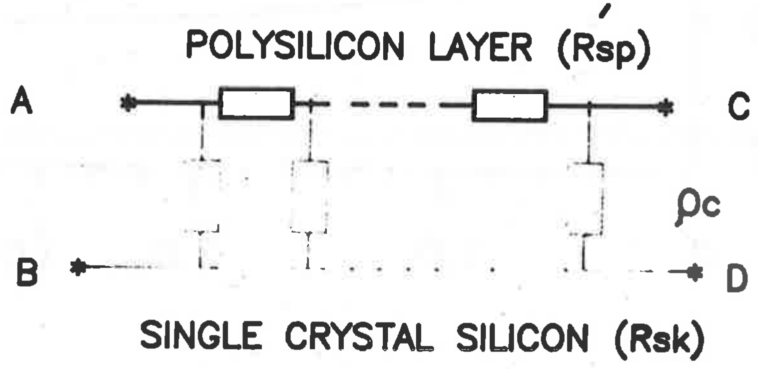
METAL–SEMICONDUCTOR OHMIC CONTACT



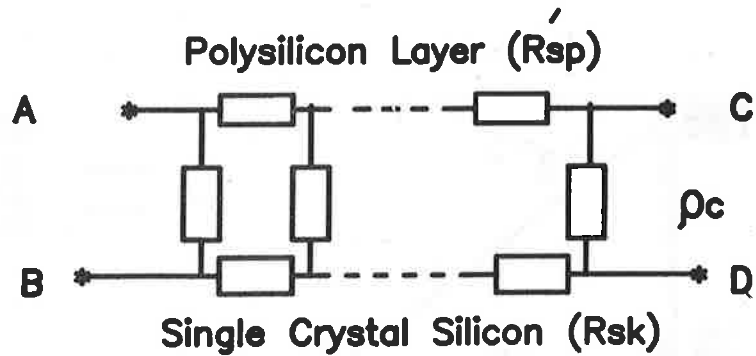
DEPENDENCE OF Rc ON CONTACT LENGTH d.



BURIED CONTACT



ELECTRICAL MODEL FOR BURIED CONTACT



Two definitions of Rc depending upon direction of current flow :

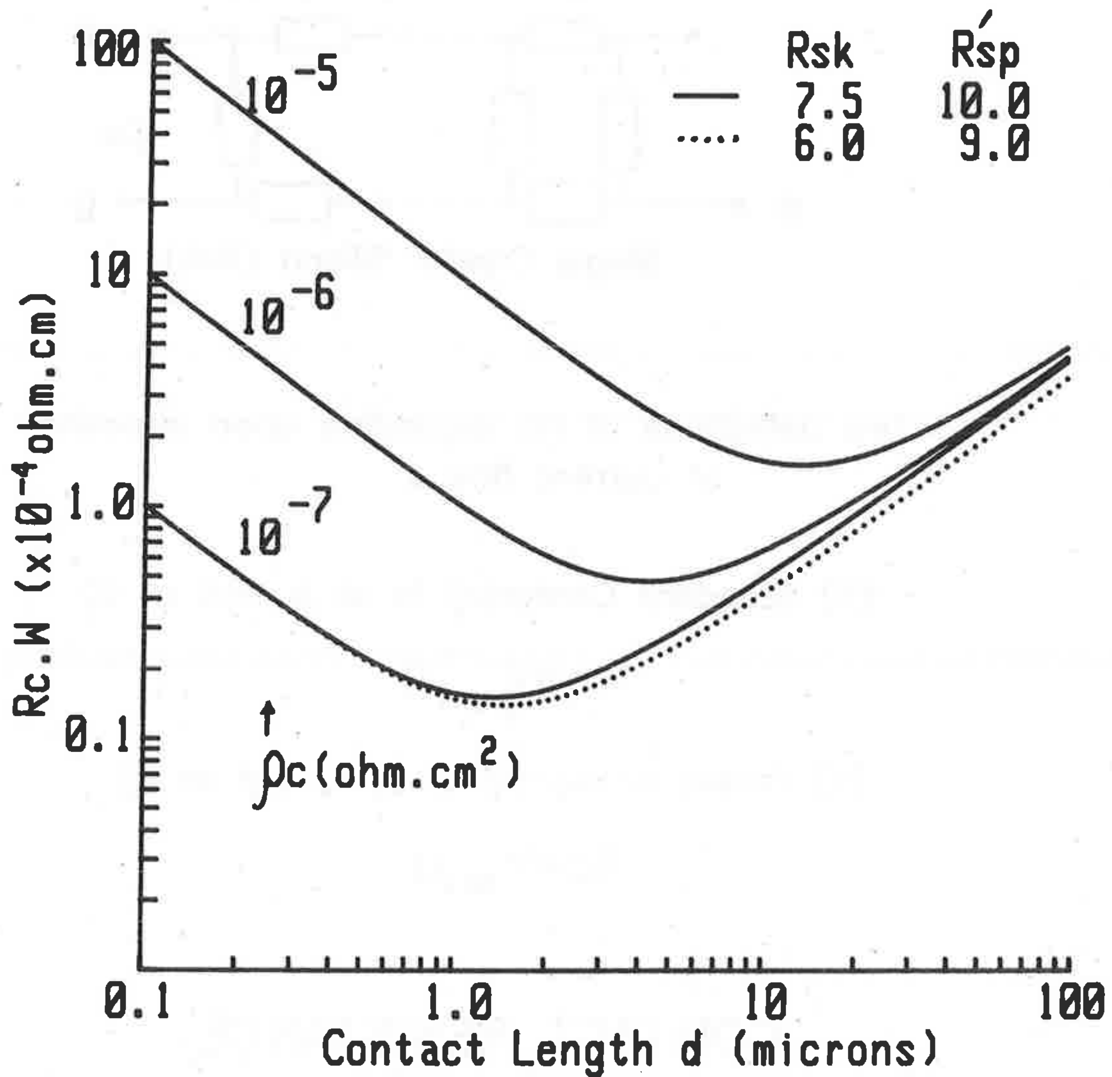
(1) Standard Contact:(I in at A, out at D)

$$Rc=V_{AD}/I$$

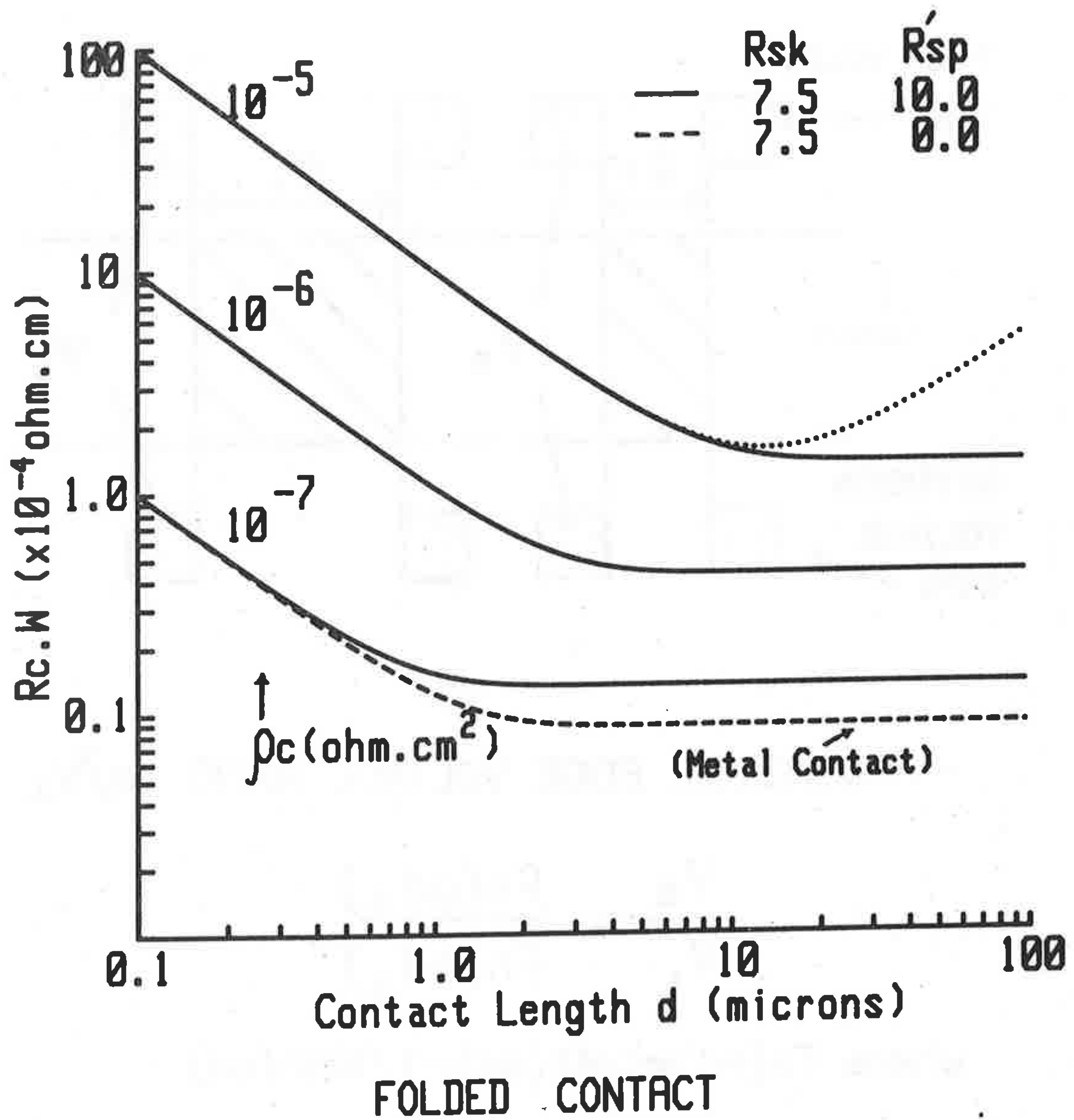
(2) Folded Contact:(I in at A, out at B)

$$Rc=V_{AB}/I$$

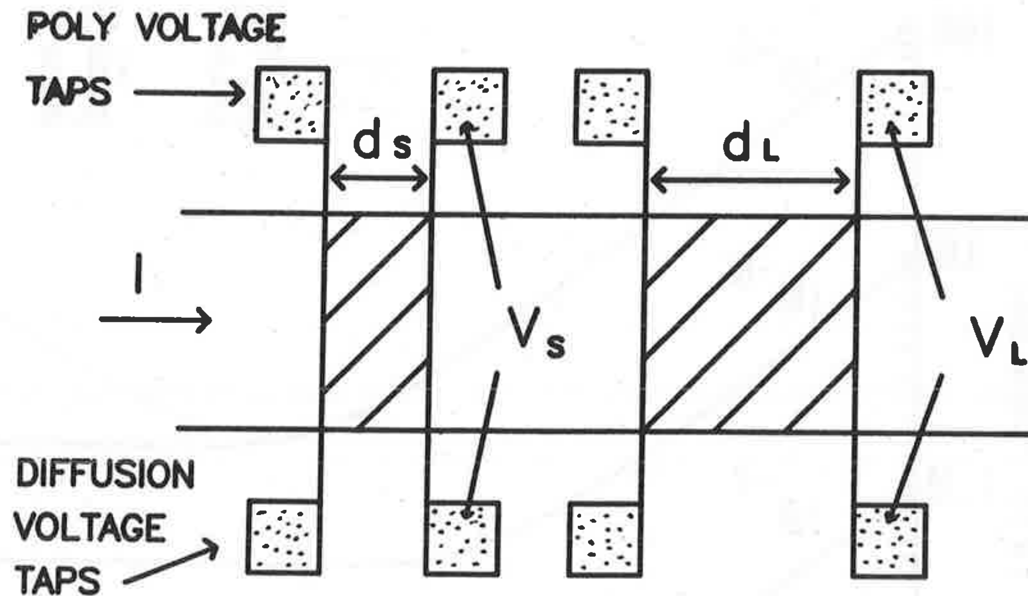
CONTACT RESISTANCE DEFINITIONS



STANDARD CONTACT



FOLDED CONTACT

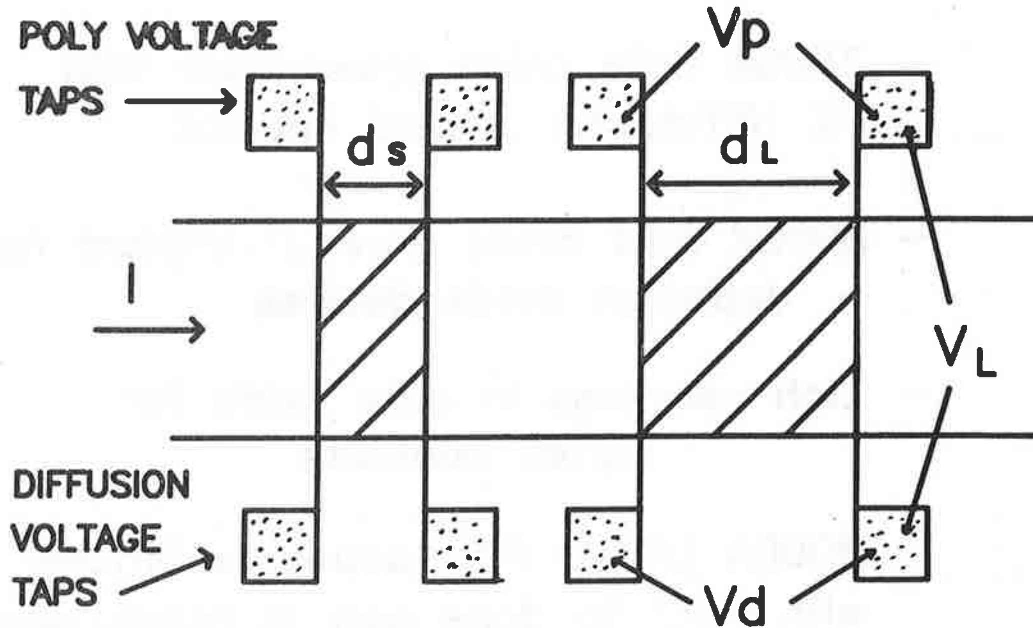


-- MEASURE EDGE VOLTAGE RATIO V_s/V_L

$$\frac{V_S}{V_L} = \frac{Fn(ad_s)}{Fn(ad_L)}$$

where $Fn(ad) = Coth(ad) - 1/Sinh(ad)$

THUS DETERMINE PARAMETER a



-- MEASURE $V_L/I \Longrightarrow R'_{sp}$

-- MEASURE POLY :DIFFUSION V. DROP

$$\frac{\text{POLY V.DROP}}{\text{DIFF. V.DROP}} \Longrightarrow \frac{R'_{sp}}{R_{sk}}$$

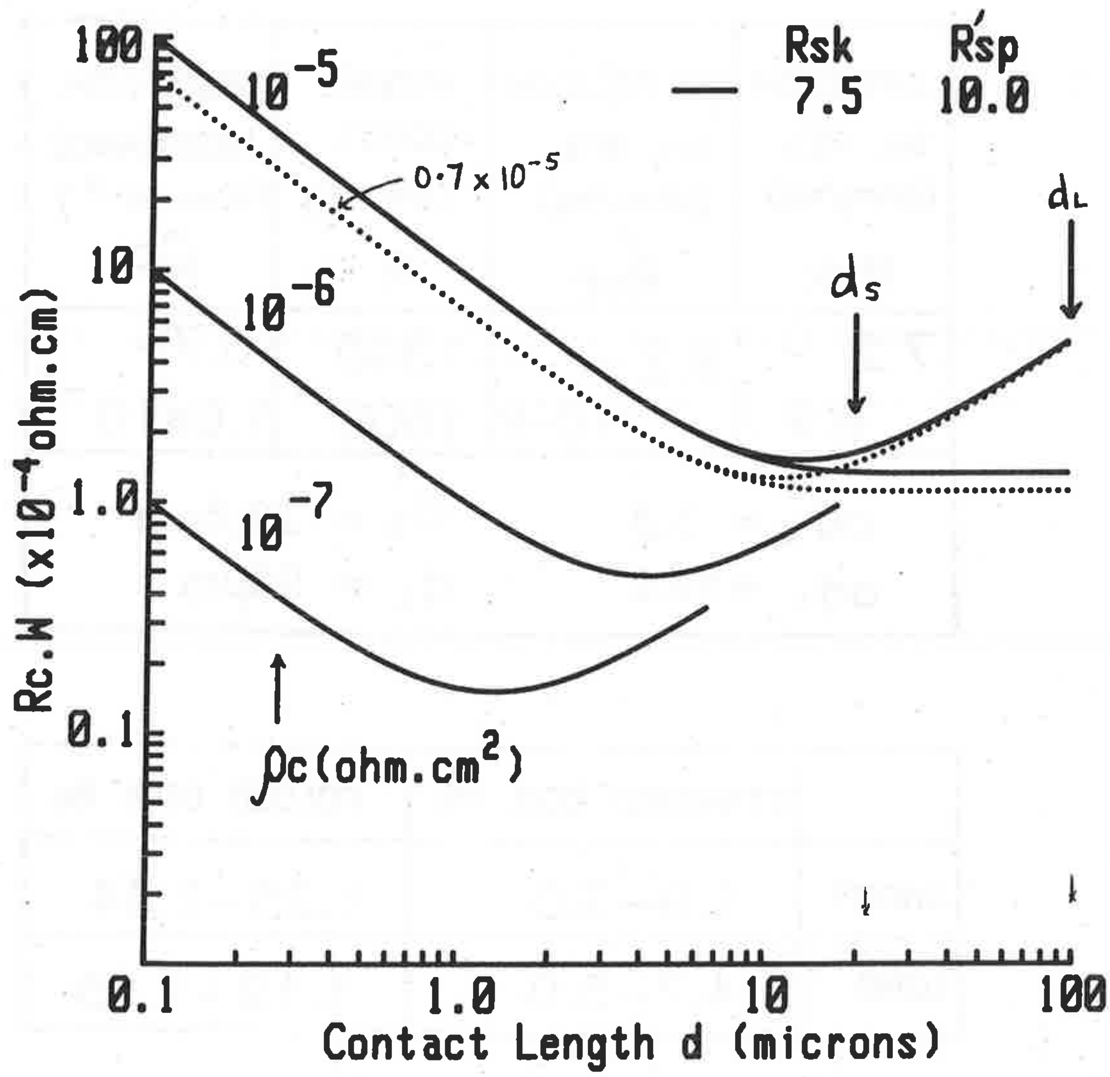
CALCULATE ρ_c: $\rho_c = (R'_{sp} + R_{sk}) / a^2$

- 1000A Gate oxide grown.Mask with Si Nitride for B field implant
- 8000A field oxide grown.P implant for depletion mode devices
- Etch openings in gate oxide for buried contacts
- 5000A LPCVD Poly deposited.Diffuse with POCl to dope poly & monoxtalline Si in buried contact regions
- Pattern polysilicon.Open gate oxide
- Diffuse monocrystalline silicon with POCl .Poly also diffused again
- Metal deposition & patterning. Deposit silox

CONTACT PARAMETERS

DIFFUSION SH. RES. (ohm/sq) R_{sk}	POLYSILICON SH. RES. (ohm/sq) R'_{sp}	ATTEN. CONST. (cm^{-1}) a	SPEC. CON. RESISTANCE ($ohm.cm^2$) ρ_c
7.2 – 8.9	9.2 – 10.4	1340 1600	0.7– 1.0×10^{-5}
$ad_s = 3.3$ $ad_L = 14.2$		$d_s = 22.5\mu m$ $d_L = 96\mu m$	

	STANDARD CON. Rc	FOLDED CON. Rc
SHORT	1.9–2.0	1.25–1.34
LONG	4.7–5.0	1.12–1.35



100
10
1.0
0.1
Rc.W (x10⁻⁴ohm.cm)
0.1
1.0
10
100
Contact Length d (microns)
Rsk
R'sp
7.5
10.0
10⁻⁵
0·7 x 10⁻⁵
10⁻⁶
10⁻⁷
ρc(ohm.cm²)
ds
dL

Isolation Test Structures for CMOS

John Y. Chen
Hughes Research Laboratories

ISOLATION TEST STRUCTURES FOR CMOS

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(213)-456-6411

CMOS is rapidly becoming a major VLSI technology due to its inherent low power characteristics. However, bulk CMOS has poorer packing density than does NMOS because a larger layout area is generally required to isolate p- and n-channel devices. These device types are physically isolated by at least one well in the substrate. Conventionally, the well is formed by diffusion process which requires a large layout area. High energy implantation has recently been employed to form the CMOS well which greatly reduces the spacing between the two devices[1]. Consequently, CMOS layout area may not be limited by the physical well dimension, but restricted by the electrical isolation.

Electrical isolation is a major concern in CMOS circuit layouts. In a CMOS IC, the gate of a p-channel FET is often connected to the gate of an n-channel FET to form logic components such inverters. Fig. 1a shown the layout of an inverter cell. The cross section of the cell along AB is shown in Fig.1b. This cross section is perpendicular to the direction of the current in the FETs. The two FETs are normally separately by a relatively thick field oxide. If the gate is biased at 5 V, the p-surface within the n-active area(indicated as the cross-hatched area in Fig. 1b) is inverted to n-type, but is isolated from the n-substrate if the p-region under the field oxide(shown as p-CS) is not inverted. This region is normally doped heavily to form a channel stop which prevents field inversion. When the gate bias is switched to 0 V, the p-device is then turned on but is isolated from the p-well by the n-region under the field oxide. An n-type channel stop may also be used for this region to avoid field inversion. As the width of the channel stop(L_F is Fig. 1) is reduced, field inversion may occur prematurely due to lateral diffusion of the channel stop(s) and two-dimensional fringing field effect at the edges of the active devices. It is therefore necessary to derive a design rule for the minimum layout spacing which is required to electrically isolate the two opposite type devices in a CMOS.

We have developed a new test structure which is suitable in obtaining these isolation design rules for a given CMOS technology. This test structure is used to measure the field

inversion voltage and the field subthreshold characteristics as a function of isolation spacing. Fig. 2a shows the cross section of the test structure which tests isolation characteristics for an n-device. Quadruple-well CMOS technology[2] is used here as an example. Notice both source and drain are formed by n^+ junctions to allow this structure operate as an n-channel MOSFET. As the gate voltage increases, the p-well surface under the thin oxide inverts first(at $V_g \approx 0.5$ V), however current does not flow until the V_g is high enough to invert the p-type channel stop. I-V_g in the channel stop region can then be measured and the field inversion voltage can be determined. A similar structure for testing p-device isolation is shown in Fig. 2b. Notice that both source and drain junctions are P^+ for this structure and the gate and the drain are now biased at negative voltages. Layout plots of a series of these test structures with various isolation spacings(L_F) are shown in Fig.3a and 3b for n- and p-device isolation respectively.

Experimental results have been obtained from the test structures fabricated by quadruple-well CMOS technology. Fig. 4a and 4b show the subthreshold I-V_g characteristics measured from the test structures shown in Fig. 3a and 3b respectively. L_F is the design rule for the isolation(or channel stop) distance shown in Fig. 3. At 2 μm design rule(L_F = 2 μm), the subthreshold leakage currents in the isolation region between the two opposite type devices are < 1 pA when V_g is biased between -16.5 V and 20 V. The field inversion voltages (defined at 1 μA) as a function of L_F are shown in Fig.5 for the n- and p-channel devices. Notice that the magnitude of the field inversion voltage($|V_{TF}|$) decreases as L_F is scaled down. However, $|V_{TF}|$ still maintains above 20 V at L_F = 2 μm for both type devices. Such experimental results verify the validity of these new test structures. Using these structures, one can derive the isolation layout rules for any bulk CMOS technology.

REFERENCES:

1. R.D. Rung, C.J. Dell'Oca and L.G. Walker, " A retrograde p-well for high density CMOS," IEEE Trans. on Ele. Dev., vol.ED-28, p1115, 1981.

2. J.Y. Chen, " Quadruple-well CMOS - A VLSI technology," IEDM Digest, p.791, 1982.

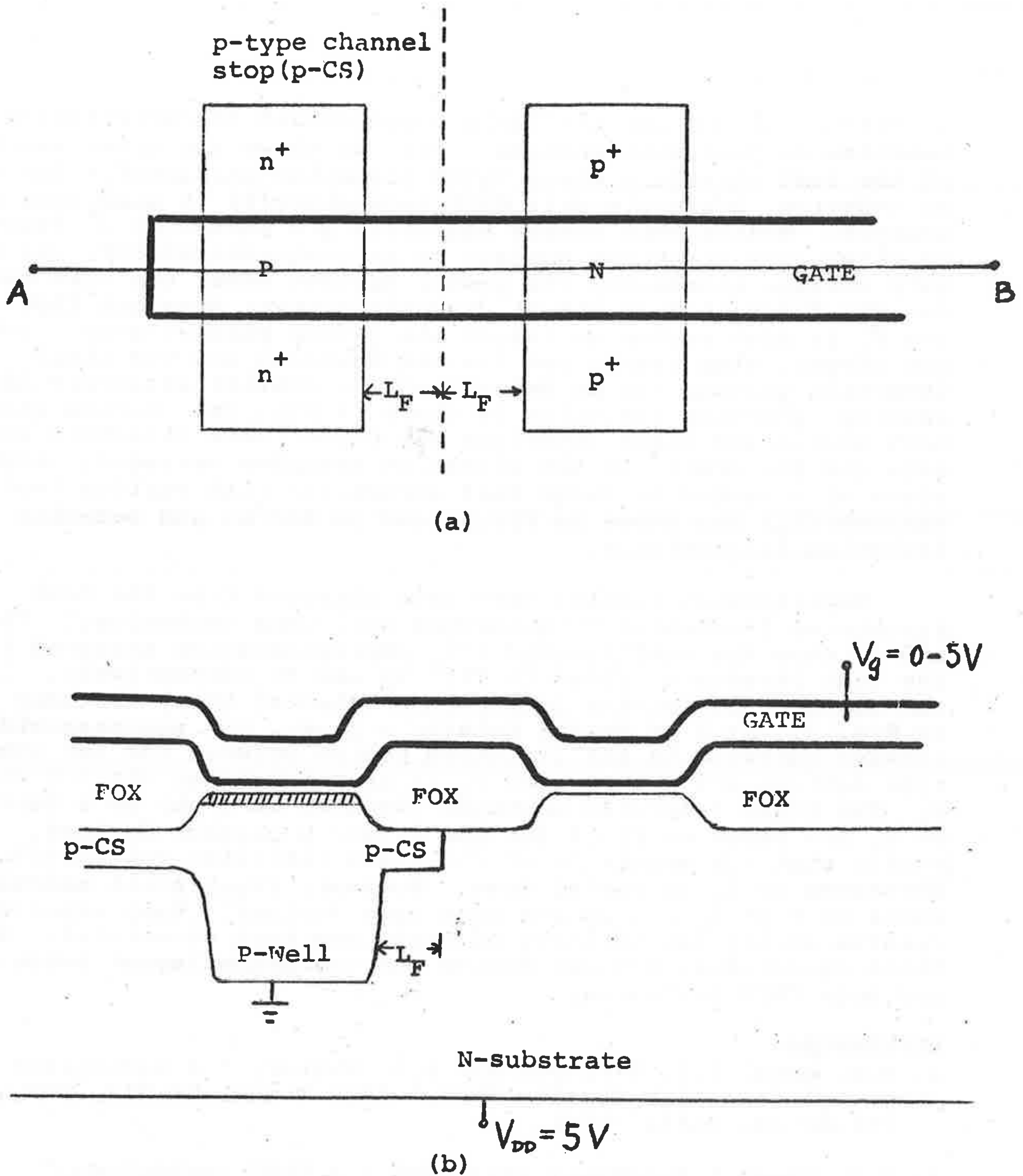
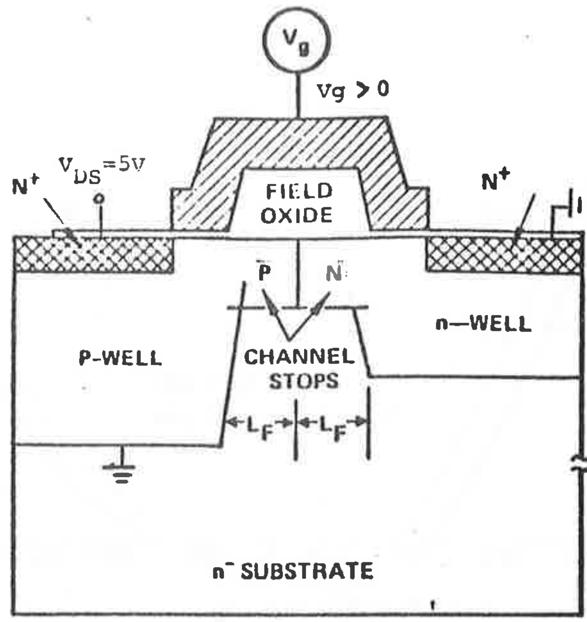
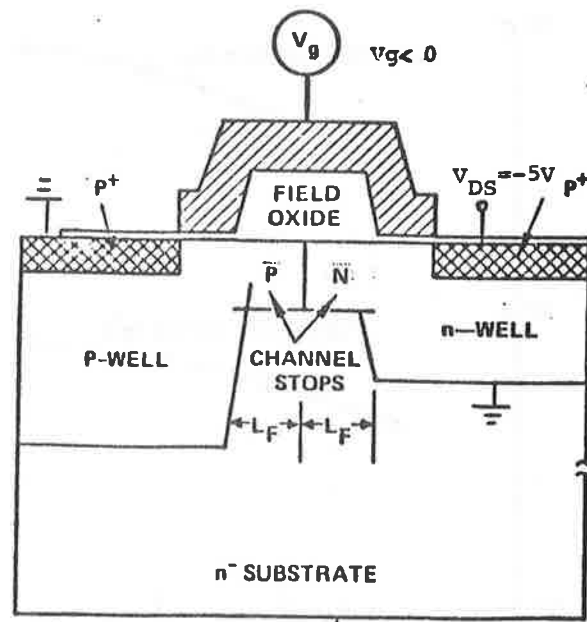


Fig.1 A schematic showing isolation problem between an n- and a p-channel FET; (a) layout view, (b) cross-section view. A conventional p-well CMOS is used here to illustrate the problem.



(a)



(b)

Fig.2 Cross sections of the test structures for (a) n- and (b) p-device isolation

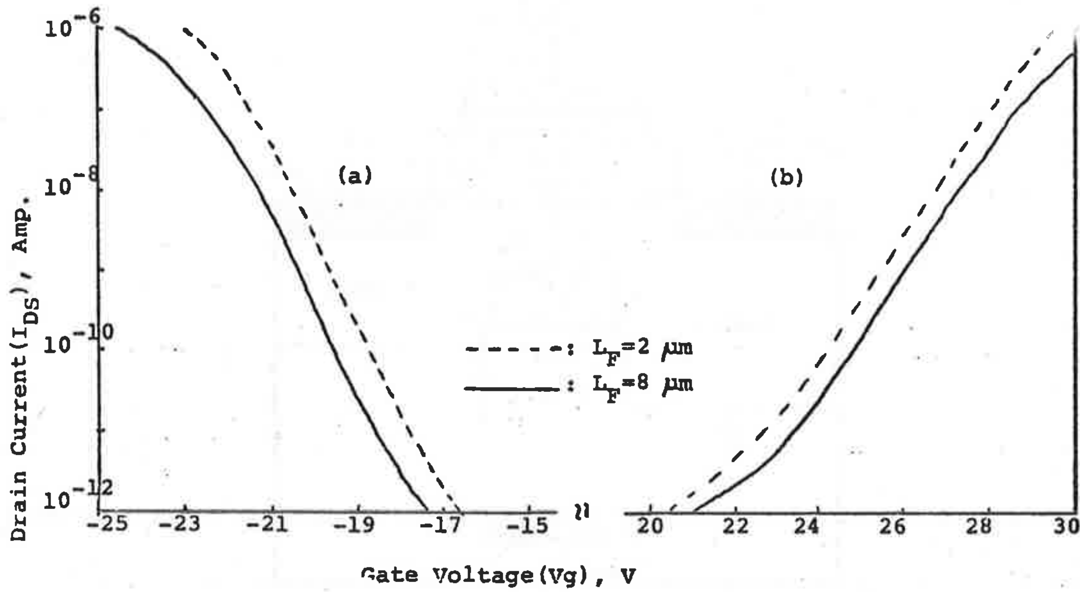


Fig. 4 Subthreshold currents measured from (a) n- and (b) p-channel isolation test structures.

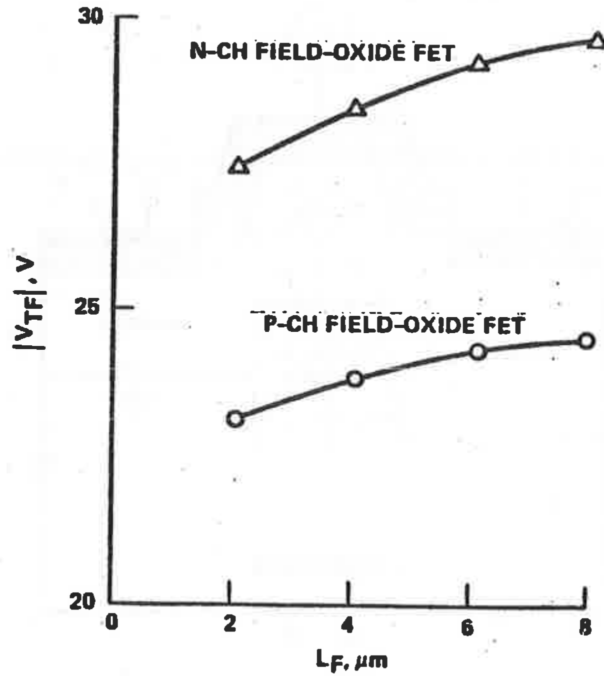


Fig. 5 Field inversion voltages as a function of isolation spacing. $|V_{TF}|$ is the magnitude of the field inversion voltage, L_F is the isolation(or channel stop) dimension.

SESSION II TEST STRUCTURE UTILIZATION

Test Device for CMOS/SOS Parameter Testing

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Microelectronics Research and Development Center
Rockwell International Corporation

OUTLINE

- TEST DEVICE REQUIREMENTS
- DESCRIPTION OF TEST STRUCTURES
- CRITICAL DEVICE PARAMETERS
- AUTOMATIC PARAMETRIC TEST SYSTEM
- DATA PRESENTATION

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TEST DEVICE

- **COMPACT**
- **MINIMUM NUMBER OF PADS**
- **SIMPLE, REVISABLE DESIGN AND LAYOUT STRATEGY**
- **STANDARD DIMENSIONS AND PAD CONFIGURATION**
  - TEST AND DATA ANALYSIS ROUTINES STANDARDIZED
- **APPLICATION:**
  - EVALUATE PROCESS GEOMETRIC AND ELECTRICAL PARAMETERS RELATED TO CIRCUIT SPECIFICATIONS
  - FLAG PROCESS PROBLEMS/ANOMALIES

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TD18-1

610 μm

305 μm

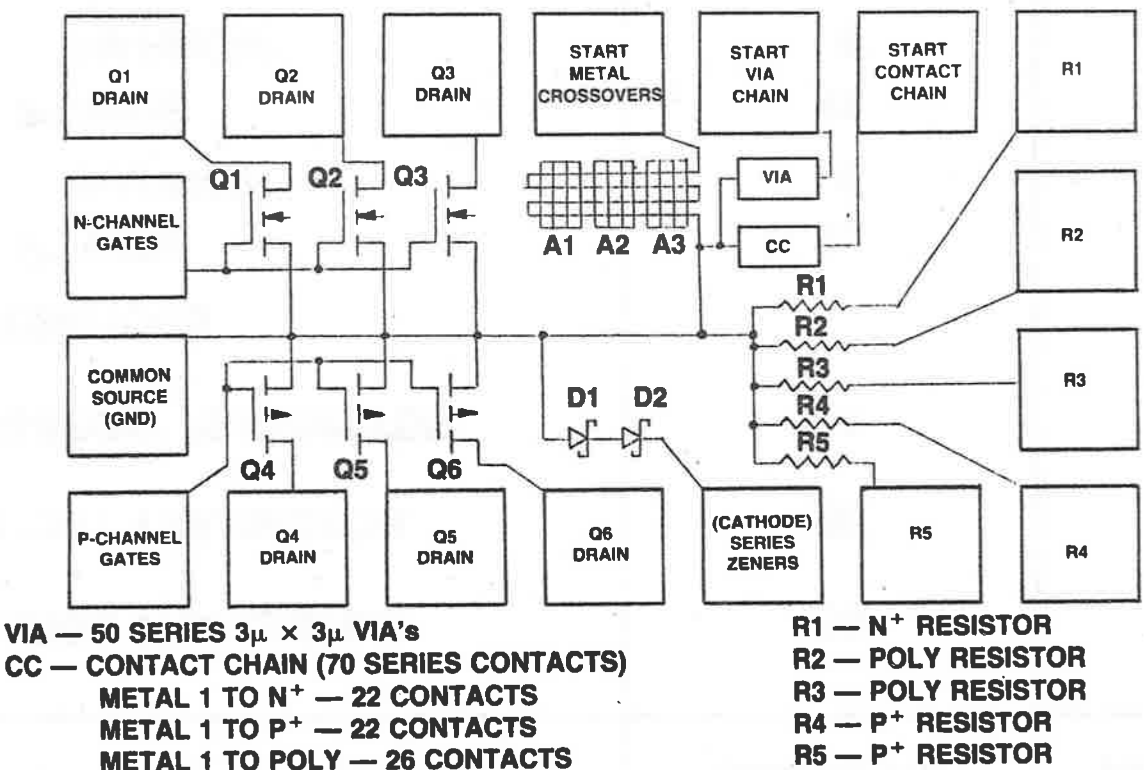
Q1 LARGE (UNIT) NFET
Q2 NARROW (LONG) NFET
Q3 SHORT (WIDE) NFET
Q4 LARGE (UNIT) PFET
Q5 NARROW (LONG) PFET
Q6 SHORT (WIDE) PFET

D1 INPUT PROTECT DIODE

R1 n^+ SQUARE RESISTOR
R2 n^+ WIDE RESISTOR
R3 n^+ NARROW RESISTOR
R4 POLY NARROW RESISTOR
R5 POLY WIDE RESISTOR
R6 p^+ NARROW RESISTOR
R7 p^+ WIDE RESISTOR

A1 POLY
A2 n^+
A3 p^+
} METAL LINE 48 CROSS OVERS (16 EACH)

TD18-2



TD18 TEST STRUCTURES DIMENSIONS

TEST STRUCTURE	W (MICRONS)	L (MICRONS)
LARGE TRANSISTOR	60	56
SHORT TRANSISTOR	60	2
NARROW TRANSISTOR	6	26
RESISTORS		
N^+ WIDE	18	260
NARROW	6	260
P^+ WIDE	18	260
NARROW	6	260
POLY WIDE	15	278
NARROW	3	278
DIODE JUNCT. WIDTH	290	—

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MEASURED DEVICE PARAMETERS

DEVICE TYPE	PARAMETER	SYMBOL	CONDITIONS
TRANSISTORS NFET, PFET	THRESHOLD VOLTAGE	VT	VDD = 100 mV (SHOWN FOR N-FEET)
	TRANSISTOR GAIN (K')	KP	VDD = 100 mV (SHOWN FOR N-FEET)
	D/S LEAKAGE CURRENT	ILD	VDS = 5V, VGS = 0, −5V
	D/S BREAKDOWN VOLTAGE	BVDSS	IDS = 10μA, VGS = 0
	GATE LEAKAGE CURRENT	ILG	VGS = ±10V
	DRAIN SATURATION CURRENT	IDS	VDS = 5V, VGS = 5V
N^+, P^+, POLY RESISTORS	RESISTANCE		AT 1mA
DIODE	REVERSE LEAKAGE CURRENT	ILR	VR = 10V
	REVERSE BREAKDOWN VOLTAGE	BVR	IR = 10μA
	FORWARD VOLTAGE	VF	IF = 10μA, 1mA
METAL CROSSOVER	RESISTANCE CONTINUITY		AT 10mA
CONTACT CHAIN	RESISTANCE CONTINUITY		AT 0.1mA

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DERIVED DEVICE PARAMETERS

DEVICE	PARAMETER	SYMBOL	EQUATIONS
TRANSISTORS	EFFECTIVE LENGTH	LEFF	$LEFF = (L_L - L_S) \frac{K_L * W_S}{K_S{*}W_L - K_L{*}W_S}$
	DELTA WIDTH	DW	$WEFF = (W_L - W_N) \frac{K_N * L_N}{K_L{*}L_L - K_N{*}L_N}$ $DW = WEFF - W_N$ WHERE: L_L, L_S, L_N = DESIGN LENGTH W_L, W_S, W_N = DESIGN WIDTHS K_L, K_S, K_N = MAXIMUM SLOPE FACTORS FROM MEASURED CONDUCTANCE CURVES ID VERSUS VGS AT VDS = 0.1V SUBSCRIPT L, S, N INDICATE LARGE, SHORT, NARROW DEVICES
	MOBILITY	UFE	$UFE = \frac{2{*}KP}{COX}$
	OUTPUT RESISTANCE	RON	RON = VDS/ID (VDS = 0.1V, VGS = 5V)
RESISTORS	SHEET RESISTANCE	RS	$RS = R_1 \frac{W_1 + DWR}{L}$
	DELTA WIDTH	DWR	$DWR = \frac{(R_1/R_2)\,W_1 - W_2}{1 - (R_1/R_2)}$ WHERE: $R_1 < R_2$ MEASURED RESISTANCE $W_1 > W_2$ DESIGN WIDTHS L DESIGN LENGTH

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DEVICE PARAMETER CHARACTERIZATION SYSTEM

TEKTRONIX 4632 HARD COPY UNIT

HP2648 GRAPHICS TERMINAL

HP2645A TERMINAL

HP2645A TERMINAL

HP1000 — F
RTE-IVB O/S
512 KBYTES

HP7925M DISC DRIVE 125 MBYTES

DATA PRINTER 600 LPM

HP7970B MAGTAPE

MEASUREMENT SYSTEM

- PACIFIC WESTERN PROBE
- RELAY MATRIX
- HP34740A DMM
- KEITHLEY 419 PICOAMMETER
- 2 PROG POWER SUPPLIES (PPS)
- DONNER DPS-50 PPS

2 KEITHLEY 200 CURRENT SOURCES
3 KEITHLEY 230 VOLTAGE SOURCES
KEITHLEY 619 ELECTROMETER
HP-4275A LCR METER

DATA PRESENTATION

- TABULAR AND STATISTICAL SUMMARY WAFER PRINTOUT
- WAFER MAP PRINTOUT
- CONTROL CHARTS
- LOT SUMMARY TABLE
- TREND CHARTS
- SCATTER PLOTS
- TEMPERATURE COEFFICIENT CHARTS

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TABULAR PRINTOUT EXAMPLE

TD18S AAMP   LOT.WAFER 366.07   5/19/83

OXIDE THICKNESS (ANG) = 514.0

TRANSISTORS

LARGE W,L (UM)	= 60.00	55.00
SHORT W,L (UM)	= 60.00	2.00
NARROW W,L (UM)	= 5.00	56.00

RESISTORS

N+,P+

WIDE W (UM)	= 18.00
NARROW W (UM)	= 6.00
LENGTH L (UM)	=261.00

POLY

WIDE W (UM)	= 15.00
NARROW W (UM)	= 3.00
LENGTH L (UM)	=282.00

DIE POSITION

	(1, 1)	(1, 2)	(1, 3)	(1, 4)	(1, 5)
METAL CONTINUITY 10MA(OHMS)	12.626	11.583	11.981	11.758	12.032
N+ RESISTANCE (OHM/SQ)	51.50	50.54	51.55	56.61	55.92
P+ RESISTANCE (OHM/SQ)	97.36	56.86	97.94	98.43	97.47
POLY RESISTANCE (OHM/SQ)	4.47	4.66	4.39	4.59	4.59
P+ DELTA W (MICRON)	.26E+00	.29E-01	.16E+00	.21E+00	.35E-01
POLY DELTA W (MICRON)	.12E+00	.19E+00	.87E-01	.21E+00	.19E+00
NFET ILG VG=+/-10V (AMP)	-.49E-11	-.17E-10	-.15E-10	-.11E-10	-.38E-11
ILD L VG= 0 (AMP/UM)	.11E-10	.15E-10	.15E-10	.17E-10	.26E-10
ILD L VG=-5 (AMP/UM)	.58E-11	.84E-11	.83E-09	.69E-11	.96E-11
BVDSS L ID= 10UA(VOLT)	19.17	20.40	19.25	18.41	20.33
ILD S VG= 0 (AMP/UM)	.80E-09	.61E-09	.43E-09	.49E-09	.13E-08
ILD S VG=-5 (AMP/UM)	.78E-10	.17E-09	.59E-10	.12E-09	.20E-09
BVDSS S ID= 10UA(VOLT)	13.28	14.56	14.01	13.50	14.59
VDD = .1 VOLT					
VTHL (VOLT)	1.06	1.18	1.12	1.05	1.08
VTHS (VOLT)	.74	.97	.79	.73	.80
VTHN (VOLT)	1.13	1.41*	1.18	1.10	1.16
UFE (SQ CM/V-SEC)	434.42	417.00	436.63	442.47	434.70
L EFF (MICRON)	1.77	1.56	1.86	1.83	1.86
CW (MICRON)	-.73*	.07	-.77*	-.78*	-.81*
KP (MHO/VOLT)	.15E-04	.14E-04	.15E-04	.15E-04	.15E-04
KS (MHO/VOLT)	.49E-03	.54E-03	.47E-03	.48E-03	.46E-03
KN (MHO/VOLT)	.14E-05	.15E-05	.14E-05	.14E-05	.14E-05
RON L VG= 5 (OHM)	.94E+04	.98E+04	.96E+04	.93E+04	.95E+04
RON S VG= 5 (OHM)	.31E+03	.30E+03	.31E+03	.33E+03	.31E+03
RON N VG= 5 (OHM)	.10E+06	.10E+06	.10E+06	.99E+05	.10E+06
ISAT L VG=VDD= 5 (AMP)	.21E-03	.20E-03	.20E-03	.21E-03	.21E-03
ISAT S VG=VDD= 5 (AMP)	.51E-02	.50E-02	.50E-02	.51E-02	.50E-02

WAFER SUMMARY PRINTOUT EXAMPLE

DATA SUMMARY

Parameter	Units	N	AVG	S.D.	MIN	MAX
METAL CONTINUITY 10MA	(OHMS)					
N+ RESISTANCE	(OHM/SQ)	5	53.22	2.82	50.54	56.61
P+ RESISTANCE	(OHM/SQ)	5	97.61	.59	96.86	98.43
POLY RESISTANCE	(OHM/SQ)	5	4.54	.11	4.39	4.66
P+ DELTA W	(MICRON)	5	.14	.10	.03	.26
POLY DELTA W	(MICRON)	5	.16	.05	.09	.21
NFET LOG ILG VG=+/-10V	(AMP)	5	-11.05	.29	-11.42	-10.77
LOG ILD L VG= 0	(AMP/UM)	5	-10.79	.13	-10.95	-10.58
LOG ILD L VG=-5	(AMP/UM)	5	-10.72	.92	-11.24	-9.08
BVDSS L ID= 10UA	(VOLT)	5	19.51	.84	18.41	20.40
LOG ILD S VG= 0	(AMP/UM)	5	-9.17	.20	-9.37	-8.88
LOG ILD S VG=-5	(AMP/UM)	5	-9.94	.22	-10.23	-9.70
BVDSS S ID= 10UA	(VOLT)	5	13.59	.60	13.28	14.59
VDD = .1 VOLT						
VTHL	(VOLT)	5	1.10	.05	1.05	1.18
VTHS	(VOLT)	5	.81	.10	.73	.97
VTHN	(VOLT)	5	1.20	.12	1.10	1.41
UFE	(SQ CM/V-SEC)	5	433.04	9.53	417.00	442.47
L EFF	(MICRON)	5	1.78	.13	1.56	1.86
DW	(MICRON)	5	-.61	.38	-.81	.07
KP	(MHO/VOLT)	5	.15E-04	.32E-05	.14E-04	.15E-04
KS	(MHO/VOLT)	5	.49E-03	.31E-04	.45E-03	.54E-03
KN	(MHO/VOLT)	5	.14E-05	.71E-07	.14E-05	.15E-05
RON L VG= 5	(OHM)	5	.95E+04	.17E+03	.93E+04	.98E+04
RON S VG= 5	(OHM)	5	.31E+03	.11E+02	.30E+03	.33E+03
RON N VG= 5	(OHM)	5	.10E+06	.11E+04	.99E+05	.10E+06
ISAT L VG=VDD= 5	(AMP)	5	.21E-03	.52E-05	.20E-03	.21E-03
ISAT S VG=VDD= 5	(AMP)	5	.50E-02	.71E-04	.50E-02	.51E-02

OVERALL LOT AVERAGE ($\overline{X}$):

$$\overline{X} = \frac{\sum_{i=1}^{k} n_i \mu_i}{N}$$

WHERE:

μ_i = AVERAGE OF THE ith WAFER

n_i = SAMPLE SIZE OF THE ith WAFER

k = NUMBER OF WAFERS

$N = \sum_{i=1}^{k} M_i$

OVERALL STANDARD DEVIATION (S)

$$S = \sqrt{\frac{\sum_{i=1}^{k} [(n_i - 1)\sigma_i^2 + n_i \mu_i^2] - N\overline{X}^2}{N - 1}}$$

WHERE:

σ_i = **STANDARD DEVIATION OF THE ith WAFER**

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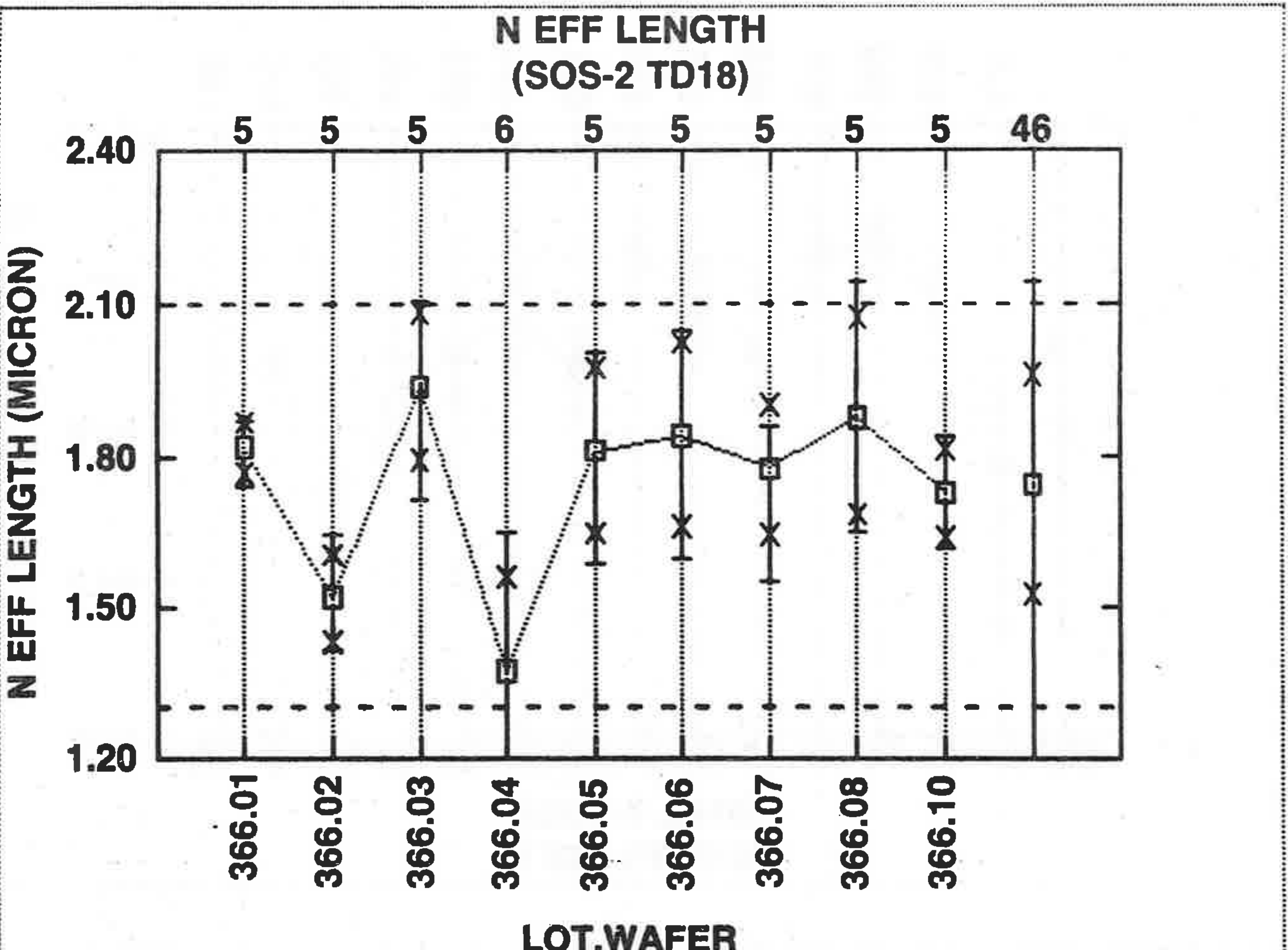
LOT SUMMARY DATA EXAMPLE

SUMMARY LOT A366 TD18S

K	PARAMETER	SPECIFICATION	AVERAGE	SD	N
17	P+RESISTANCE	<220 OHM/SQ	94.96	3.96	46
18	N+RESISTANCE	< 90 OHM/SQ	48.38	4.48	44
19	POLY RESISTANCE	< 30 OHM/SQ	4.77	.34	45
41	N GATE LEAKAGE	<-9 LOG AMP	-10.99	.42	45
45	N VBD (S)	> 8 VOLT	14.30	1.13	45
94	N IDL (S) VG=0V	<-8.00 LOG AMP/MICRON	-9.59	.45	46
95	N ISAT (S)	2 TO 10 m AMP	4.67	.41	46
50	N THRESHOLD (S)	0.7 TO 1.3 VOLT	.92	.16	46
52	N MOBILITY	>300 SQ CM/V-S	398.63	44.46	46
53	N EFF LENGTH	1.3 TO 2.1 MICRON	1.74	.22	46
55	N KP	9.4 TO 16.1 uMHO/VOLT	13.28	1.47	46
121	P GATE LEAKAGE	<-9 LOG AMP	-10.86	.37	46
125	P VBD (S)	<-8 VOLT	-19.42	.37	44
174	P IDL (S) VG=0V	<-8.00 LOG AMP/MICRON	-11.17	.26	45
175	P ISAT (S)	1 TO 5 m AMP	2.88	.23	46
130	P THRESHOLD (S)	-1.3 TO -0.7 VOLT	-.86	.07	45
132	P MOBILITY	>150 SQ CM/V-S	161.72	12.20	46
133	P EFF LENGTH	1.40 TO 2.20 MICRON	1.56	.13	45
135	P KP	4.7 TO 8.1 uMHO/VOLT	5.39	.40	46

CONTROL CHART EXAMPLE

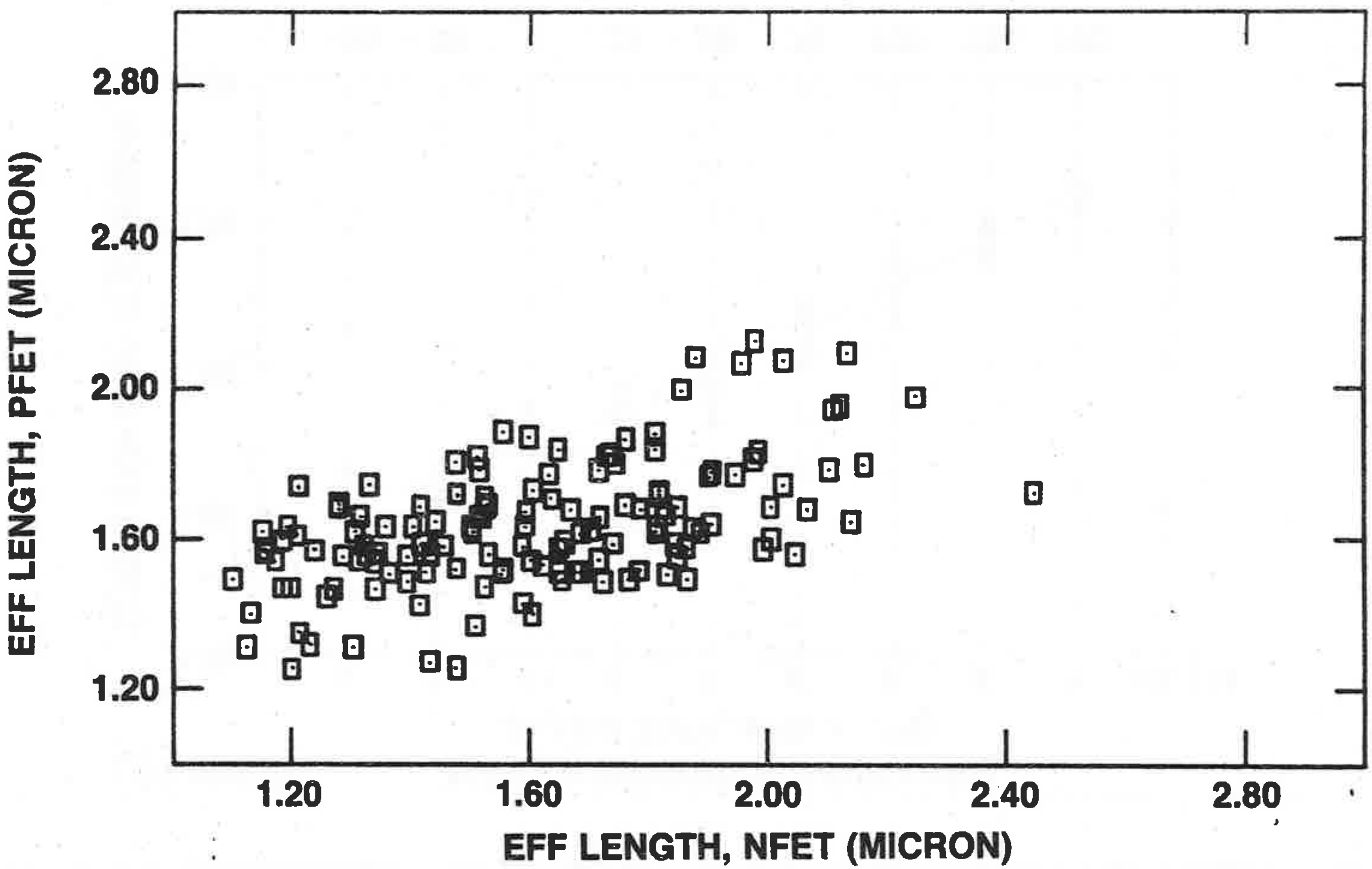


Rockwell International

TREND CHART EXAMPLE

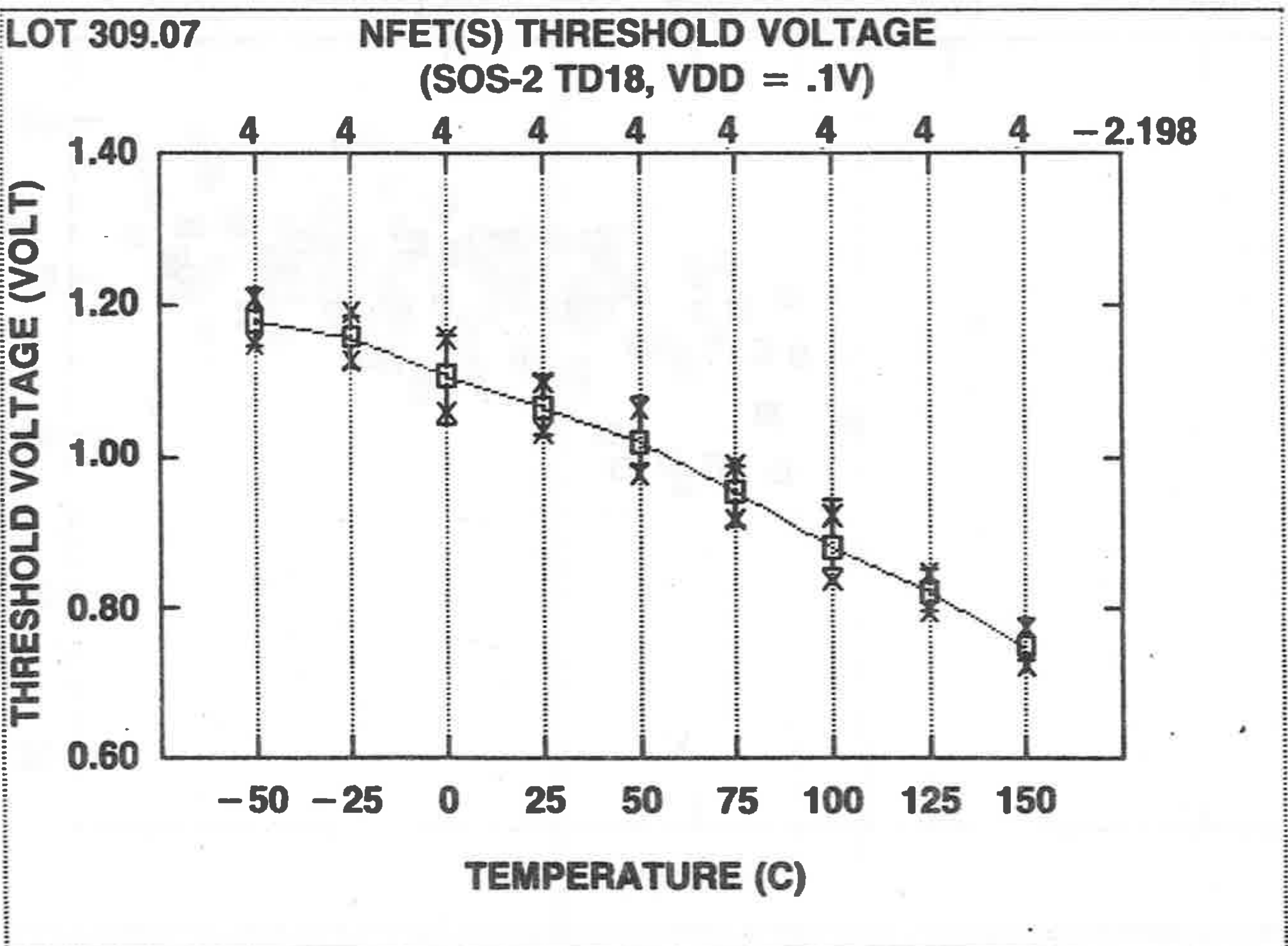
Rockwell International

SCATTER PLOT EXAMPLE



Rockwell International

TEMPERATURE COEFFICIENT PLOT EXAMPLE



Rockwell International

GRAPHICAL DISPLAYS INDISPENSABLE TOOL TO:

- DETERMINE BEST ESTIMATE FOR A DEVICE PARAMETER WITH A SPECIFIC PROCESS
- ESTIMATE THE SCATTER ASSOCIATED WITH A PROCESS
- INDICATE THE REPRODUCIBILITY OF THE PROCESS

Rockwell International

FLAG PROBLEMS/ANOMALIES

CONTACT PROBLEM

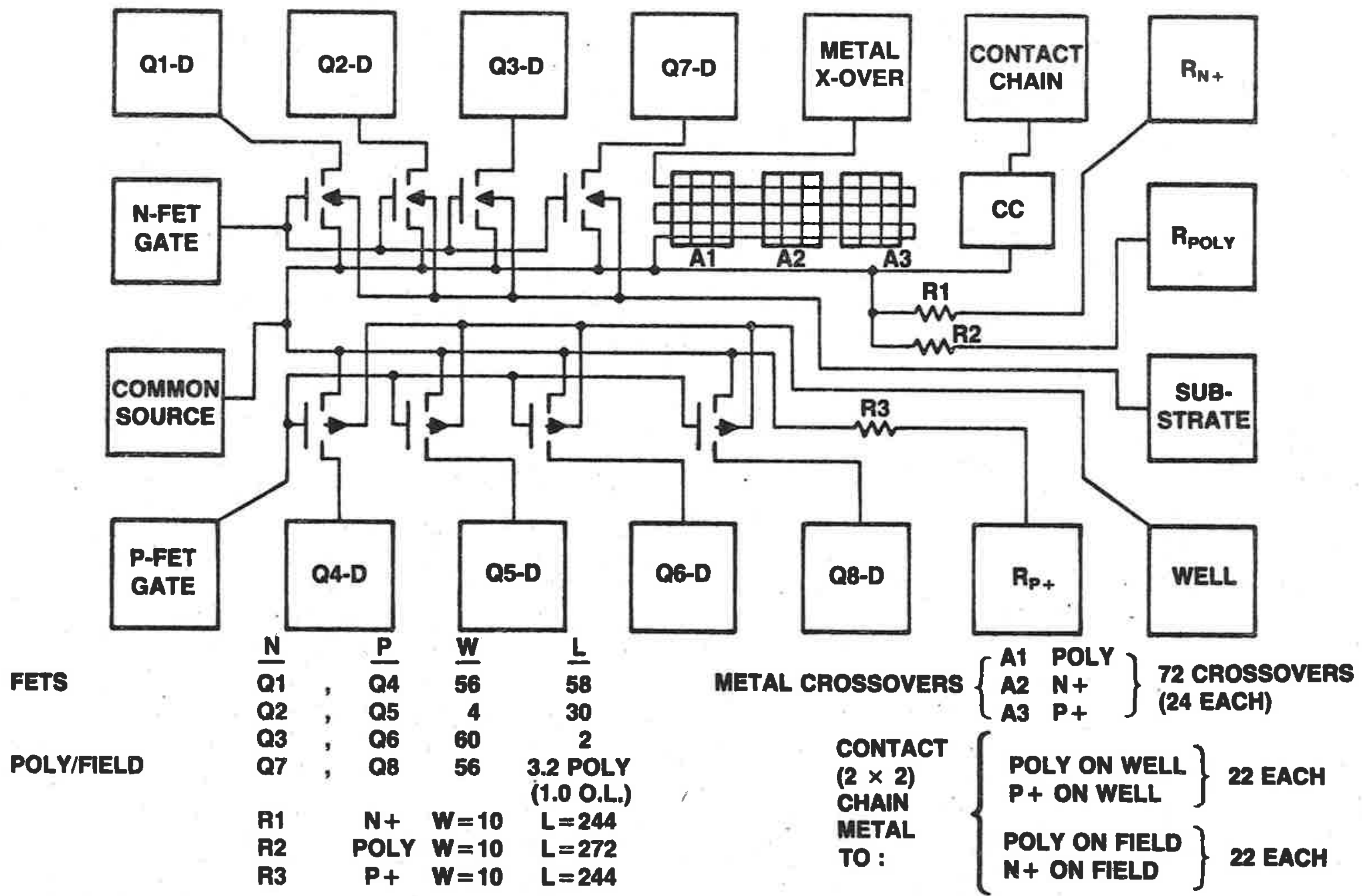
- HIGH R_{ON}
- LOW I_D (SAT)
- HIGH L_{EFF}

GATE OXIDE PROBLEM

- HIGH GATE LEAKAGE CURRENT

Rockwell International

TD18 FOR CMOS (BULK)



	N		P	W	L
FETS	Q1	,	Q4	56	58
	Q2	,	Q5	4	30
	Q3	,	Q6	60	2
POLY/FIELD	Q7	,	Q8	56	3.2 POLY (1.0 O.L.)
	R1		N+	W=10	L=244
	R2		POLY	W=10	L=272
	R3		P+	W=10	L=244

METAL CROSSOVERS { A1 POLY, A2 N+, A3 P+ } 72 CROSSOVERS (24 EACH)

CONTACT (2 × 2) CHAIN METAL TO :
- POLY ON WELL, P+ ON WELL — 22 EACH
- POLY ON FIELD, N+ ON FIELD — 22 EACH

Rockwell International

Test Chip Strategy for a High Volume VLSI Design Laboratory

Mark E. Potter
Bell Labs

Subject: Test Chip Strategy for a high volume VLSI design laboratory

October 15, 1983

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Bell Labs
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ABSTRACT

An environment of many design prove-ins per year using an existing VLSI technology requires a special test chip strategy. Process monitoring for control and speedy failure analysis in a production mode are the driving forces rather than process development motivations. The goals of a test chip system for such a situation will be listed in this paper. The methods used to achieve these goals in the Custom Logic laboratory of Bell Labs will be outlined. Examples will be drawn from the technologies used routinely by Custom Logic designers, namely, 3.5um and 2.5um Twin Tub CMOS [1], which have been up and running on Western Electric facilities for several years. The characterization parameters and test structures used will be reviewed. Software data manipulation results will be presented in format form showing what can be done once a data base is established.

The following capabilities are the test chip objectives in approximate order of importance:

1. Fast and complete process evaluation.
2. Process parameter centering via feed back to the clean room.
3. Simplified drafting utilizing all available space.
4. Simplified failure mode analysis (FMA).
5. Yield improvement.
6. Evaluation of design sensitivity to process variation.
7. Production parametric gathering.
8. Device modeling for simulation files.
9. Next generation design rule experience.
10. Evaluation of experimental structures.

Most of the goals have been achieved with a Test Pattern Array (TPA) strategy. A 1500um square arrangement of probe pads was designed and defined as a "module", see figure 1. Nine modules were filled with the minimum number of test structures needed for complete process characterization, hence, each test chip is required to contain at least these 9 modules. A total of 17 modules per technology have been created. A BASIC software routine called "TPA" was written which takes the "primary chip" size of a design, the number of bonding pads on the primary chip and the optimum alignment feature placement as inputs, and outputs the most efficient rectangular array of modules for the test chip ("secondary chip") along with complete drafting instructions. About 25 TPA's were drafted in anticipation of chip size requirements. Automatic probing of these TPA's is preprogrammed to minimize delays.

If the number of primary pads is large enough, the TPA output requests that certain module pads be connected via metal to an exact copy of the primary pads on the secondary. This will allow measurement of selected parameters during primary functionality testing in a production environment with no change of probe cards (goal 7). An example TPA output is labeled as figure 2 and the resulting secondary site layout can be seen in figure 3.

The contents of all the modules are outlined in figure 4a, including the non-essential modules which are included on secondaries as space permits. The categories of parameters are listed in figure 4b. Four of the non-essential modules are "buffer" modules. An example buffer module is seen in figure 5. These contain I-O buffer circuits wired to the module pads giving access to all the buffer's nodes. These prove very useful in buffer characterization for performance and reliability and for general failure analysis. The 53 specific parameters which are extracted from the modules are listed in figure 6. These are stored in a cumulative data base in a compact format.

Since most secondary sites contain more than the 9 basic modules, an experimental module can be easily substituted for a non-essential module. No special probe cards are needed since the standard pad arrangement is used. This procedure is especially effective in an laboratory which places mask orders almost daily.

The most important ingredient in a successful test chip strategy is yield improvement capabilities. While the devices listed above will help keep processing parameters centered, they contribute no information about uniformity across a wafer or cosmetic factors since they are placed in only two specific locations as dictated by the alignment feature requirements. Two additional sets of structures have been created to handle uniformity and cosmetic control.

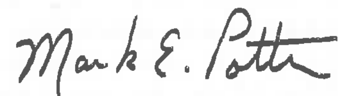
First, a set of very simple two terminal devices (called FMA features) are placed inside the saw apart grid above every primary and secondary chip. Wafer maps can then be generated for failure analysis investigations using a pair of manual probes attached to an automatic prober. Non-uniformities in process parameters are easily detected with these. The map shown in figure 7 is the forward turn-on voltage of an N+ source/drain to P-Tub diode. The entire center region is showing leakage current problems as seen by the 100 milivolt numbers (normal turn-on is about 600 milivolts) in figure 7a. Using the same data, a shaded plot was generated and is shown in figure 7b. Note that nothing unusual would have been detected in the upper test site since it lies in a good region of the wafer.

Second, a set of dense meandering patterns on critical lithography levels (called PRETEST for: Process Resolution & Evaluation TEST chip) have been developed by B. Keramati and are placed on the periphery of the tailored chip array for cosmetic data acquisition. These patterns are also used in design rule

evaluations. Failure analysis and process improvement efforts have been greatly simplified with these two sets of structures.

Figure 6 has shown the format used for lot average reporting. Parameters out of spec are flagged with an asterisk as seen in the figure at a glance. The entire data base can be averaged in this manner. Figure 8 shows other convenient output formats. Part "a" displays the 10 most critical parameters for each test site in a lot. With this information bad wafers can be weeded out, thus, saving valuable primary testing time. Part "b" shows the electrical line size data in a similar format. This is especially useful for analyzing lots with deliberately varied line sizes for design sensitivity to process variation evaluation.

There are many possible data manipulation schemes to present the data in useful plots, e.g., histograms, correlation plots, and control charts. Figure 9 shows the control chart of the p-channel threshold voltage from August of '82 through August of '83 for a particular clean room. A processing correction was obviously needed in March since the lower spec of -0.9 volts was crossed.



Mark E. Potter

ws:sandiego.ppr

REFERENCES

[1] L. C. Parillo, R. S. Payne, R. E. Davis, G. W. Reutlinger, and R. L. Field, "Twin-Tub CMOS - A Technology For VLSI Circuits", IEDM '80, Washington, DC, p752.

TRANSISTOR MODULE

(Standard 24 pad arrangement is shown)

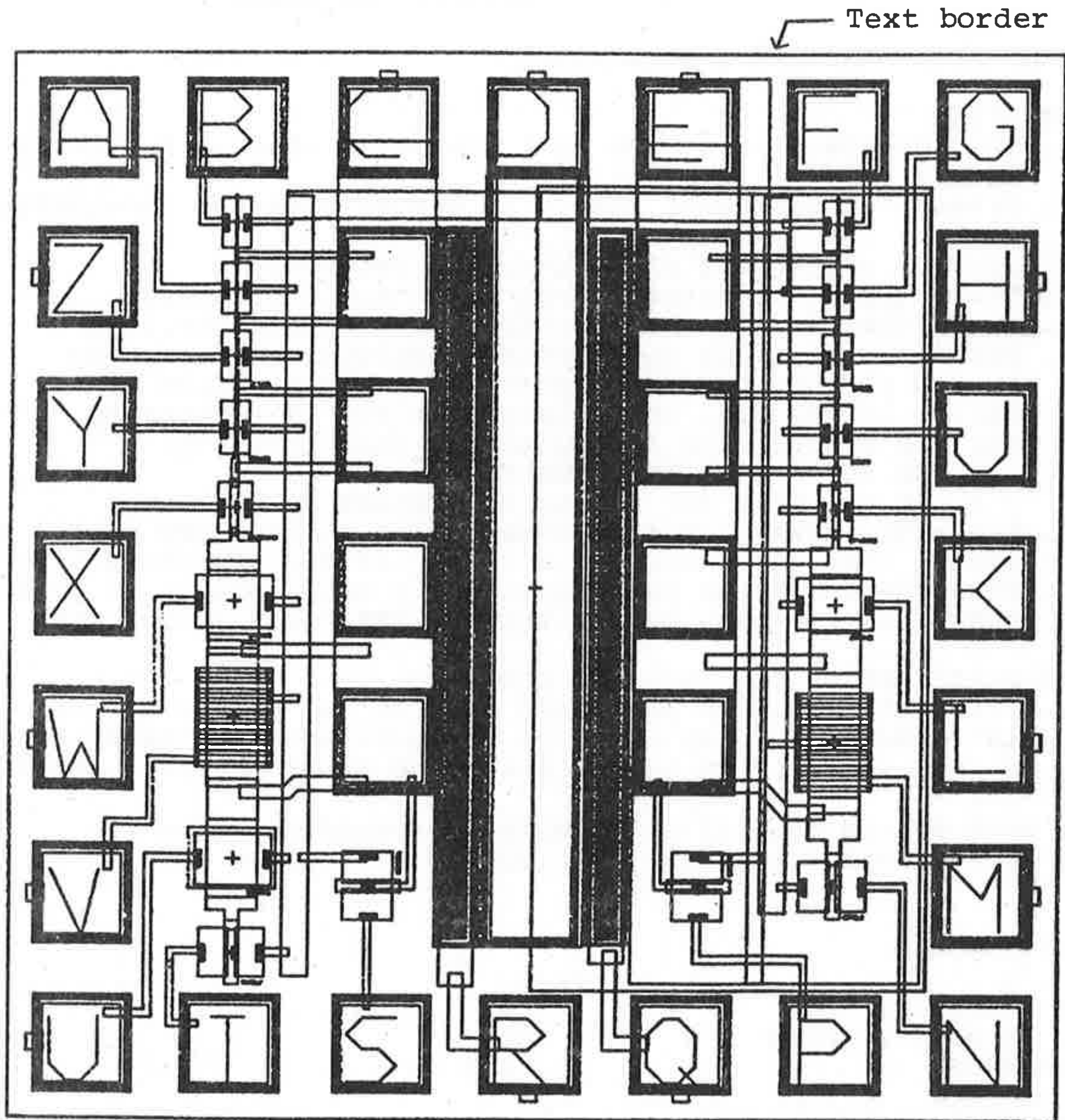


Figure 1.

PKG. CODE : 327U   TECH = 3.5 um   8/3Ø/82

STEP & REPEAT = 673Ø by 713Ø um   # PINS = 68   PEP TARGET = -1.73 mm

DRAFTING PERSON:
PRIMARY DESIGNER:

SECONDARY SITE DRAFTING INSTRUCTIONS

A. SITE SIZE
   1. The secondary site size is 1 times the size of a primary site: 673Ø by 713Ø um.
   2. Primary bonding pads should be copied onto the secondary.

B. PEP LOCATION within the clump & on the secondary
   1. The clump name containing the PEP module is TP3X3.
   2. Check the position of the PEP module within the test pattern. If it is not located Ø column(s) of modules to the LEFT of the TPA center and 1 row(s) BELOW the center of the TPA, then place it there by exchanging the PEP module with the module in that location.
      a. DO NOT ROTATE ANY MODULES !
      b. DO NOT MOVE ANY MODULE OFF-COLUMN OR OFF-ROW !
   3. Place the center of this clump Ø um to the LEFT of the site center and 154 um BELOW the center of the secondary site.
   4. Wire the inner TPA pads marked by a metal square to primary pads, one for one; DO NOT WIRE TO THE POWER SUPPLY PADS !

C. SITE PLACEMENT IN THE TAILORED ARRAY
   1. Place the finished secondary site in two places in the tailored array such that the PEP module is on the sites containing the PEP target specified by DFM's array sheet.

Please send a hard copy of all completed secondary sites to:
M. E. Potter AL 2D-249 (x7Ø9Ø)   Thank you.

SUMMARY	
TPA	TP3X3
PEP MODULE IN TPA	Ø ,-1
WIRING TO BONDING PADS	YES
TPA PLACEMENT	Ø ,-155 um

PROGRAMMER'S INFO (DRAFTING IGNOR)	
XPAD	62Ø
FINAL DELTA PEP	Ø , Ø
XB,YB	552.5 , 752.5
FLAGS	Ø Ø 1 Ø Ø Ø Ø
NX,NY,NX2,NY2	3 3 4 4

Figure 2,

TPA Layout
(from instructions in fig 2)

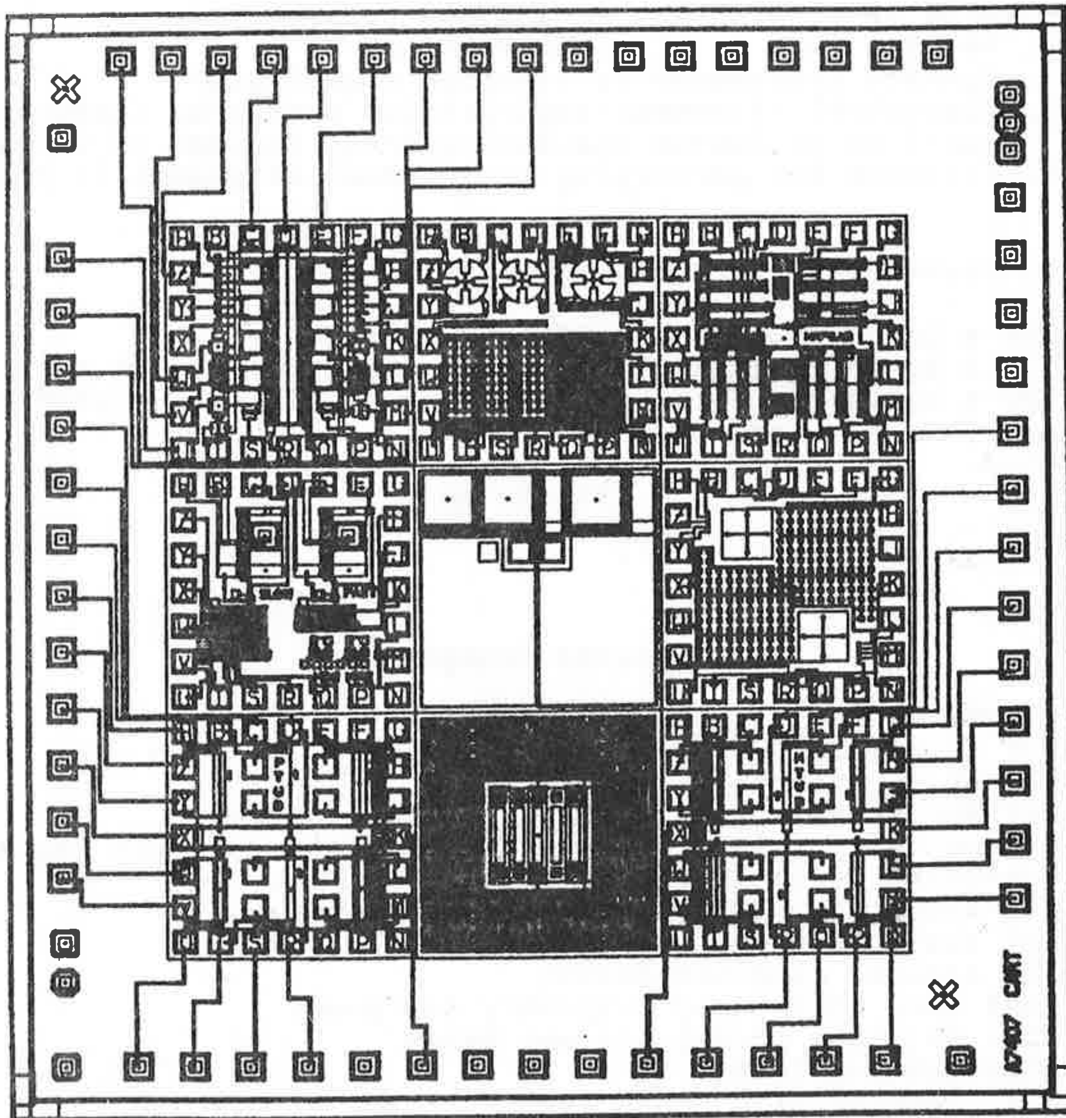


Figure 3.

Contents of the TPA Modules

(essential modules)

1. Transistors (sub-minimum design rule up to large square; field and composite devices; no threshold adjust device)
2. N-type four terminal resistors (diffusion & gate)
3. P-type " " " " "
4. Capacitors (all oxides possible)
5. Ring Oscillator and accessible polycells
6. Van der Pauw (& aluminum spiking)
7. Contact Resistance (& junction capacitors)
8. Electrical alignment registration measuring features (gate to diffusion and source/drain implant to diffusion)
9. Features for performing the optical alignment in process

(non-essential modules)

10. a large composite oxide capacitor
11. a dense feature suitable for SEM or TEM cross sections
12. a spreading resistance feature for diffusion profiling
13. four "buffer" modules

Figure 4a

Parameter Categories

(1) transistor thresholds and gains
(2) parasitic device parameters
(3) oxide thickness
(4) substrate surface doping concentrations
(5) mobility fall-off coefficients & source/drain resistance
(6) sheet resistances
(7) electrical diffusion & gate line sizes
(8) electrical channel lengths and widths
(9) lateral junction depths
(10) Ring Oscillator frequency and power
(11) polycell thresholds and betas
(12) tub contacts
(13) reverse bias break down voltages of all junctions
(14) Van der Pauw sheet resistance measurements and diode leakage currents
(15) contact resistances

Figure 4b

Buffer Module

(Individually wired circuits with access to all nodes.)

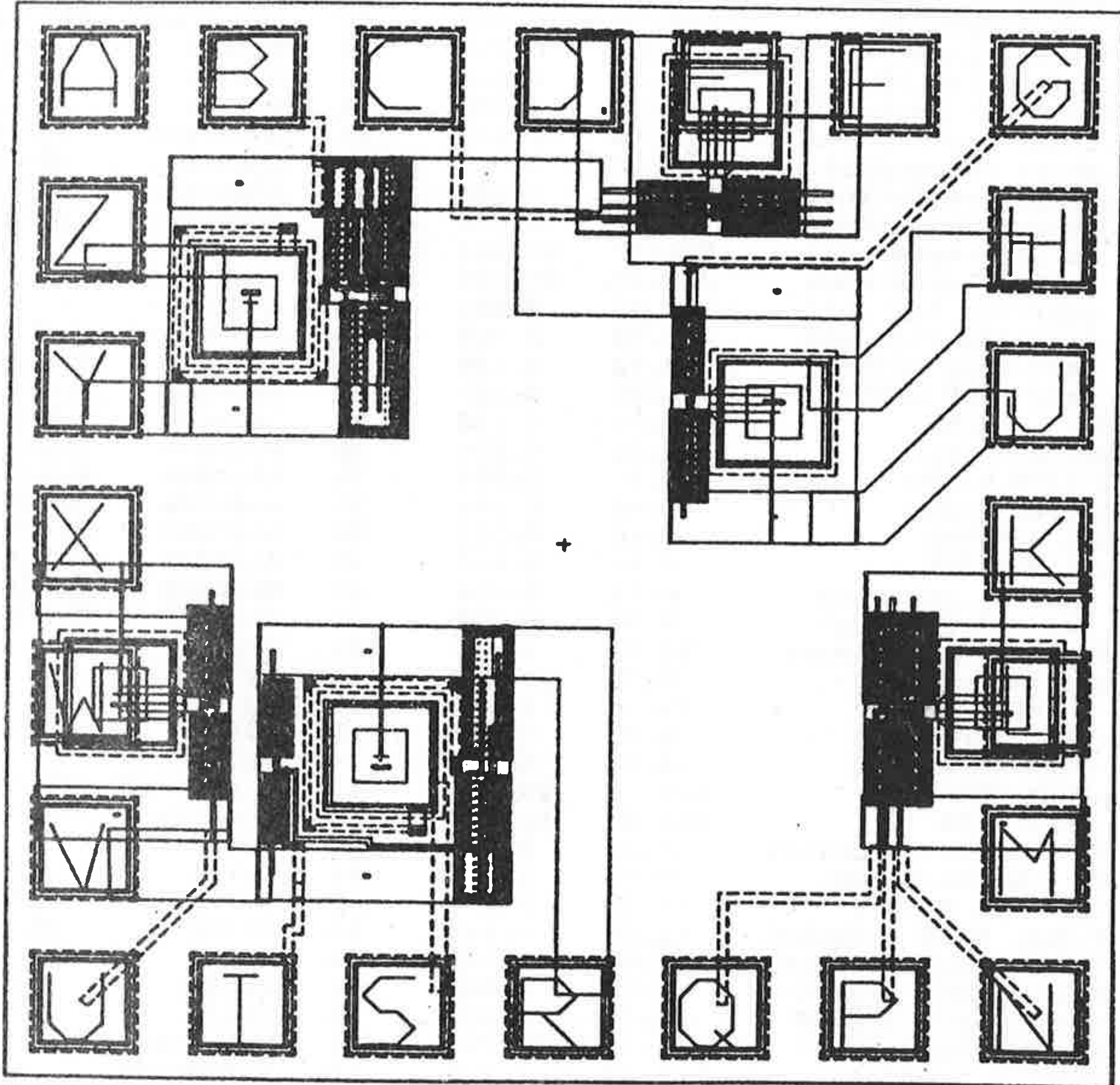


Figure 5

Figure 6

PROCESS PARAMETER AVERAGES FOR 3.5UM CMOS

lot number 8242 package code 366B date 27-JUN-83

PARAMETER	AVERAGE	STD DEV	SITES	UNITS	SPEC RANGE
N-CHAN 4X75 threshold	0.74	0.019	16	volts	.5/.9
P-CHAN 4X75 threshold	-0.79	0.023	16	volts	-.5/-.9
LARGE SQUARE N-CHAN BETA	42.81	0.725	15	E-6A/V**2	35/48
LARGE SQUARE P-CHAN BETA	14.47	0.293	15	E-6A/V**2	9/18
N-CHAN FIELD OX threshold	9.86	0.160	16	volts	> 8
P-CHAN FIELD OX threshold	-17.97	1.575	16	volts	< -8
GATE OXIDE THICKNESS	523.10 *	10.480	15	angstroms	525/625
N-TUB doping consentration	1.00	0.014	8	E16/cc	.8/1.5
N-TUB doping with VT ADJ	0.64	0.030	15	E16/cc	.3/.9
P-TUB doping consentration	1.25	0.100	15	E16/cc	.8/1.5
P-POLY sheet resistance	13.43	0.677	16	ohms/sq.	10/18
N-POLY sheet resistance	13.07	0.577	16	ohms/sq.	10/18
P-GASAD sheet resistance	105.24	1.720	16	ohms/sq.	90/135
N-GASAD sheet resistance	28.63	1.070	16	ohms/sc.	20/35
P-CHAN series resistance	166.57	85.264	15	ohms	
N-CHAN series resistance	120.45	38.704	16	ohms	
P-CHAN mobility fall-off	83.66	9.251	16	E-3/volt	
N-CHAN mobility fall-off	47.73	7.404	16	E-3/volt	
P-POLY GATE LINE WIDTH	3.52	0.139	16	microns	3.0/4.0
N-POLY GATE LINE WIDTH	3.50	0.131	16	microns	3.0/4.0
P-CHANNEL L PRIME	2.07	0.163	15	microns	1.5/2.5
N-CHANNEL L PRIME	1.95	0.254	16	microns	1.5/2.5
P-GASAD LINE WIDTH	4.66	0.095	16	microns	4.0/5.0
N-GASAD LINE WIDTH	4.48	0.044	16	microns	4.0/5.0
P-CHANNEL W PRIME	3.68	0.112	16	microns	3.0/4.5
N-CHANNEL W PRIME	4.36	0.115	14	microns	3.5/4.5
P-CHAN lateral junction	0.72	0.061	15	microns	0.6/1.0
N-CHAN lateral junction	0.80	0.078	15	microns	0.6/1.0
RING OSCILLATOR frequency	18.92	5.296	16	MHz	
RING OSCILLATOR power	5.55	0.310	15	mw	
BUFFER & INRB power	19.64	1.975	15	mw	
INRB N-CHAN threshold	0.69	0.022	15	volts	.5/.9
INRB P-CHAN threshold	-0.80	0.041	14	volts	-.5/-.9
INRB N-CHAN BETA	422.78	28.957	15	E-6A/V**2	250/700
INRB P-CHAN BETA	340.88	15.239	14	E-6A/V**2	250/700
N-TUB TO SUBSTRATE CONTACT	0.01	0.000	16	volts	< .2
P-TUB TO SUBSTRATE FWD.	0.63	0.007	16	volts	.5/.75
N-TUB TO P-TUB REV.	-49.38	0.547	16	volts	40/60
N+ TO P-TUB, GATE & SOURCE	15.84	4.983	16	volts	10/20
P+ TO N-TUB, GATE & SOURCE	-26.93	2.162	16	volts	20/30
N+ TO P+TC & GATE (ZENER)	6.33	0.067	16	volts	5/7
P+ TO N+TC & GATE (ZENER)	-6.30	0.075	16	volts	-5/-7
P-TUB Van Der Pauw sheet	7338.53	101.214	16	ohms/sq.	
TUB LEAKAGE @ 5 volts	1.42	1.705	16	E-15A/um2	
N+ Van Der Pauw sheet	27.79	1.518	16	ohms/sq.	20/35
N+ LEAKAGE @ 5 volts	1.28	1.644	12	E-15A/um2	
P+ Van Der Pauw sheet	103.35	3.092	16	ohms/sq.	90/135
P+ LEAKAGE @ 5 volts	1.92	1.809	13	E-15A/um2	
P+ contact resistance	12.01	3.952	14	ohms	-
N+ HIGH con. resistance	83.98	24.976	16	ohms	
N+ LOW con. resistance	120.47	63.681	16	ohms	
N-POLY con. resistance	2.41	0.726	16	ohms	
P-POLY con. resistance	2.41	0.590	16	ohms	

number of sites averaged = 16

*** 3.5um CMOS Individual Site Critical Parameters ***

lot number 8242 package code 366B date 27-JUN-83

WAFER	SITE	TOX	RsP	RsN+	RsP+	n-LP	p-LP	Vtn	Vtp	nB	pB	EPI
*****	****	***	***	****	****	****	****	***	***	**	**	***
5	TOP	48.	13.2	28.6	104.1	1.83	11.84	0.70	-0.78	441.	349.	N
5	BOT	521.	14.3	29.8	103.4	2.01	2.01	0.69	-0.78	424.	344.	N
8	TOP	514.	13.0	28.2	105.6	1.75	1.78	0.69	-0.76	462.	362.	N
8	BOT	515.	13.8	29.6	106.0	1.86	1.92	0.67	-0.76	462.	363.	N
14	TOP	526.	13.4	26.0	107.7	1.50	1.89	0.68	-0.88	442.	352.	N
14	BOT	529.	14.4	29.2	103.4	1.88	2.03	0.68	-0.83	414.	345.	N
2	TOP	506.	12.8	28.2	106.7	1.86	1.96	0.66	-0.82	410.	344.	N
2	BOT	503.	13.8	30.4	104.1	2.11	2.15	*****	-7.97	0.	0.	N
18	TOP	537.	12.8	28.3	107.0	1.93	2.05	0.73	-0.73	395.	322.	N
18	BOT	537.	14.0	29.4	103.6	2.07	2.23	0.67	-0.89	369.	312.	N
16	TOP	524.	12.6	27.9	107.2	2.01	2.19	0.71	-0.73	396.	329.	N
16	BOT	522.	13.9	29.3	104.2	2.08	2.35	0.71	-0.77	392.	322.	N
3	TOP	523.	12.5	27.9	106.8	1.75	2.00	0.71	-0.78	453.	345.	N
3	BOT	522.	12.6	27.8	107.4	2.71	2.31	0.68	-0.81	459.	349.	N
22	TOP	534.	13.4	28.1	104.1	1.85	2.00	0.73	3.18	412.	0.	N
22	BOT	534.	14.5	29.6	102.6	1.98	2.22	0.71	-0.80	411.	334.	N
AVERAGES		523.	13.4	28.6	105.2	1.95	2.07	0.69	-0.80	423.	341.	
STD DEVs		10.	0.7	1.1	1.7	0.25	0.16	0.02	0.04	29.	15.	

Figure 8a

*** Design Tolerance Data * 3.5um CMOS ***

lot number 8242 package code 366B date 27-JUN-83

wafer	site	N-CHANNEL L	L-ELEC	W	W-ELEC	XJ	P-CHANNEL L	L-ELEC	W	W-ELEC	XJ
*****	****	****	******	****	******	****	****	******	****	******	****
5	TOP	3.43	1.83	4.52	4.33	0.80	3.46	****	4.66	3.59	****
5	BOT	3.53	2.01	4.47	4.55	0.76	3.54	2.01	4.54	3.79	0.76
8	TOP	3.22	1.75	4.55	4.40	0.73	3.25	1.78	4.76	3.75	0.74
8	BOT	3.22	1.86	4.45	4.56	0.68	3.22	1.92	4.55	3.70	0.65
14	TOP	3.46	1.50	4.40	4.34	0.98	3.45	1.89	4.89	3.79	0.78
14	BOT	3.54	1.88	4.52	4.39	0.83	3.53	2.03	4.65	3.82	0.75
2	TOP	3.48	1.86	4.52	4.17	0.81	3.41	1.96	4.71	3.56	0.73
2	BOT	3.51	2.11	4.48	4.49	0.70	3.52	2.15	4.59	3.84	0.68
18	TOP	3.69	1.93	4.45	4.24	0.88	3.71	2.05	4.62	3.63	0.83
18	BOT	3.65	2.07	4.42	9.12	0.79	3.74	2.23	4.54	3.51	0.76
16	TOP	3.51	2.01	4.49	4.32	0.75	3.56	2.19	4.74	3.57	0.68
16	BOT	3.63	2.08	4.50	9.23	0.77	3.57	2.35	4.60	3.68	0.61
3	TOP	3.50	1.75	4.42	4.33	0.88	3.52	2.00	4.73	3.49	0.76
3	BOT	3.54	2.71	4.49	4.28	0.42	3.58	2.31	4.69	3.75	0.64
22	TOP	3.60	1.85	4.54	4.38	0.87	3.57	2.00	4.71	3.63	0.78
22	BOT	3.56	1.98	4.48	4.24	0.79	3.63	2.22	4.59	3.75	0.71
AVERAGES		3.50	1.95	4.48	4.96	0.78	3.52	2.07	4.66	3.68	0.72
Std Dev		0.13	0.25	0.04	1.65	0.12	0.14	0.16	0.10	0.11	0.06

Figure 8b

Wafer Maps

FORWARD VOLTAGE*100 @ +1mA

CODE 382A LOT 0011 WAFER 8521-09 PIN INPUT

				596	324	142	459	567	542	571				
			564	546	526				568	581	3976			
		552	540	540	569	569	558	579	274	1109	3976	3976		
	438	540	567	560	586	616	598	98	97	97	96	96	362	
	561	569	552	508	140	99	99	99	98	98	97	96	111	
529	532	545	587	100	100	100	100	100	99	98	99	97	144	625
562	564	562	622	100	101	101	101	100	100	100	99	97	97	652
214	566	580	100	101	101	102	102	101	101	100	99	98	97	98
73	565	578	100	101	102	102	102	102	102	101	100	98	98	103
90	567	81	101	102	102	103	103	102	102	101	100	98	97	111
464	570	100	101	102	102	103	103	103	102	101	100	99	98	3616
	590	99	100	101	102	103	103	102	102	101	100	100	101	
	583	98	100	101	101	102	102	102	101	101	100	99	99	
		98	99	100	100	101	101	101	101	102	101	100		
			98	98	99				100	99	100			
				141	99	124	456	100	116	98				

Figure 7a

FORWARD VOLTAGE @ +1mA

CODE 382A LOT 0011 WAFER 8521-09 PIN INPUT

,,, 0.00 *** 1.10 ...

				...	...	...	...	...	...	...				
			...	...	...				...	...	...			
		...	...	...	...	...	...	...	...	...	...	...		
	...	...	...	...	...	...	...	***	***	***	***	***	...	
	...	...	...	...	...	***	***	***	***	***	***	***	...	
...	...	...	...	***	***	***	***	***	***	***	***	***	...	...
...	...	...	...	***	***	***	***	***	***	***	***	***	***	...
...	...	...	***	***	***	***	***	***	***	***	***	***	***	***
***	...	...	***	***	***	***	***	***	***	***	***	***	***	***
***	...	***	***	***	***	***	***	***	***	***	***	***	***	...
...	...	***	***	***	***	***	***	***	***	***	***	***	***	...
	...	***	***	***	***	***	***	***	***	***	***	***	***	
	...	***	***	***	***	***	***	***	***	***	***	***	***	
		***	***	***	***	***	***	***	***	***	***	***		
			***	***	***				***	***	***			
				...	***	...	...	***	...	***				

Figure 7b

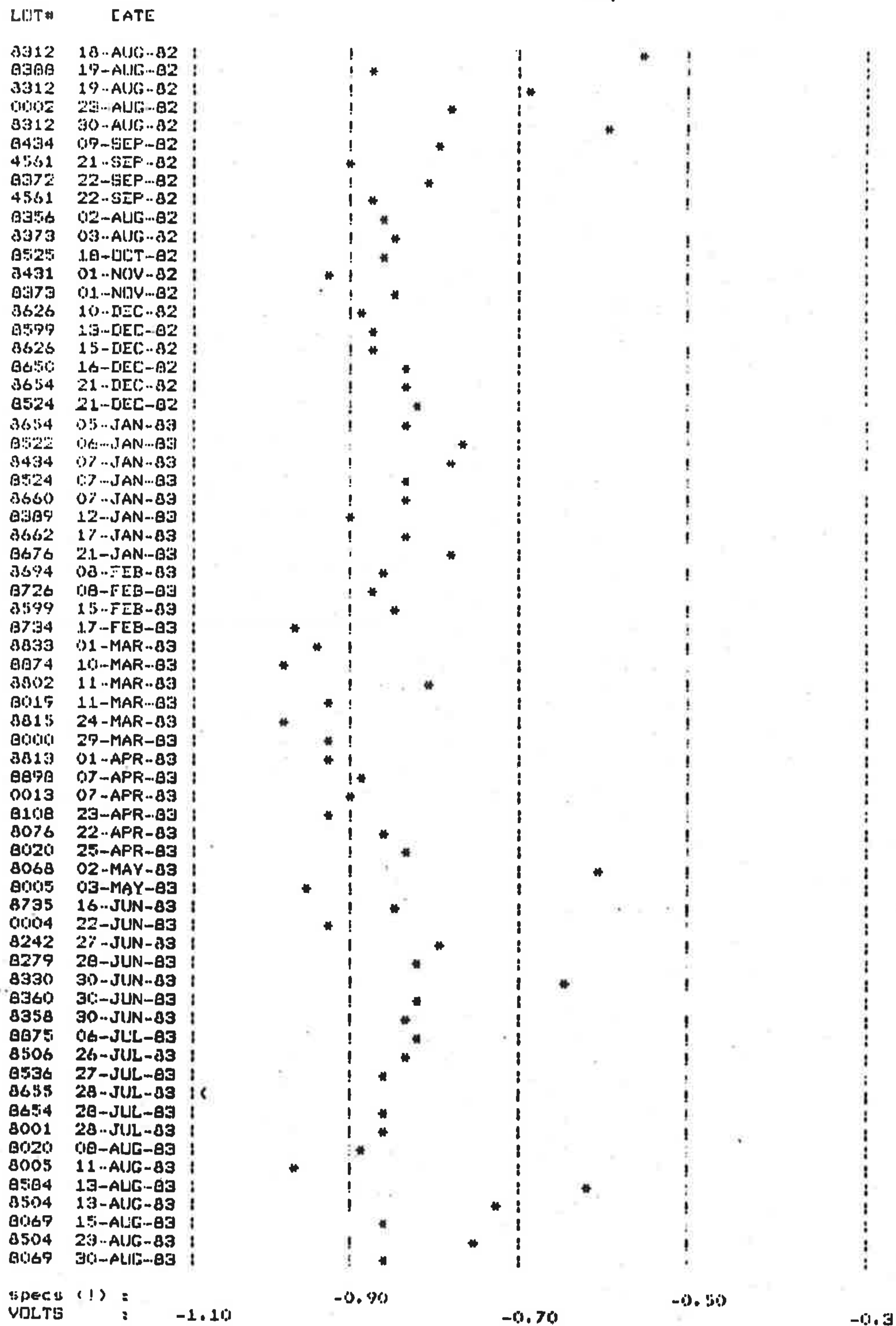


Figure 9

SESSION III YIELD AND RELIABILITY ASSESSMENT

Pinhole Array Capacitor for Oxide Integrity Analysis

Martin G. Buehler
Jet Propulsion Laboratory

PINHOLE ARRAY CAPACITOR FOR OXIDE INTEGRITY ANALYSIS

MARTIN BUEHLER

JET PROPULSION LABORATORY

FEBRUARY 1984

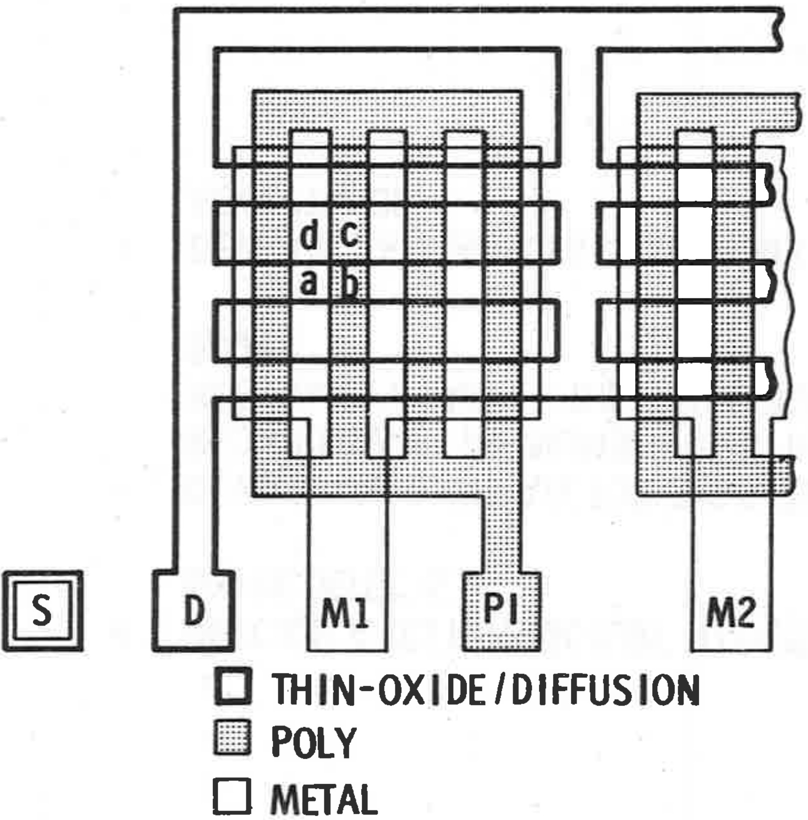
MGB-1

PINHOLE ARRAY CAPACITOR STUDY GOALS

- DEVELOP A TEST STRUCTURE TO DETECT AND CHARACTERIZE OXIDE DEFECTS
- DEVELOP AN ESTIMATE FOR THE SIZE OF THE STRUCTURE REQUIRED AND THE NUMBER OF SITES/WAFER REQUIRED TO ADEQUATELY SAMPLE THE OXIDE-DEFECT DENSITY ON A WAFER
- DEVELOP DATA ANALYSIS METHODS FOR USE IN LOT ACCEPTANCE

MGB-2

PINHOLE ARRAY CAPACITOR: LAYOUT DIAGRAM



- ELEMENT CONSISTS OF a-b-c-d REGION
- YIELD ANALYSIS

$Y = \exp(-N/E)$

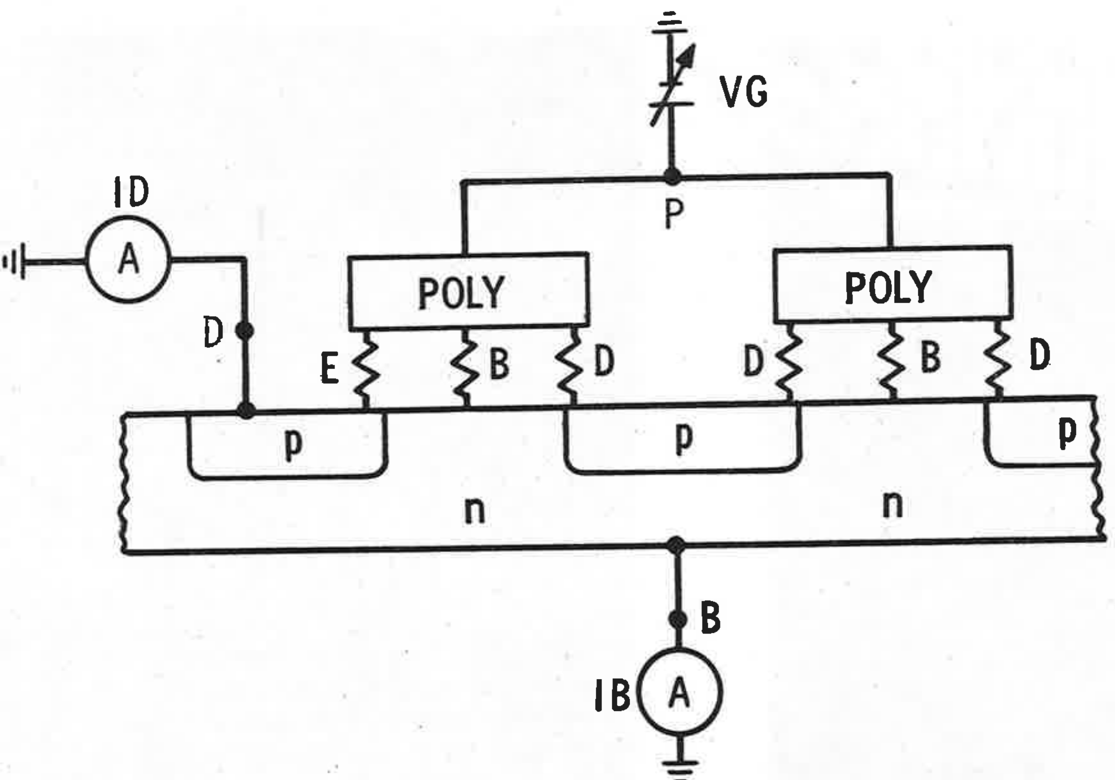
N = NUMBER OF ELEMENTS PER SUBARRAY

E = NUMBER OF ELEMENTS/DEFECT

AFTER BUEHLER, BLAES, PINA AND GRISWOLD (1983)

MG8-3

CROSS-SECTION OF THE PINHOLE ARRAY CAPACITOR



MGB-4

DEFECTIVE PIN-HOLE ARRAY CAPACITOR
METAL-TO-POLY SHORT

WAFER = 1104
LOCATION = R5C13
POLY TYPE = N

AFTER BUEHLER, BLAES, PINA, AND GRISWOLD (1983)

MGB-5

METAL-TO-POLY SHORT WAFER MAP

238

476

952

1904

3808

7616

: = OPEN (GOOD) SUBARRAY

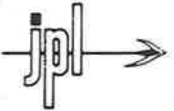
+⊕ = SHORT (DEFECTIVE) SUBARRAY

⊕ = EXCLUDED SITE

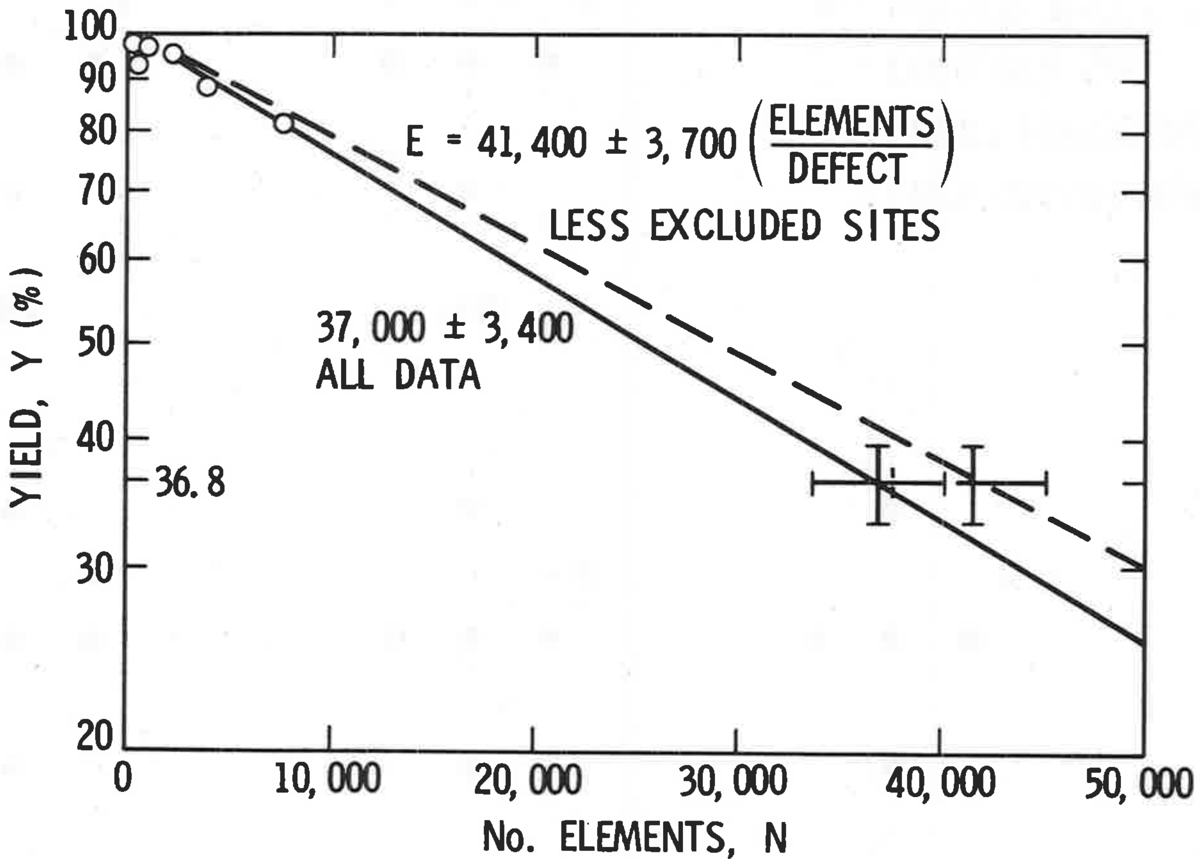
● = VENDOR TEST SITE

WAFER 1104
TEST CHIP 2012

MGB-6



YIELD ANALYSIS: METAL-POLY SHORTS



$$Y = \exp(-N/E)$$

MGB-7

WAFER MAPS OF DEFECTS DETECTED BY THE PINHOLE ARRAY CAPACITOR

○ = PHOTOMASK DEFECT
⬯ = VISUAL BLEMISH

B = POLY-BULK SHORT
M = METAL-POLY SHORT

G = GATE-OXIDE GLOBAL SHORT
P = PROBE FAULT

```
WAFER 3
           COL 369369C369C69
           ROW 4447777AAAADD
M/NP       756 -------------
          2268 -------------
          5292 ------P------
         11340 ----(M)------
P/ND       756 -------------
          2268 ------G------
          5292 -------------
         11340 ----(G)------
M/PP       756 -------------
          2268 -------------
          5292 --M----------
         11340 M-M----------
P/PD       756 -------------
          2268 -------------
          5292 ---B----B----
         11340 ------G---BB

M/NP      1668 -------------
          5004 -------------
         11676 -------------
         25020 M-M----------
P/ND      1668 -------------
          5004 -------G-[G]-G
         11676 ---------[G]-G
         25020 ---------[G]--
M/PP      1668 -------------
          5004 -------------
         11676 --------M----
         25020 --(M)--------
P/PD      1668 -------------
          5004 ------------B
         11676 ----G--BB----
         25020 --B(G)B--B--BBB

M/NP      2628 -------------
          7884 -------------
         18396 ------------M
         39420 -------------
P/ND      2628 -------------
          7884 -------------
         18396 ------------G
         39420 -----------G-
M/PP      2628 P------------
          7884 -------------
         18396 -------------
         39420 ---M-------M-M
P/PD      2628 -------------
          7884 ---B--B------
         18396 -------------
         39420 B--B-B-B---B-G

M = 12     D =  0
           E =  0
           B = 20
           G = 14
           ------
           T = 34
```

```
WAFER 4
           COL 369369C369C69
           ROW 4447777AAAADD
M/NP       756 -------------
          2268 -------------
          5292 -------------
         11340 -----(M)-----
P/ND       756 -------------
          2268 -------------
          5292 -------------
         11340 -----(G)B----
M/PP       756 ------M------
          2268 -------------
          5292 -------------
         11340 PPPP---------
P/PD       756 -------------
          2268 -------------
          5292 -------------
         11340 PPPP---------

M/NP      1668 -------------
          5004 -------------
         11676 -------------
         25020 -------------
P/ND      1668 -------------
          5004 -------------
         11676 -------------
         25020 -------------
M/PP      1668 -------------
          5004 -------------
         11676 ----------M--
         25020 ---(M)--M--M--
P/PD      1668 -------------
          5004 -----------B--
         11676 -------------
         25020 ---(G)B-B---B--

M/NP      2628 -------------
          7884 -------------
         18396 -------------
         39420 -------------
P/ND      2628 -------------
          7884 -------------
         18396 -------------
         39420 -------------
M/PP      2628 -------------
          7884 ------------M
         18396 -------------
         39420 -------------
P/PD      2628 -------------
          7884 -------------
         18396 -------------
         39420 B------------

M =  7     D =  0
           E =  0
           B =  6
           G =  2
           ------
           T =  8
```

```
WAFER 5
           COL 369369C369C69
           ROW 4447777AAAADD
M/NP       756 -------------
          2268 -------------
          5292 -------------
         11340 ----(M)-----M-
P/ND       756 -------------
          2268 -------------
          5292 -------------
         11340 ----(G)------
M/PP       756 -------------
          2268 -------------
          5292 ------------M
         11340 -------------
P/PD       756 -------------
          2268 -------------
          5292 -------------
         11340 -------------

M/NP      1668 -------------
          5004 -------------
         11676 -------------
         25020 ------------M
P/ND      1668 -------------
          5004 -------------
         11676 -------------
         25020 ------------G
M/PP      1668 -------------
          5004 -------------
         11676 ------------M
         25020 ---(M)------M-M
P/PD      1668 -------------
          5004 -----B-------
         11676 ------------G
         25020 ---(G)------G-G

M/NP      2628 -------------
          7884 -----M-------
         18396 -------------
         39420 ------------M
P/ND      2628 -------------
          7884 -------------
         18396 -------------
         39420 -------------
M/PP      2628 -------------
          7884 -------------
         18396 -------------
         39420 -------------
P/PD      2628 -------------
          7884 -----B-B-----
         18396 -------B-----
         39420 --B----------

M = 10     D =  0
           E =  0
           B =  5
           G =  6
           ------
           T = 11
```

```
WAFER 6
           COL 369369C369C69
           ROW 4447777AAAADD
M/NP       756 ----[M]-------
          2268 [M]--[M]-------
          5292 [M]--[M]-------
         11340 [M]-M-(M)-------
F/ND       756 ----[G]-------
          2268 G---[G]-------
          5292 ----[G]-------
         11340 G-G-(G)----G--
M/PP       756 M------------
          2268 ----[M]-------
          5292 ---M[M]-------
         11340 ----[M]-------
P/PD       756 -------------
          2268 ----[G]-------
          5292 --B-[G]-------
         11340 ----[G]-------

M/NP      1668 -------------
          5004 ------------[M]
         11676 [M]--[M]-------[M]
         25020 [M]--[M]-------[M]
P/ND      1668 -------------
          5004 ------------G
         11676 [G]--[G]-------
         25020 [G]-G-G[G]------
M/PP      1668 ---------M---
          5004 ---------M-[M]
         11676 ---------M-[M]
         25020 -M-(M)M------[M]
P/PD      1668 -------------
          5004 -------------
         11676 -------------
         25020 -G-(G)-------B

M/NP      2628 -------------
          7884 ---------M-[M]
         18396 [M]--[M]-------[M]
         39420 [M]--[M]---M---[M]
P/ND      2628 G------------
          7884 -------------
         18396 [G]--[G]-------
         39420 [G]--[G]-------
M/PP      2628 ---------M-[M]
          7884 ---------M-[M]
         18396 ------------[M]
         39420 ----M-M-M-M[M]
P/PD      2628 -------------
          7884 -------------
         18396 -------------
         39420 ----------GGG

M = 50     D =  0
           E =  0
           B =  2
           G = 29
           ------
           T = 31
```

AFTER BUEHLER, BLAES, PINA, AND GRISWOLD (1983)

MGB-8
2-21-84

CROSS-SECTION OF THE PINHOLE ARRAY CAPACITOR

TEST	CHAN	ID	IB	DEFECTS
1	0	0	0	N, D(7)
2†	0	0	1	B, B*
3†	0	1	0	E
4†	0	1	1	G
5†	1	0	0	N
6†	1	0	1	B*
7†	1	1	0	E, D, B
8	1	1	1	G

G = GLOBAL (MULTIPLE) DEFECT

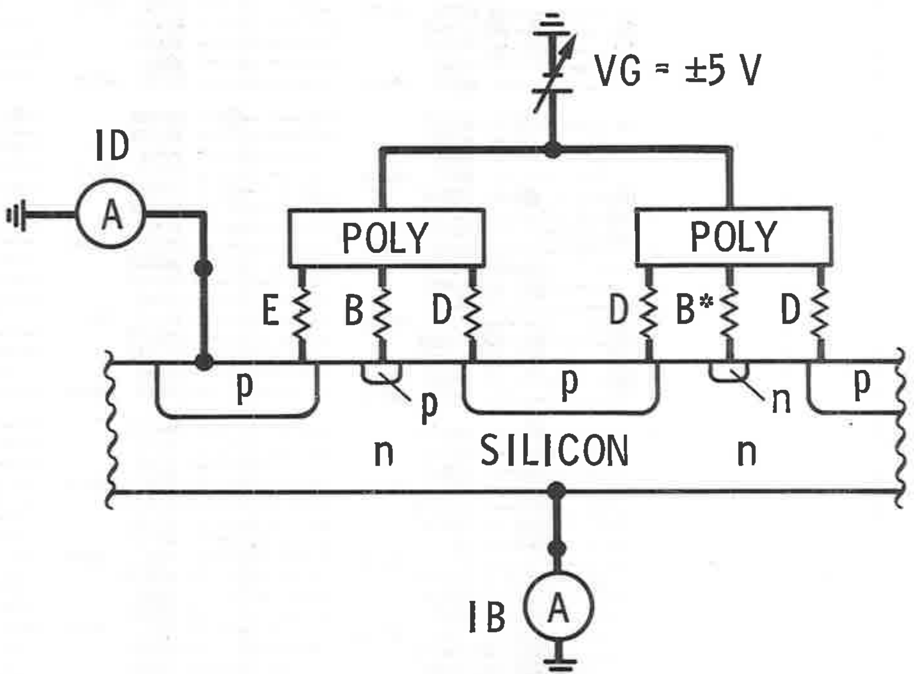
N = NO DEFECT DETECTED

B* = POLY-BULK DEFECT (RESISTOR)

B = POLY-BULK DEFECT (DIODE)

D = POLY-DIFFUSION DEFECT

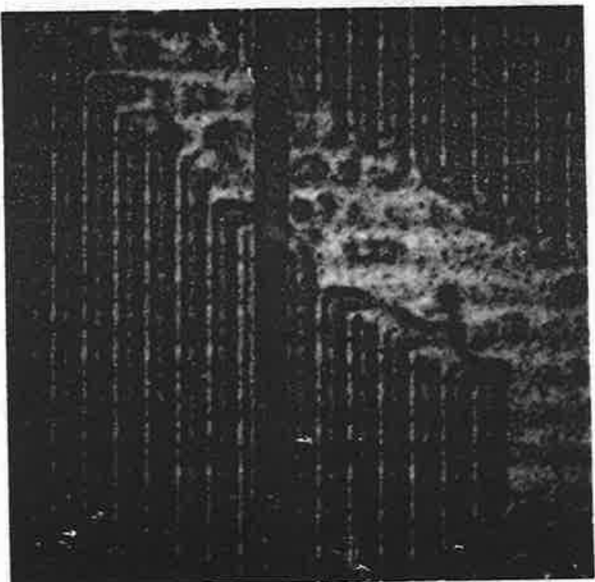
E = POLY-DIFFUSION DEFECT (EDGE OF ARRAY)



† = REQUIRED TEST

MGB-9

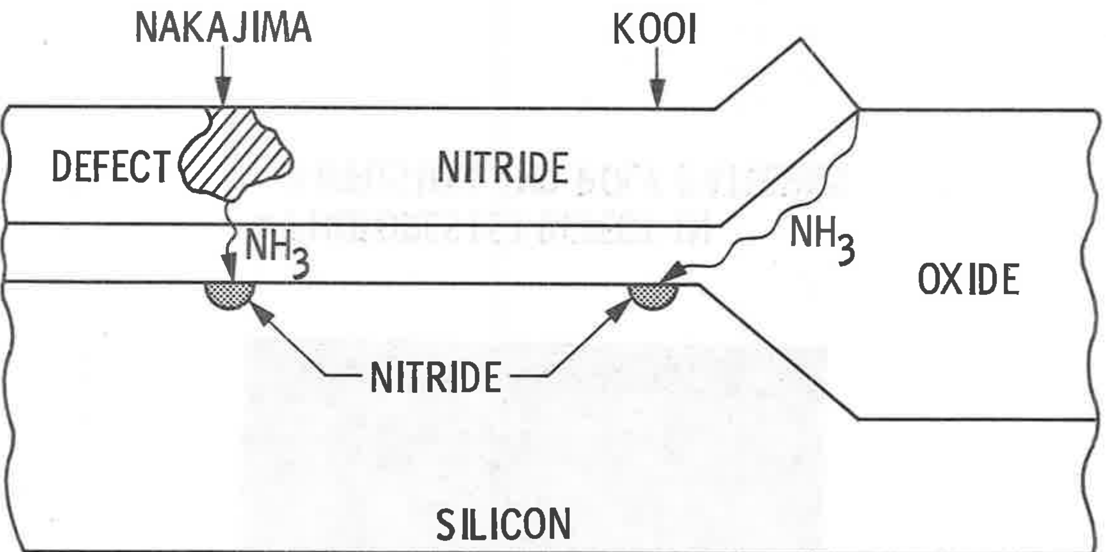
PINHOLE ARRAY CAPACITOR GLOBAL FAULT

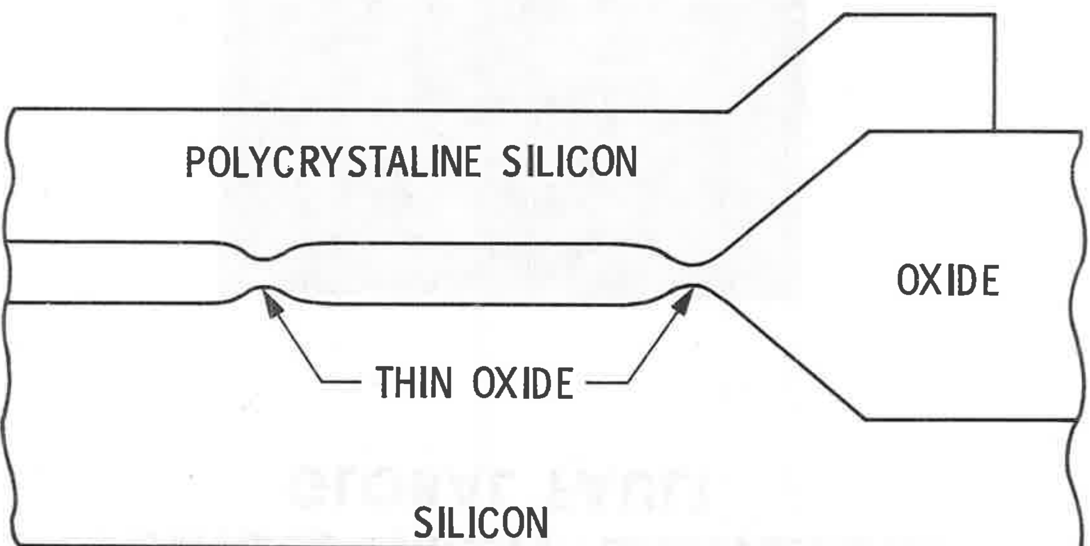


- PHOTORESIST DEFECT IN DIFFUSION AND POLY PATTERNS

jpl

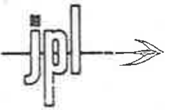
OXIDE POINT DEFECTS





AFTER KOOI (1976) AND NAKAJIMA ET AL (1979)

MGB-10B



PHOTOMICROGRAPH OF PINHOLE ARRAY CAPACITOR

PAC-3P PAC-3N

25020
11676
5004
1668

25020
11676
5004
1668

39420
18396
7884
2623

39420
18396
7884
2623

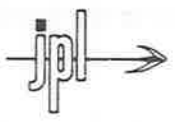
11340
5292
2268
756

11340
5292
2268
756

PAC-4P PAC-4N PAC-2P PAC-2N

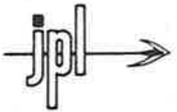
AFTER BUEHLER, BLAES, PINA, AND GRISWOLD (1983)

MGB-11



FROM MOSIS OF ISI

MGB-12



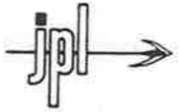
ELEMENTS/DEFECT* DETERMINED FROM THE PINHOLE ARRAY CAPACITOR

	WAFER 3	WAFER 4	WAFER 5	WAFER 6
M/NP	>107	>107	86	30
P/ND	>107	86	>107	25
M/PP	70	>107	>107	80
P/PD	42	>107	>107	82
M/ND	190	>237	>237	79
P/ND	150	>237	>237	68
M/PP	>237	105	105	65
P/PD	35	82	100	125
M/NP	>373	>373	>373	95
P/ND	>373	>373	>373	199
M/PP	189	>373	>373	71
P/PD	76	>373	330	190

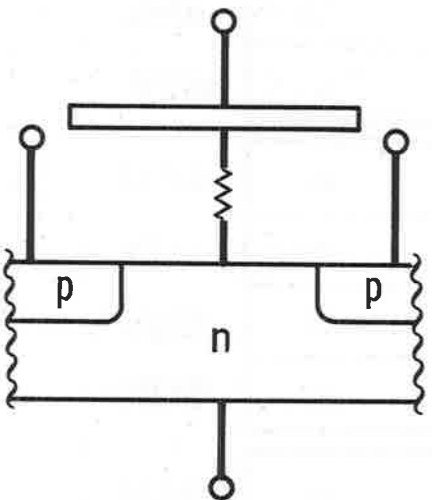
*NUMBERS IN THOUSANDS OF ELEMENTS/DEFECT

AFTER BUEHLER, BLAES, PINA, AND GRISWOLD (1983)

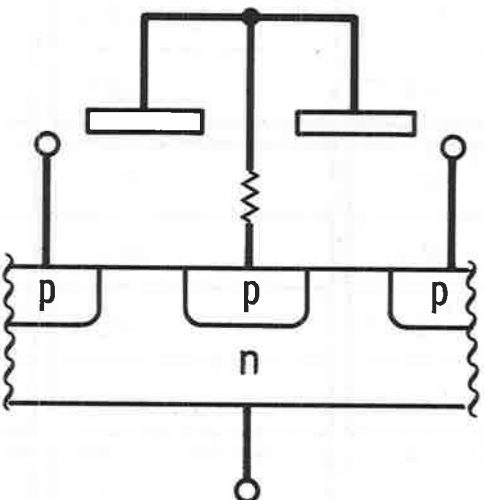
MGB-13



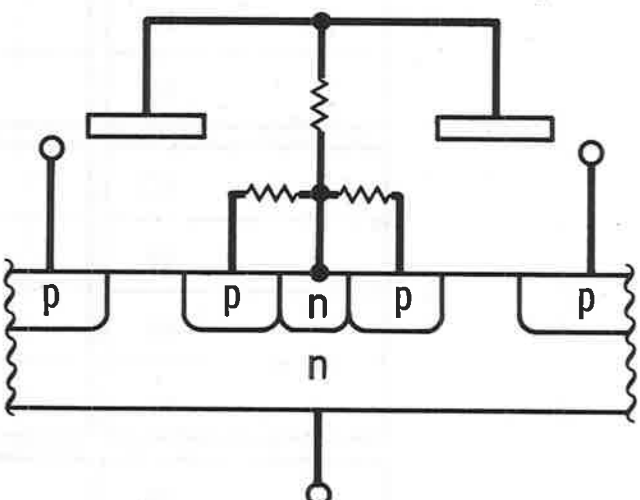
PROPOSED FAULT MODELS FOR OXIDE DEFECTS



NORMAL TRANSISTOR

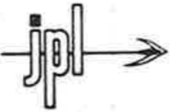


RESISTOR/DIODE MODEL



RESISTOR MODEL

MGB-14



PINHOLE ARRAY CAPACITOR STUDY CONCLUSIONS

- THE ANALYSIS FOR OXIDE DEFECTS IS DIFFICULT BECAUSE OF THEIR LOW DENSITY BUT AN "ORDER-OF-MAGNITUDE" ESTIMATE IS POSSIBLE GIVEN PROPER SAMPLING TECHNIQUES
- BY UTILIZING THE SWITCHING NATURE OF MOSFETs IN AN ARRAY, DIFFERENT TYPES OF GATE-OXIDE DEFECTS CAN BE DISTINGUISHED AND USED TO CONSTRUCT FAULT MODELS
- BY OBSERVING FAULTING IN ADJACENT SUBARRAYS, GLOBAL DEFECTS CAN BE IDENTIFIED
- SIGNIFICANT VARIABILITY IN OXIDE-DEFECT DENSITY WAS OBSERVED BETWEEN WAFERS AND THIS IMPLIES THAT ACCEPTANCE PLANS SHOULD BE BASED ON WAFER ACCEPTANCE

MGB-15

Test Structures for Examining Electromigration

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OUTLINE

- RELIABILITY ASSESSMENT WITH TEST STRUCTURES
- ELECTROMIGRATION: A VLSI FAILURE MECHANISM
- MULTIPURPOSE TEST CHIP
- INTERFERENCES
  - AREA UNCERTAINTY
  - TEMPERATURE PROFILE
    - o THERMAL MODELING
    - o FEEDBACK TO DESIGN AND TESTING
- NEEDS
  - PRE-INDICATORS
  - DEPENDABLE MEASUREMENTS AND REPORTING

RELIABILITY ASSESSMENT WITH TEST STRUCTURES

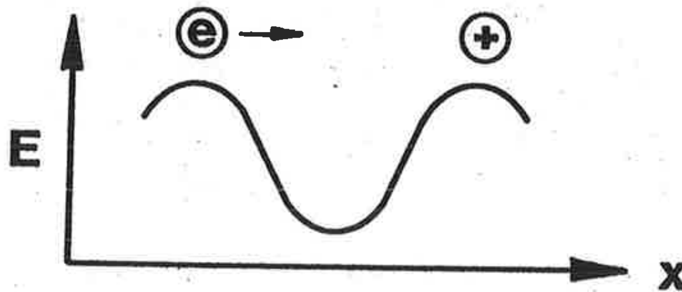
- NEW APPROACH FOR COMPLEX ICs
- DESIGN-IN SENSITIVITY TO FAILURE MECHANISM
- PAYOFFS:
  - MORE SPECIFIC INFORMATION
  - TIME SAVED
- GOAL: ON-WAFER TESTING

ELECTROMIGRATION METAL FLUX DENSITY

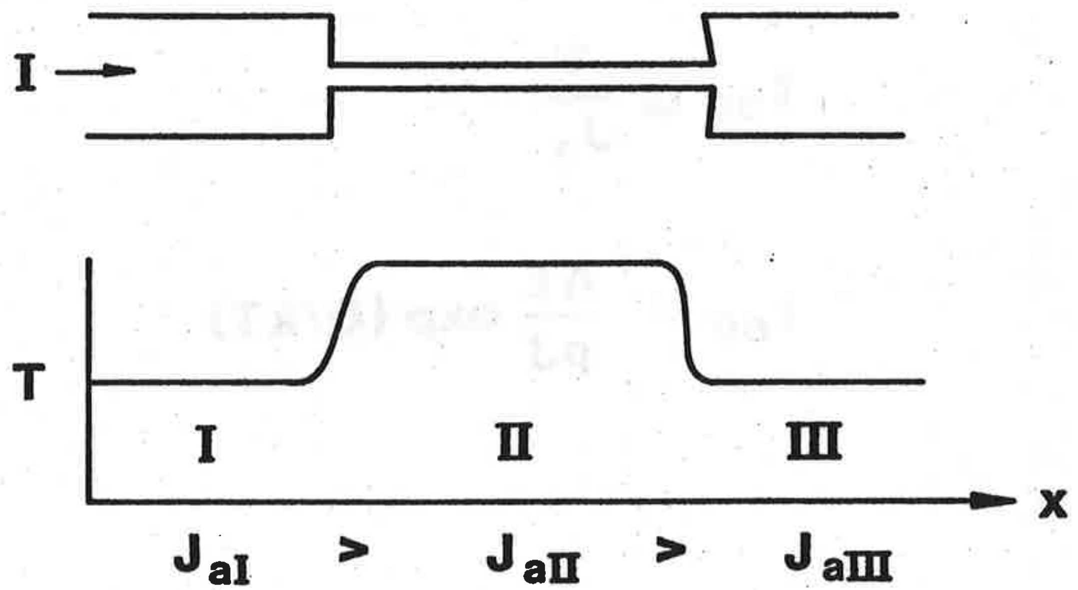
$$J_a = \mu F = \frac{D}{kT} F$$

$$F = Z^* e \mathcal{E} = Z^* e \rho J \; ; \quad D = D_o \exp(-Q/kT)$$

$$\boxed{J_a = \frac{C \rho J}{T} \exp(-Q/kT)}$$



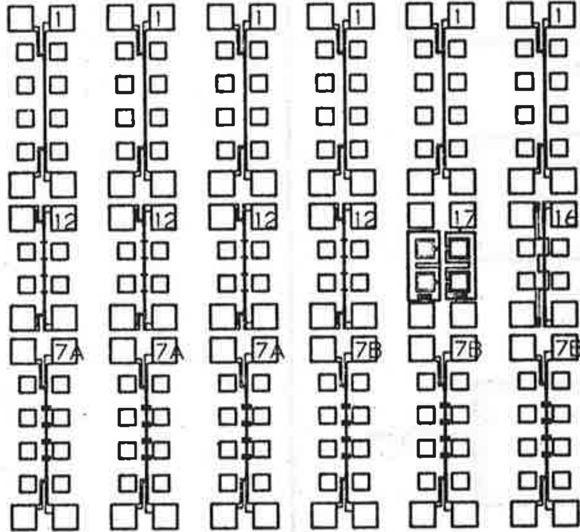
EFFECT OF TEMPERATURE GRADIENT

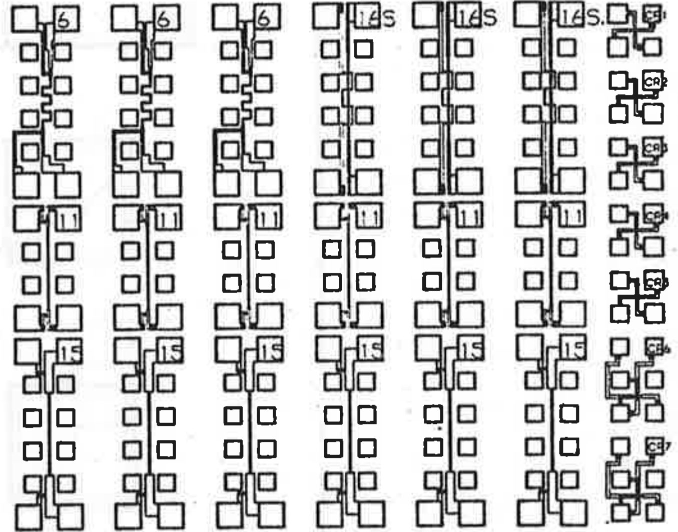


MEAN-TIME-TO-FAILURE, t_{50}

$$t_{50} \propto \frac{1}{J_a}$$

$$t_{50} = \frac{AT}{\rho J} \exp(Q/kT)$$


NBS-38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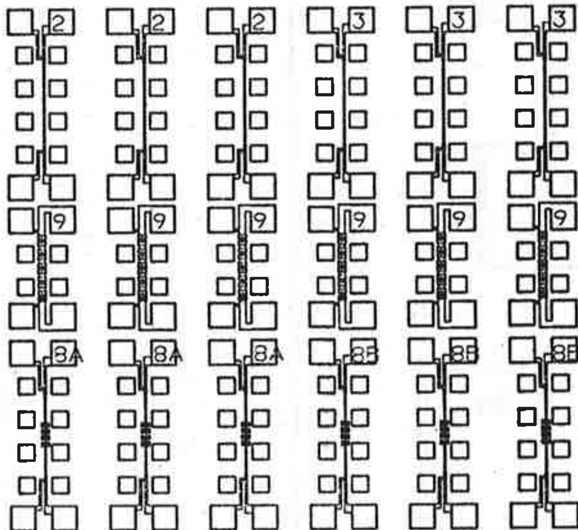
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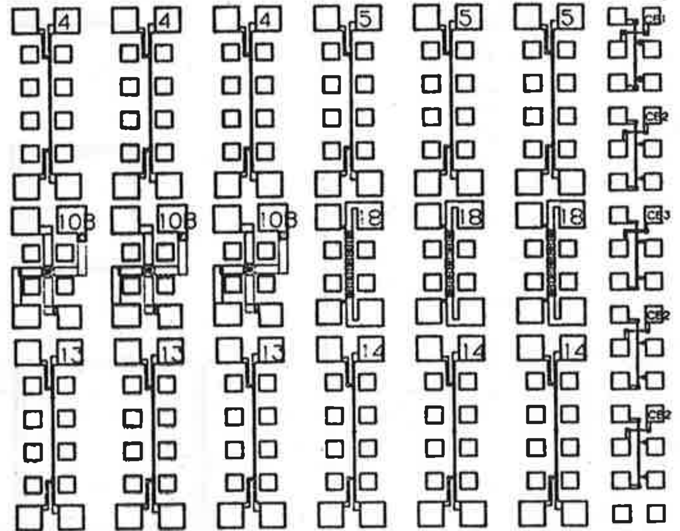
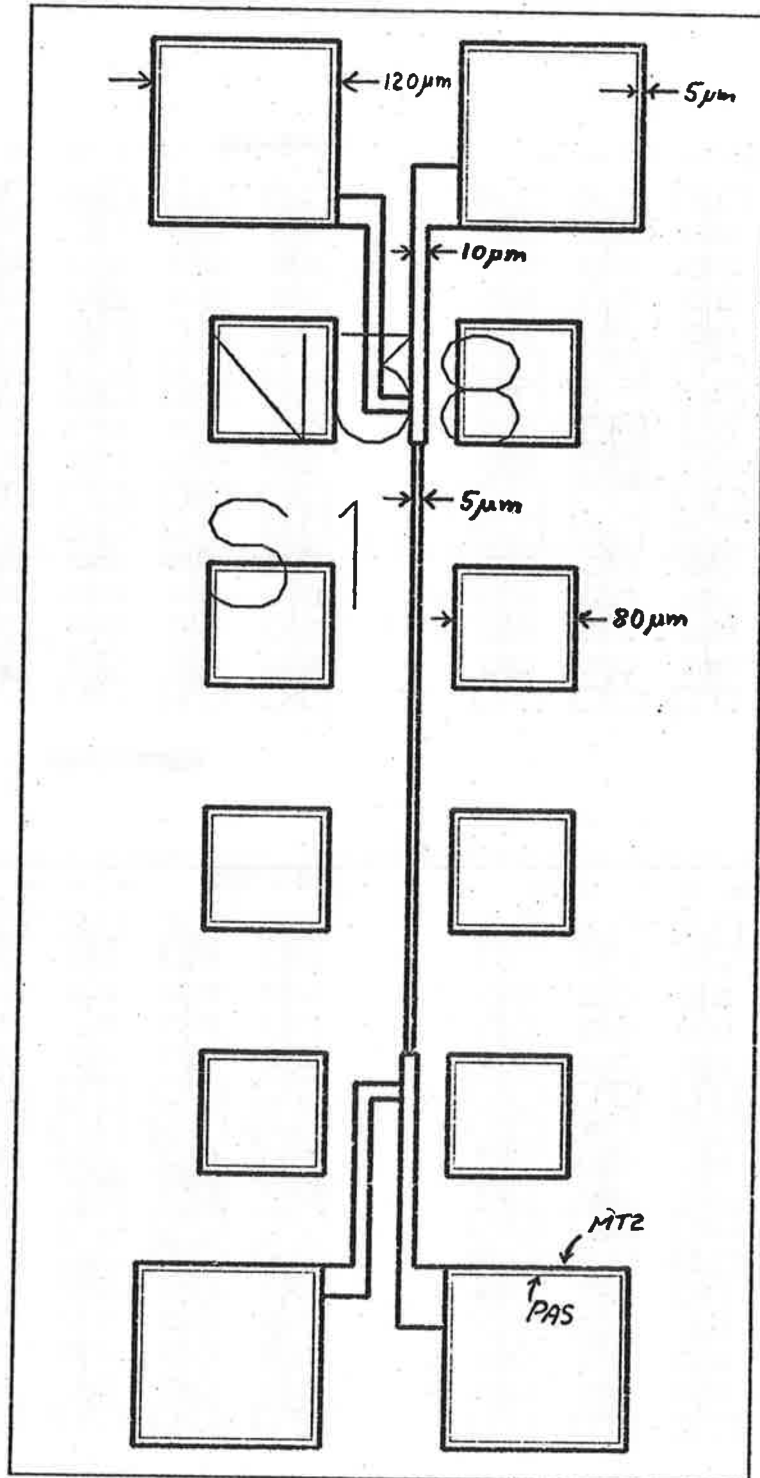
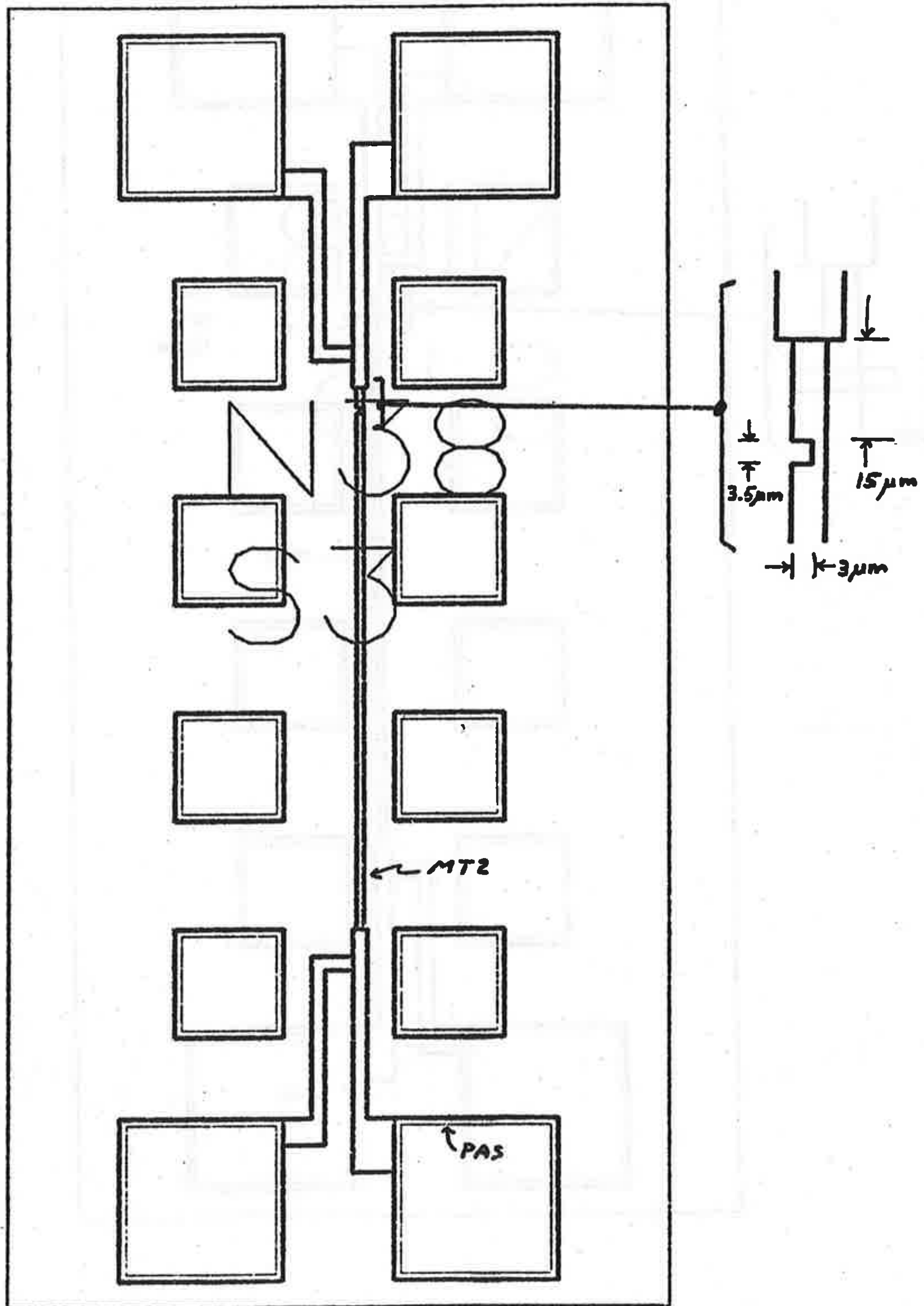
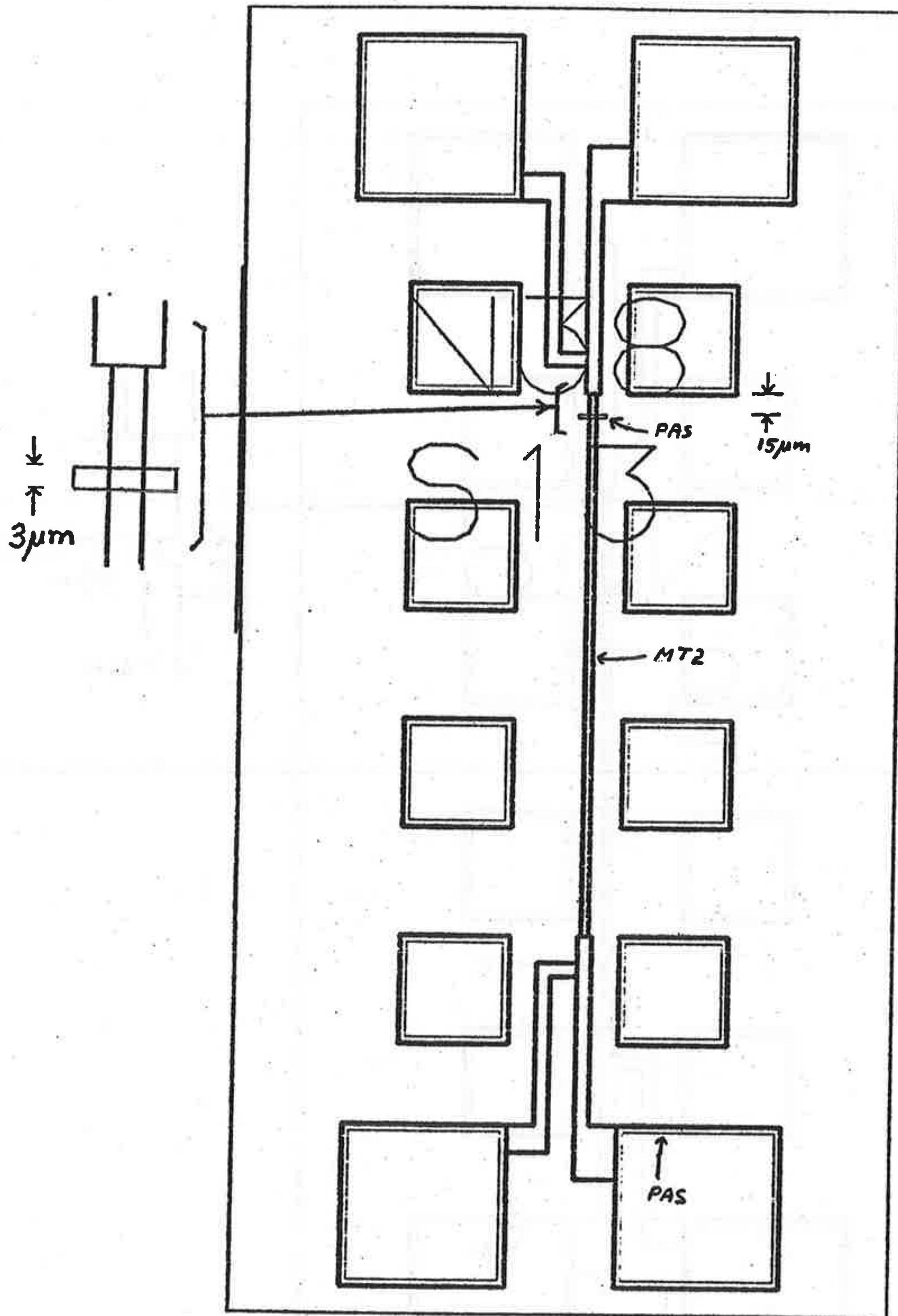

NBS-38



120μm
5μm
10μm
NU8
S1
5μm
80μm
MT2
PAS

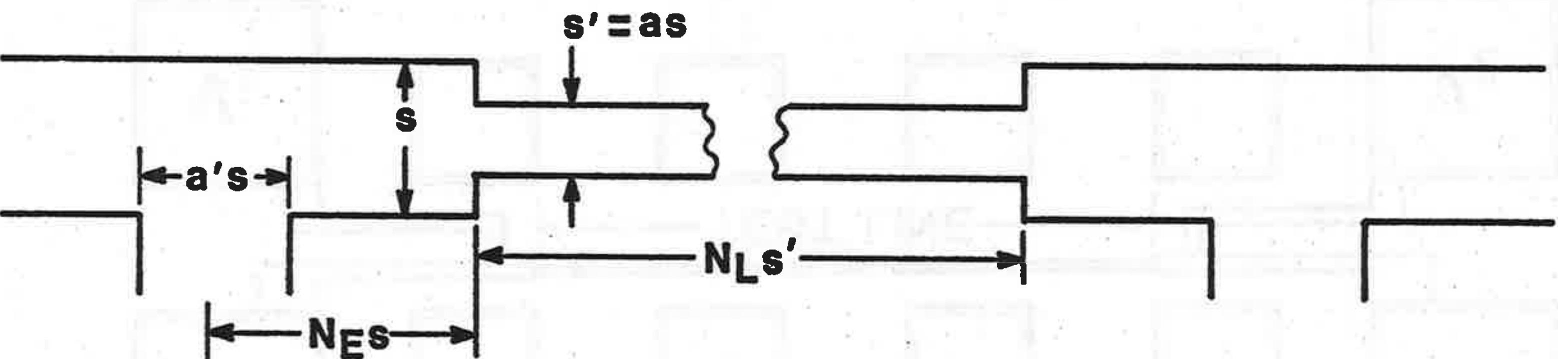


3.5μm
15μm
3μm
MT2
PAS



3μm
PAS
15μm
MT2
PAS

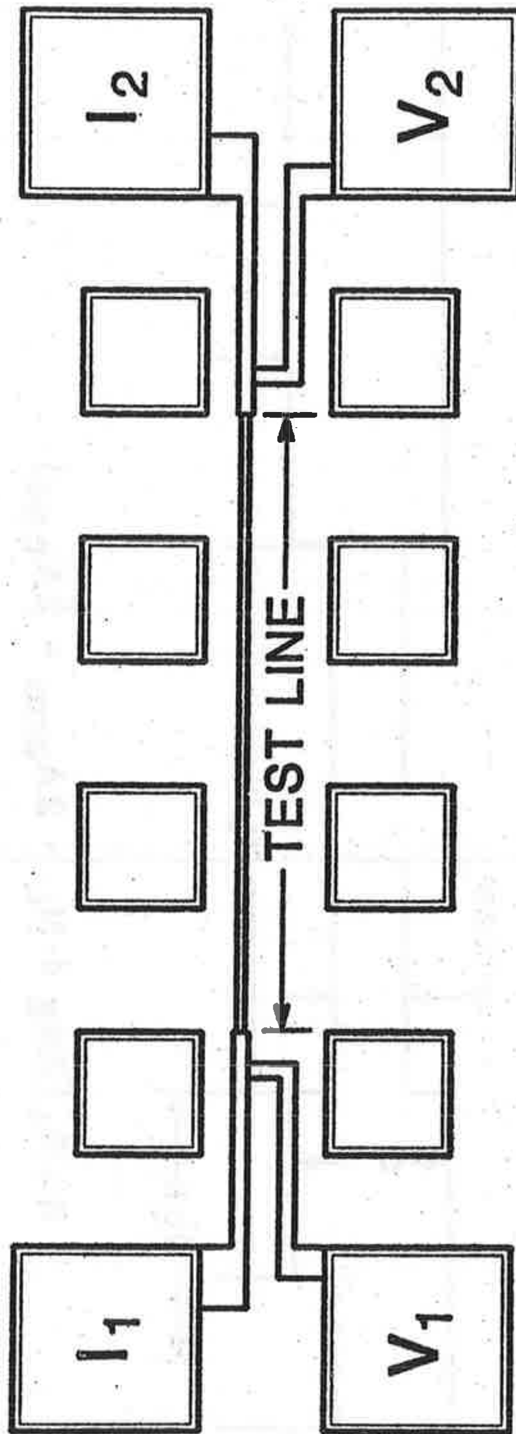
AREA CALCULATION



$$R = R_s(2N_E + N_L - 2A_{arm} + 2A_{end})$$

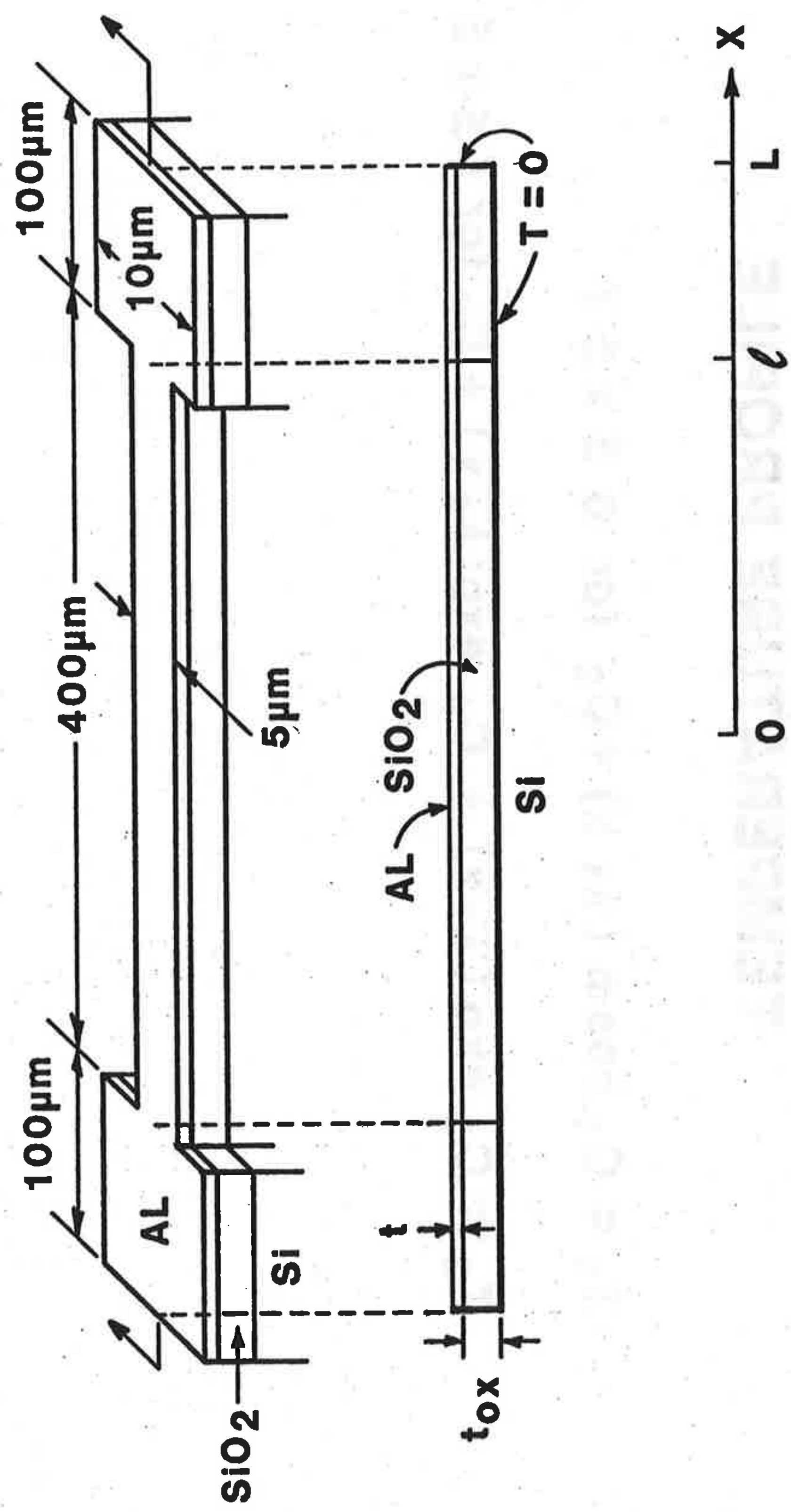
$$R \cong \frac{\rho}{tw}(50s'/s + 400)$$

$$A \cong \frac{\rho}{R}(50s'/s + 400)$$



I_2
V_2
TEST LINE
I_1
V_1

MODEL FOR TEMPERATURE PROFILE CALCULATIONS



TEMPERATURE PROFILE

$$T_1 = C_1 \cosh(\lambda_1 x) + C_2 \quad \text{for} \quad 0 \leq x \leq \ell$$

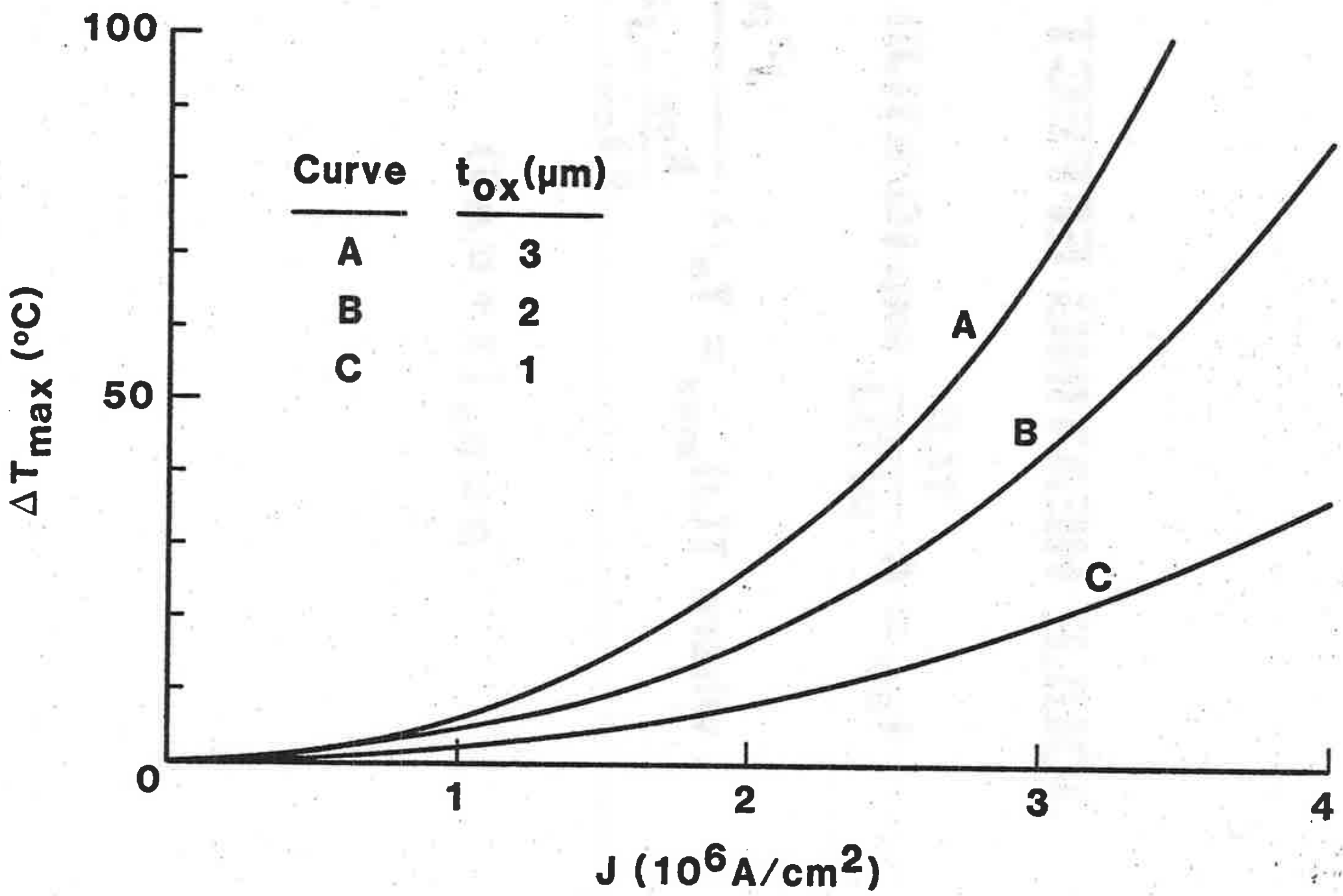
$$T_2 = C_3 \exp(\lambda_2 x) + C_4 \exp(\lambda_2 x) + C_5 \quad \text{for} \quad \ell \leq x \leq L$$

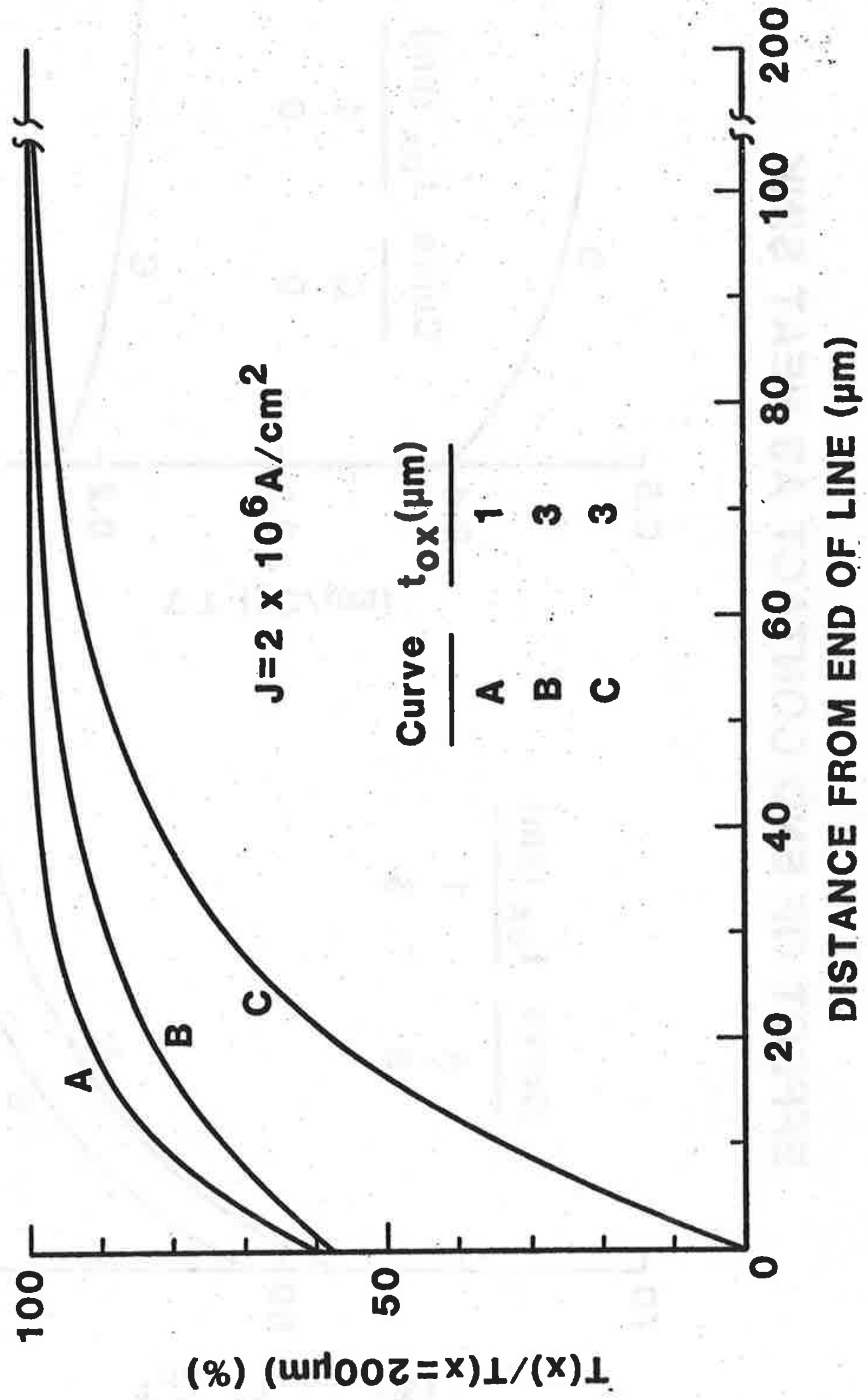
JOULE HEATING EFFECT ON t_{50}

$$t_{50} = A \frac{T(J)}{\rho(T)J} \exp\left(Q/kT(J)\right)$$

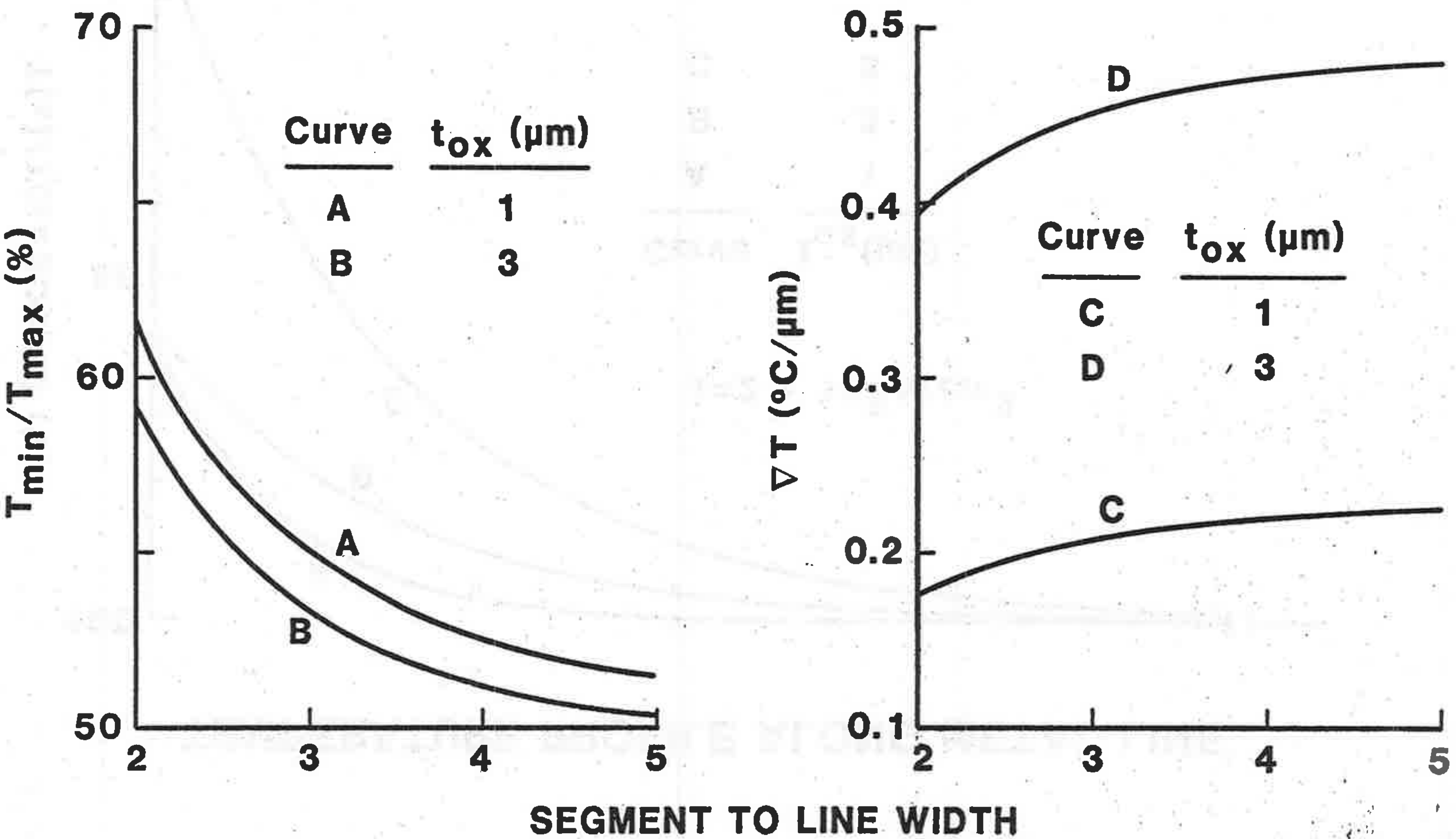
$$\text{where } T(J)_{max} = T_a + \frac{J^2 \rho_o}{\frac{k_{ox}}{t\, t_{ox}} - J^2 \rho_o \alpha}$$

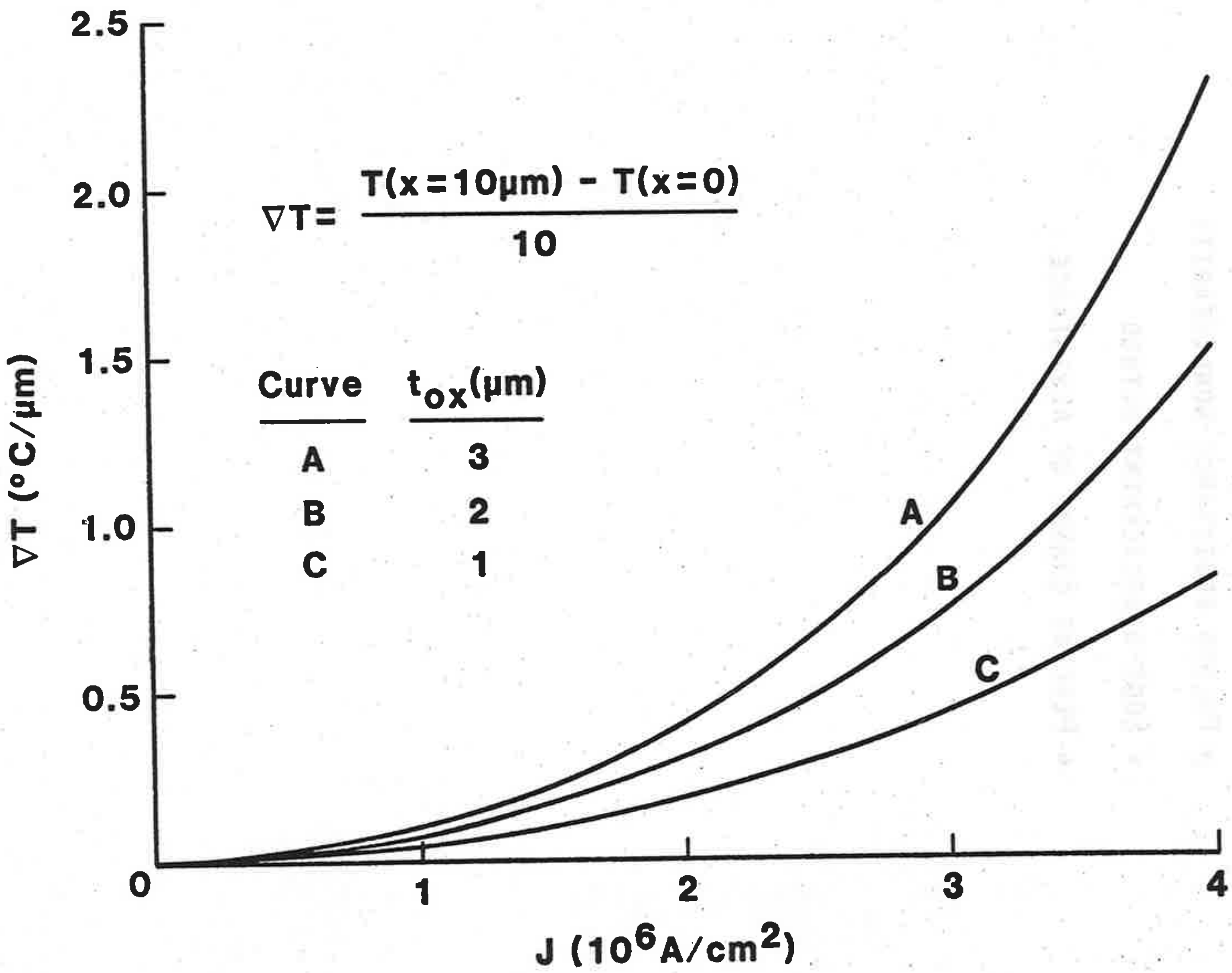
$$\rho = \rho_o (1 + \alpha \Delta T)$$


TEMPERATURE RISE DUE TO JOULE HEATING
Curve
t_{ox}(μm)
A
3
B
2
C
1
100
50
0
ΔT_{max} (°C)
1
2
3
4
J (10^6A/cm^2)
A
B
C



TEMPERATURE PROFILE ALONG METAL LINE
$J=2 \times 10^6 A/cm^2$
Curve
t_{ox}(µm)
A
1
B
3
C
3
A
B
C
T(x)/T(x=200µm) (%)
100
50
0
20
40
60
80
100
200
DISTANCE FROM END OF LINE (µm)

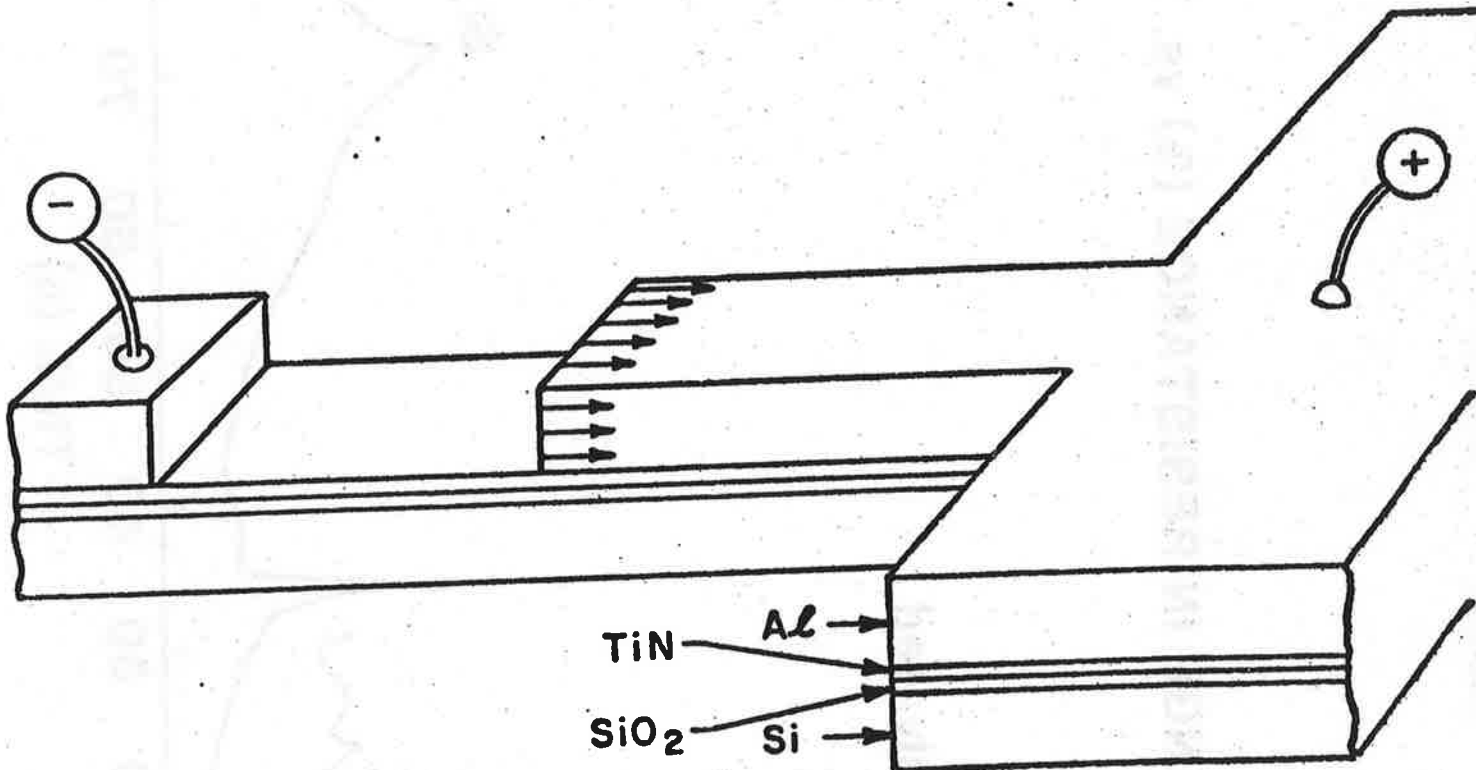

EFFECT OF END CONTACT AS HEAT SINK
Curve
t ox (μm)
A
1
B
3
T min/T max (%)
70
60
50
2
3
4
5
A
B
Curve
t ox (μm)
C
1
D
3
∇T (°C/μm)
0.5
0.4
0.3
0.2
0.1
D
C
SEGMENT TO LINE WIDTH



TEMPERATURE GRADIENT NEAR END OF TEST LINE
∇T = T(x=10µm) - T(x=0) / 10
Curve
A
B
C
t_ox(µm)
3
2
1
A
B
C
2.5
2.0
1.5
1.0
0.5
0
∇T (°C/µm)
1
2
3
4
J (10^6 A/cm^2)

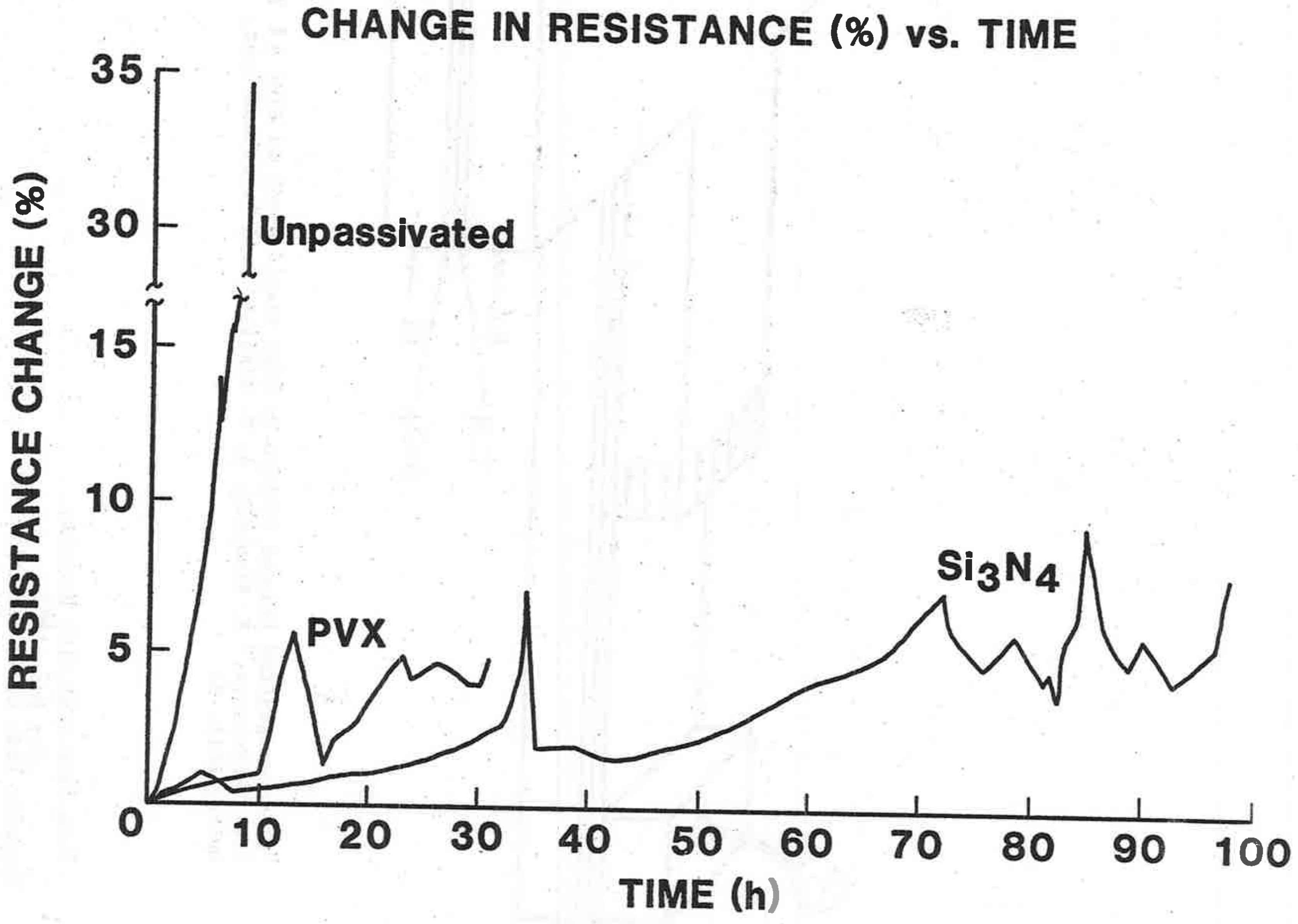
SUGGESTED PRE-INDICATORS OF FAILURE

- PULSED RESISTANCE-NONLINEARITY
- EDGE-DISPLACEMENT METHOD
- PERCENT CHANGE OF RESISTANCE



"Electromigration Induced Failure by Edge Displacement in Fine Aℓ Thin Film Conductors," E. Kinsbron, A. P. English, Bell Telephone Labs, Murray Hill, NJ

From 1982 IEEE VLSI Workshop
May 6-7, 1982
Hyannis, Cape Code, Massachusetts


CHANGE IN RESISTANCE (%) vs. TIME
RESISTANCE CHANGE (%)
35
30
15
10
5
0
10
20
30
40
50
60
70
80
90
100
TIME (h)
Unpassivated
PVX
Si_3N_4

SESSION IV DEVICE AND CIRCUIT CHARACTERIZATION

Latch-Up Test Structures and Their Characterization

W. J. Craig
IBM Corporation

"Latch-Up Test Structures And Their Characterization"

- Brief Review of Latch-Up
- Structures
- Testing
- Results
  - a. Punch Through Induced Latch-Up
  - b. Avalanche Induced Latch-Up
- Summary

W.J. Craig
D/G33 B/966-2
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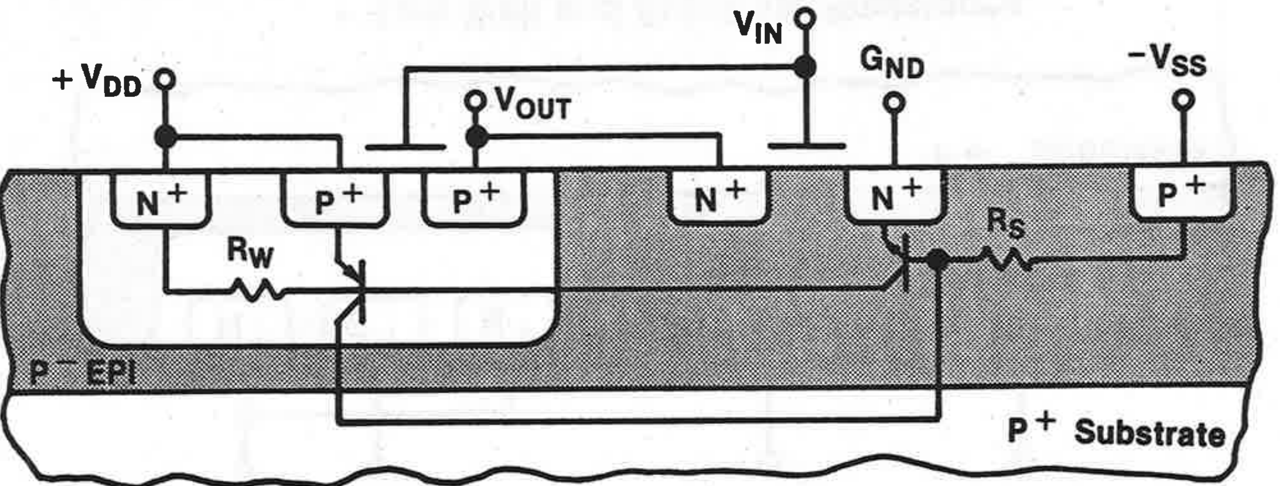
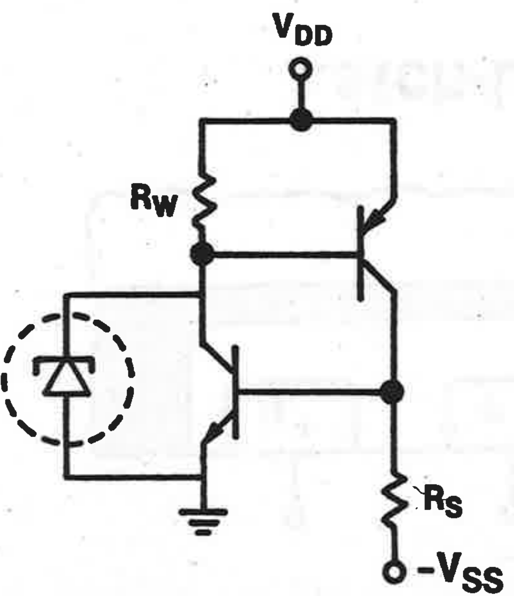
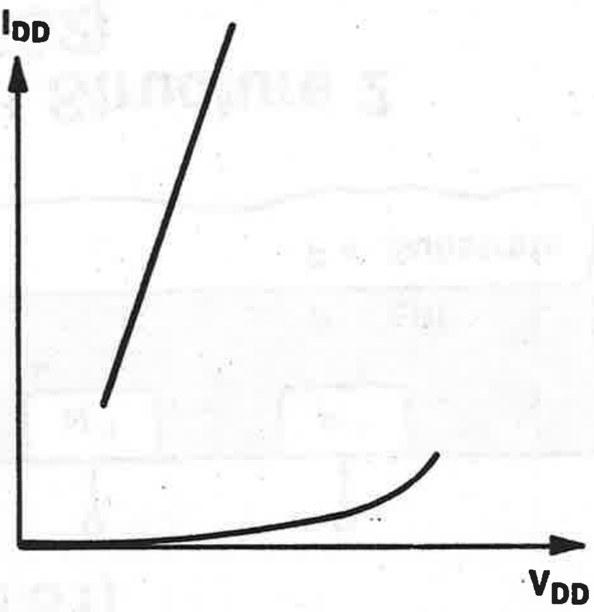
Essex Junction, Vermont 05452

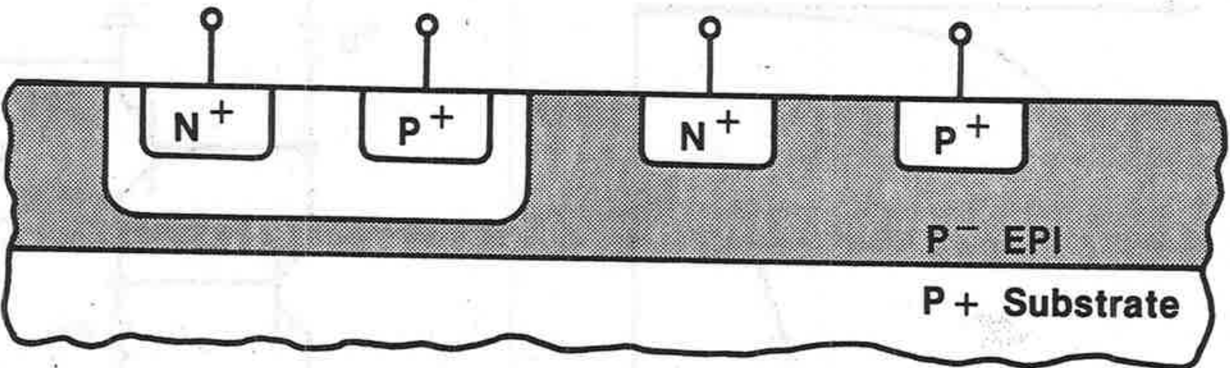
Latch-Up



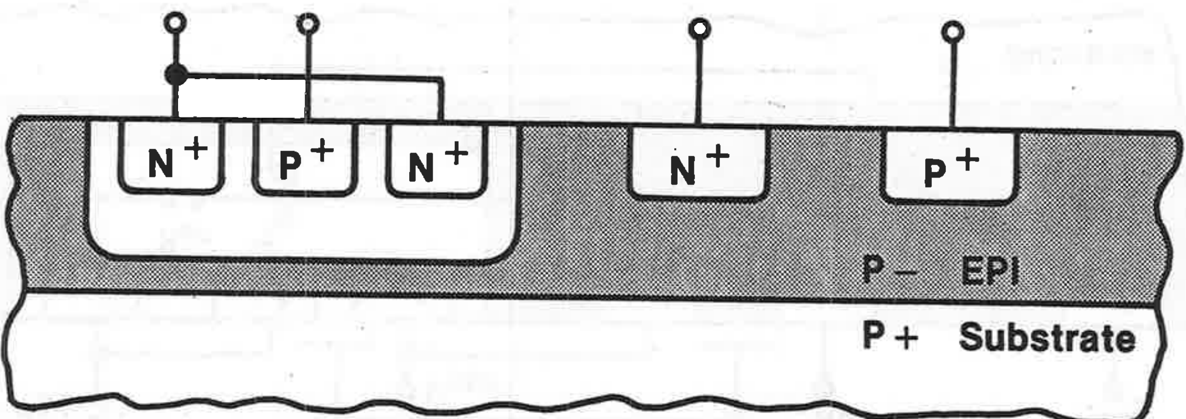




Latch-Up Test Structure 1 (LUTS1)

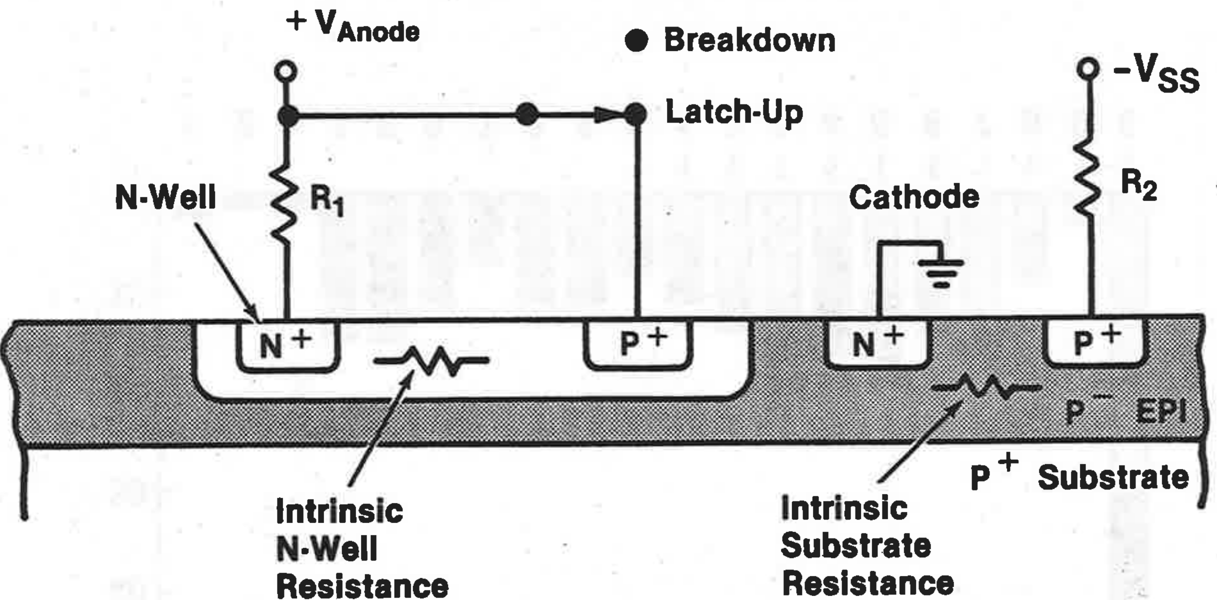


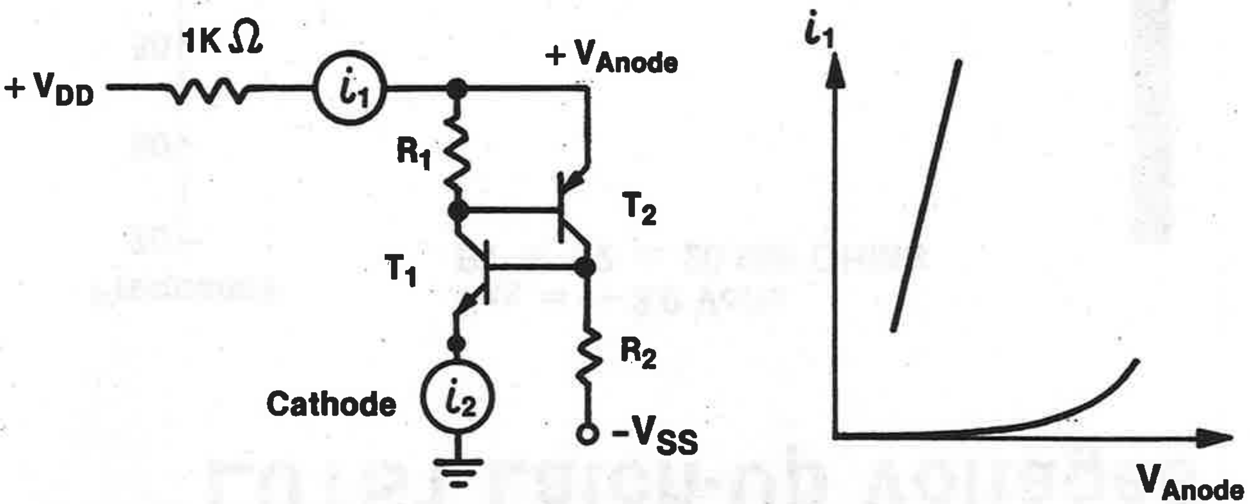
Latch-Up Test Structure 2 (LUTS2)



- Low Well and Substrate Resistance
- High Parasetic Bipolar Gain

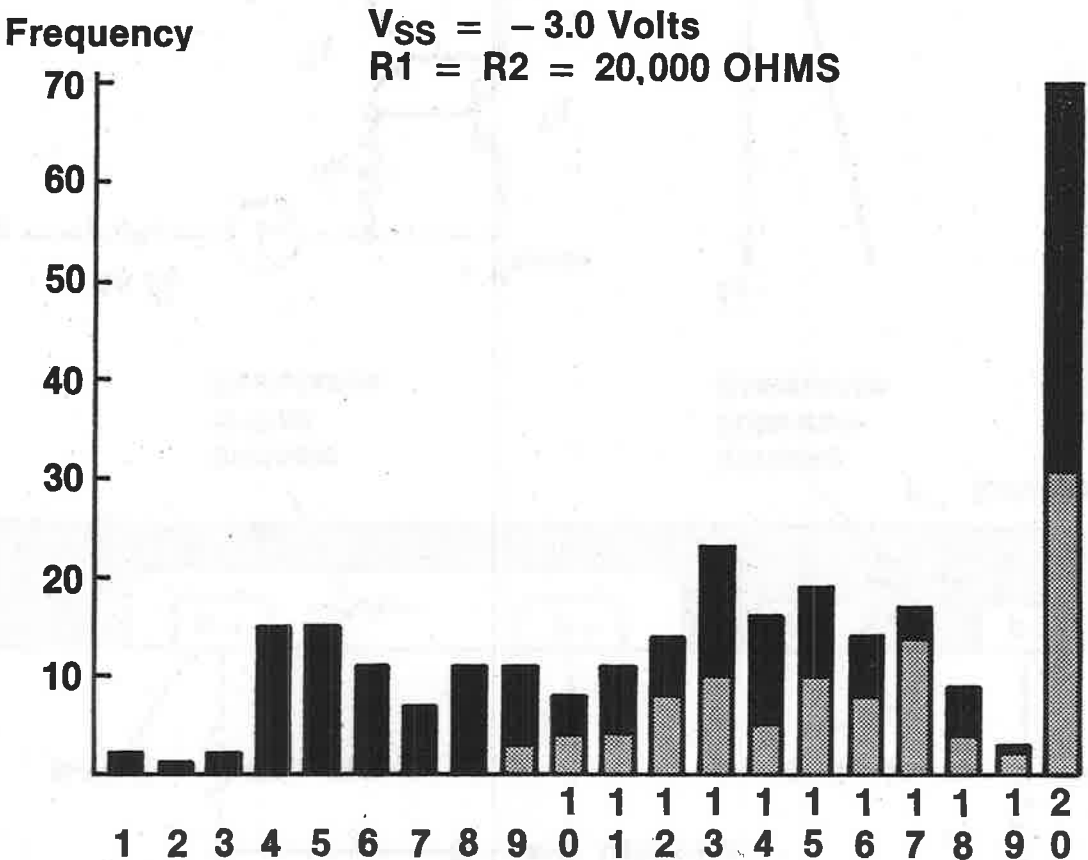
Latch-Up Test Configuration



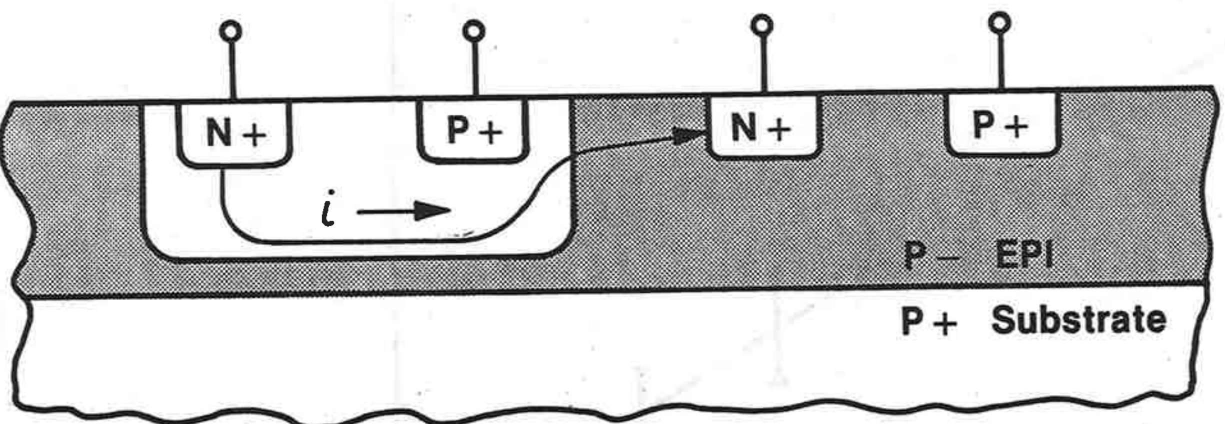


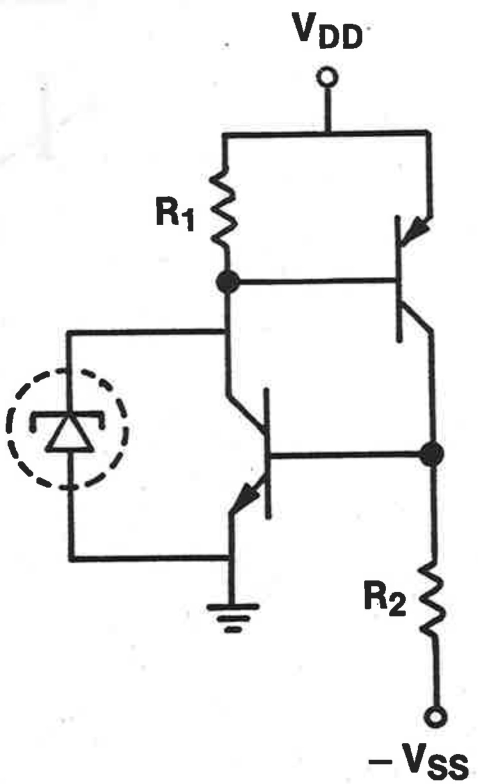
Breakdown - Open Switch
- R1 = R2 = 0.0 K Ω

LUTS1 Latch-Up Voltages

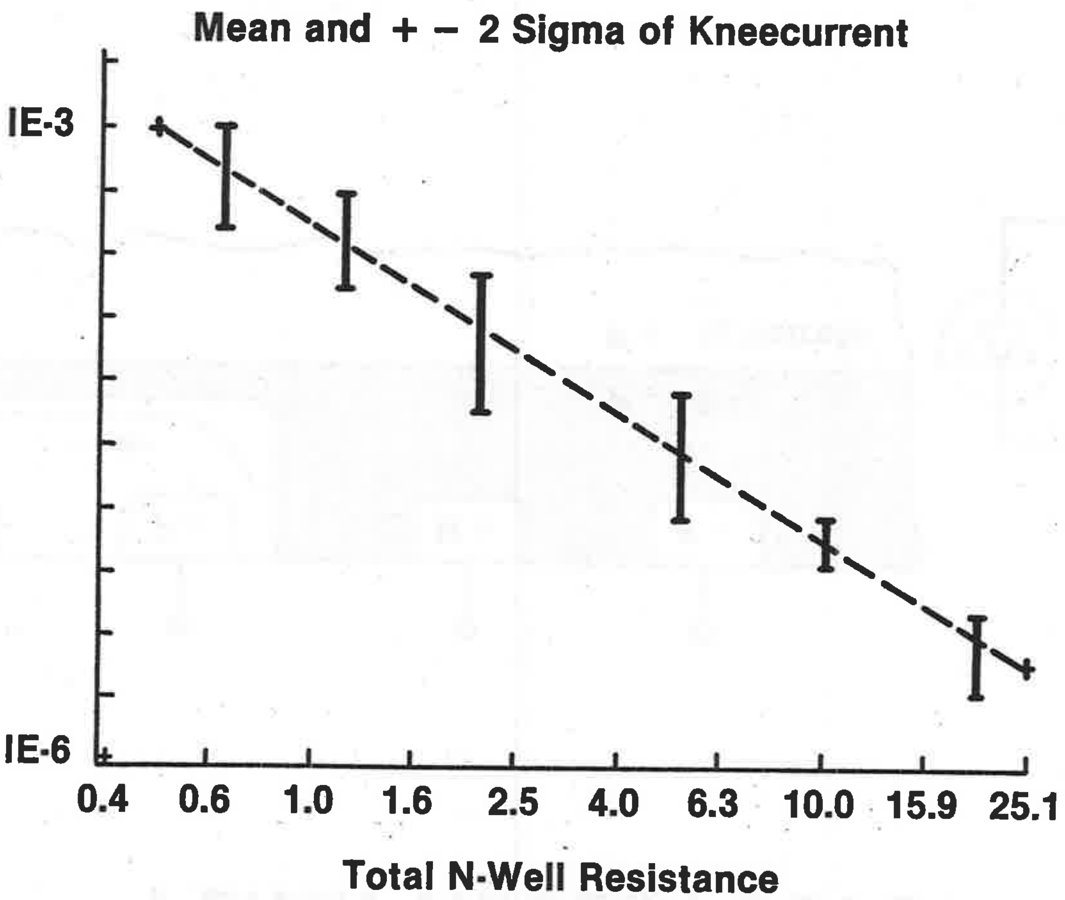


Punch Through LUTS1

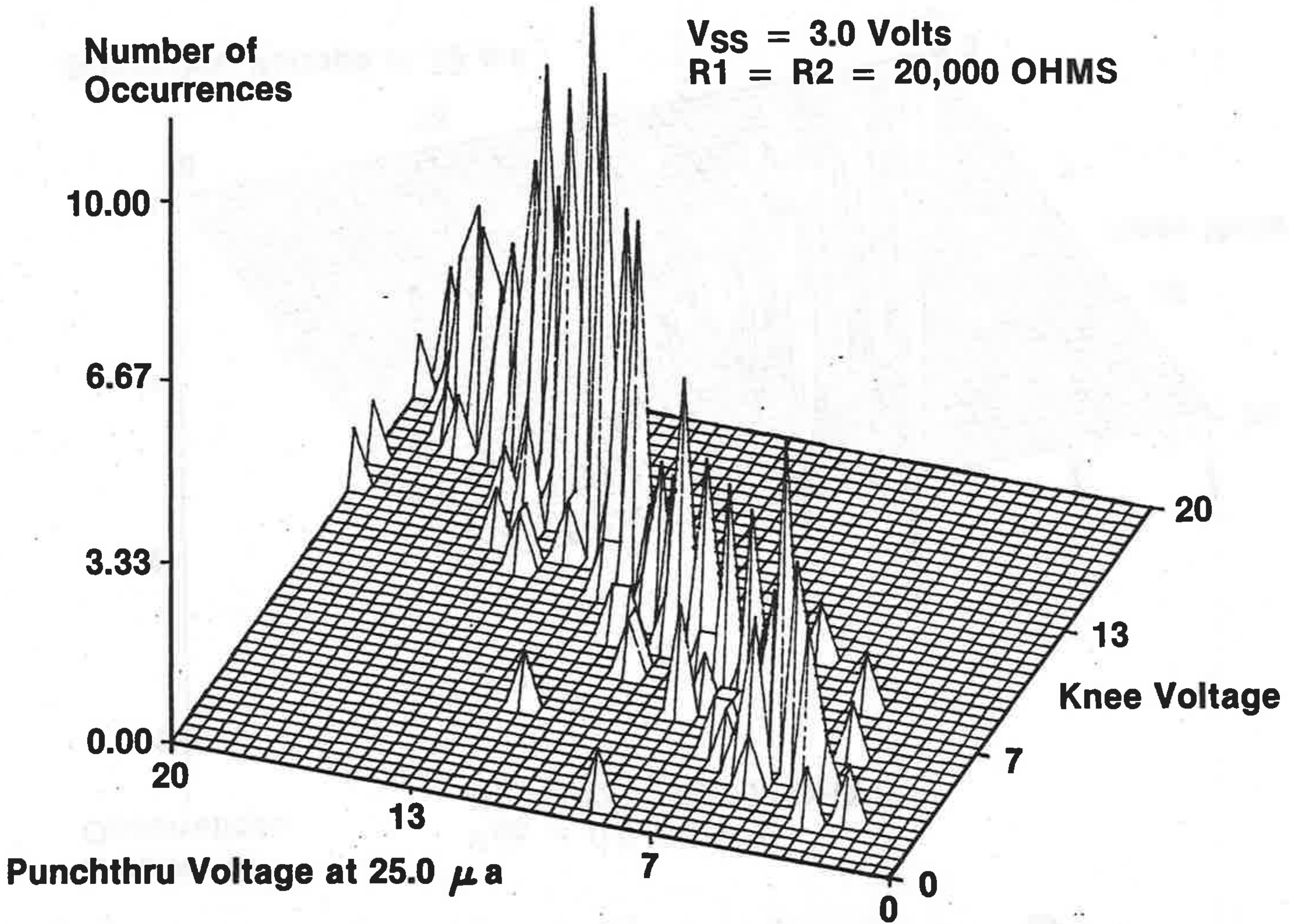




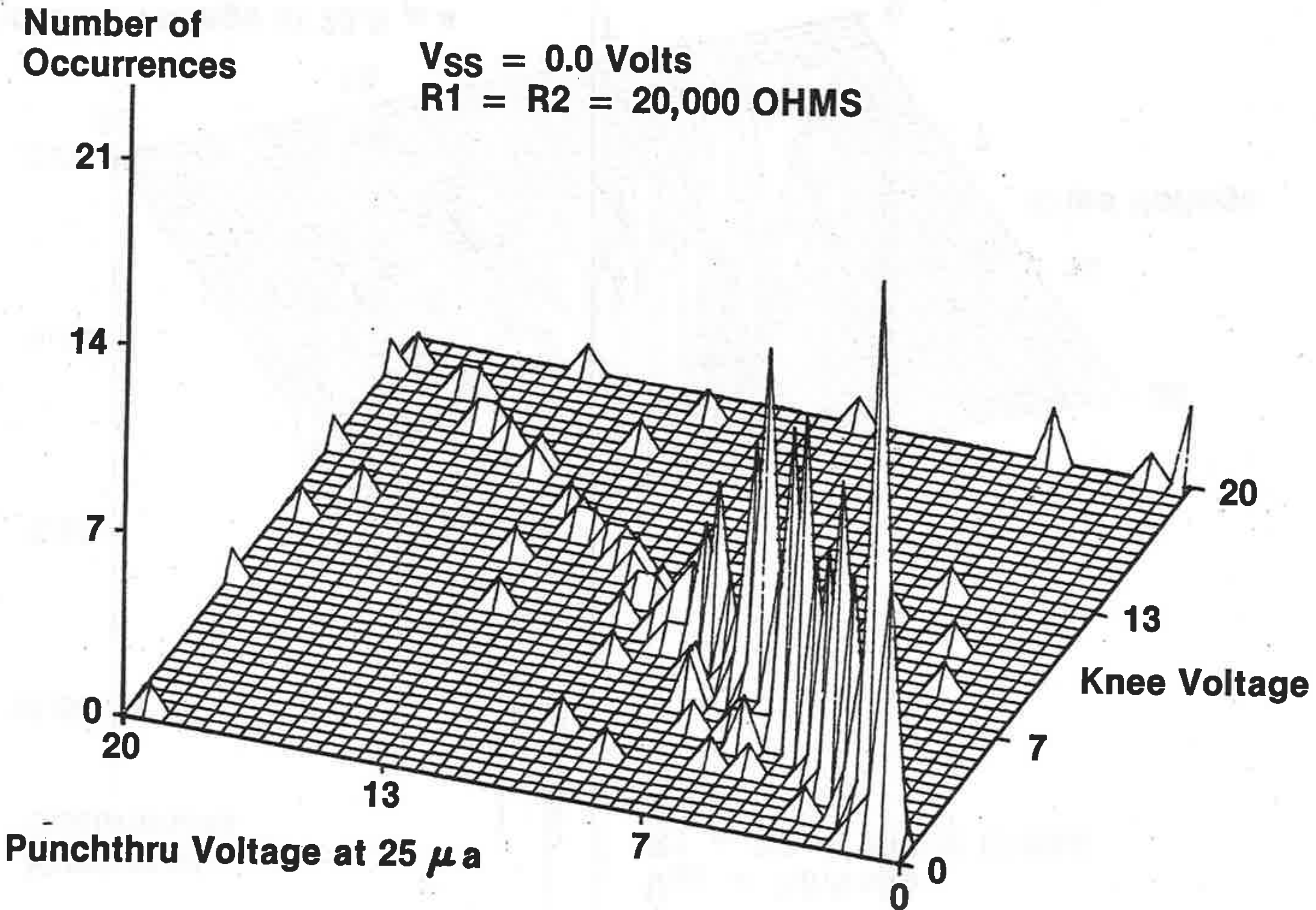
Kneecurrent as a Function of N-Well Resistance



LUTS1 Latch-Up Voltages

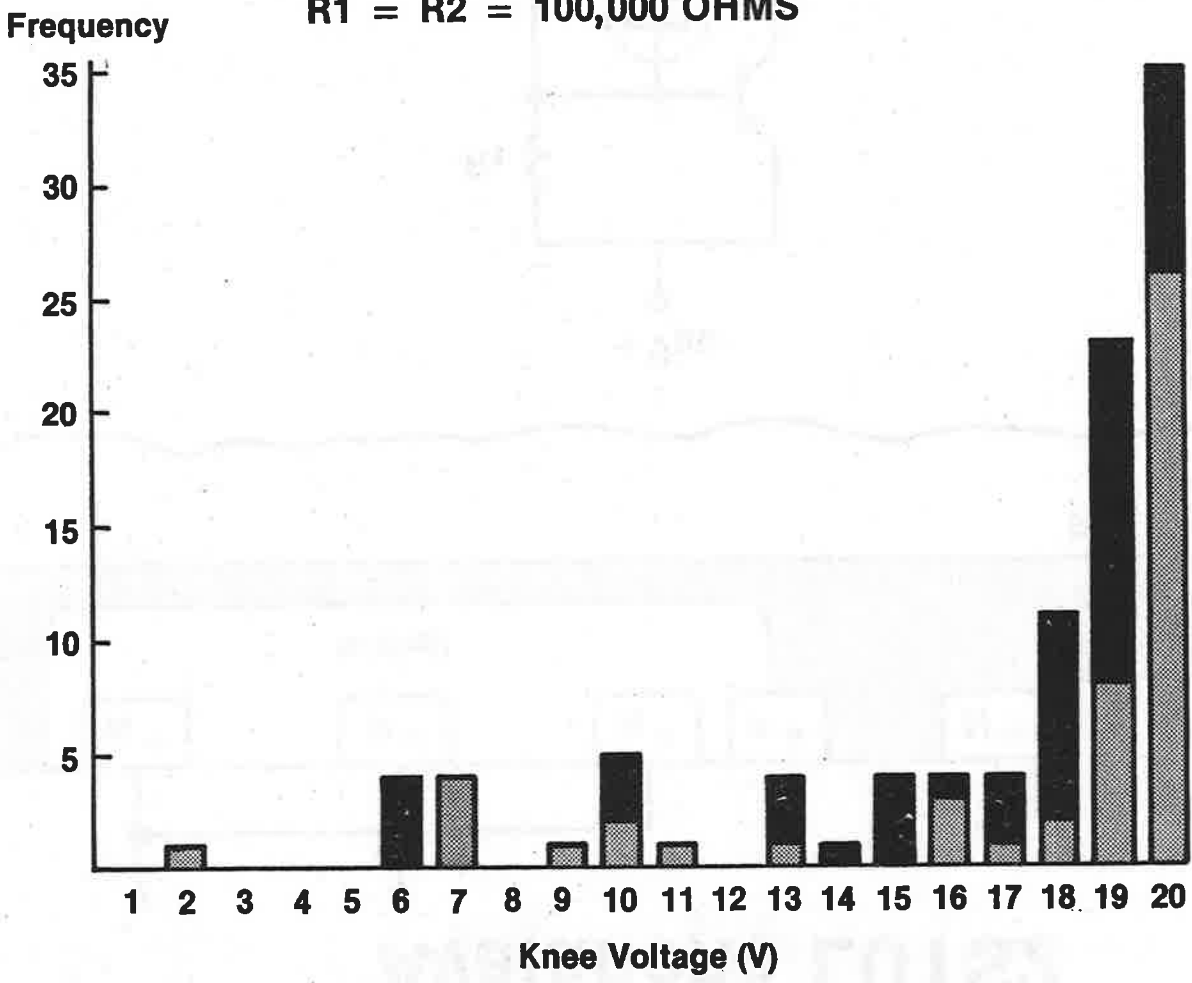


LUTS1 Latch-Up Voltages

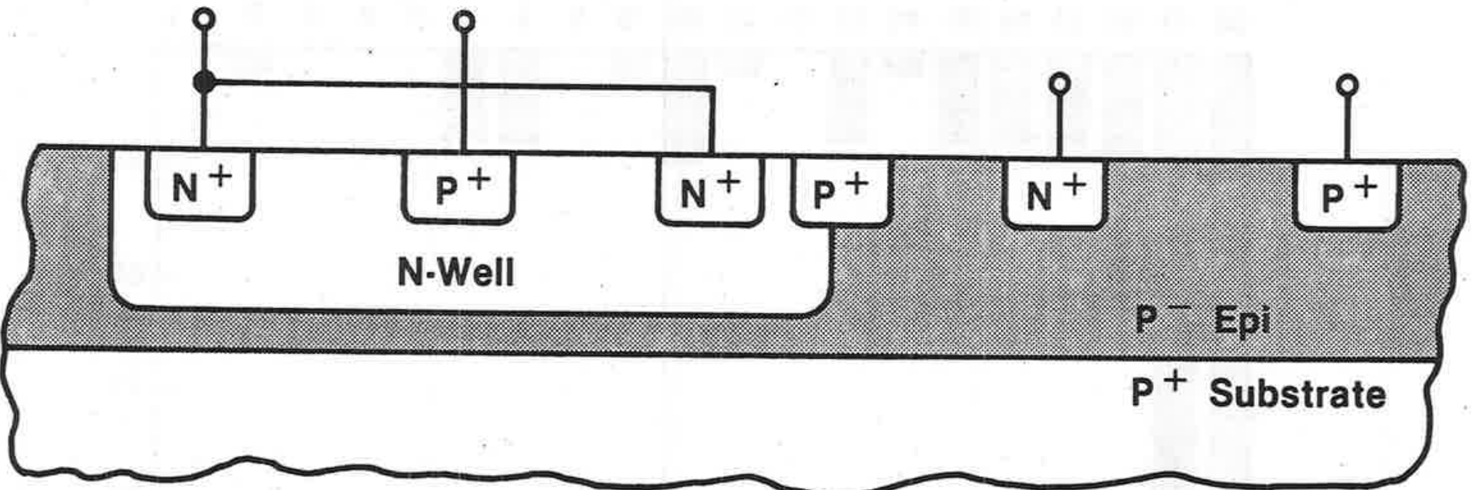


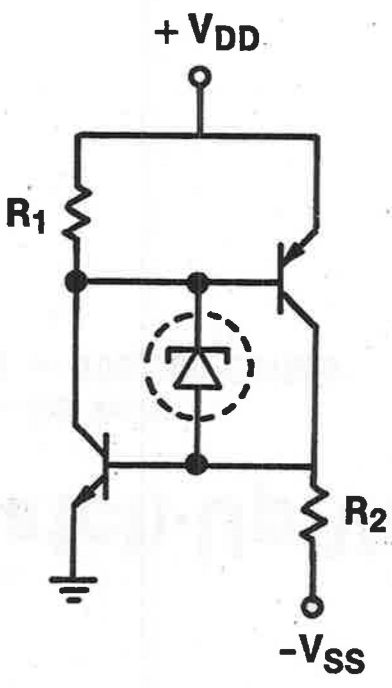
LUTS2 Latch-Up Voltages

V_{SS} = − 3.0 Volts
R1 = R2 = 100,000 OHMS

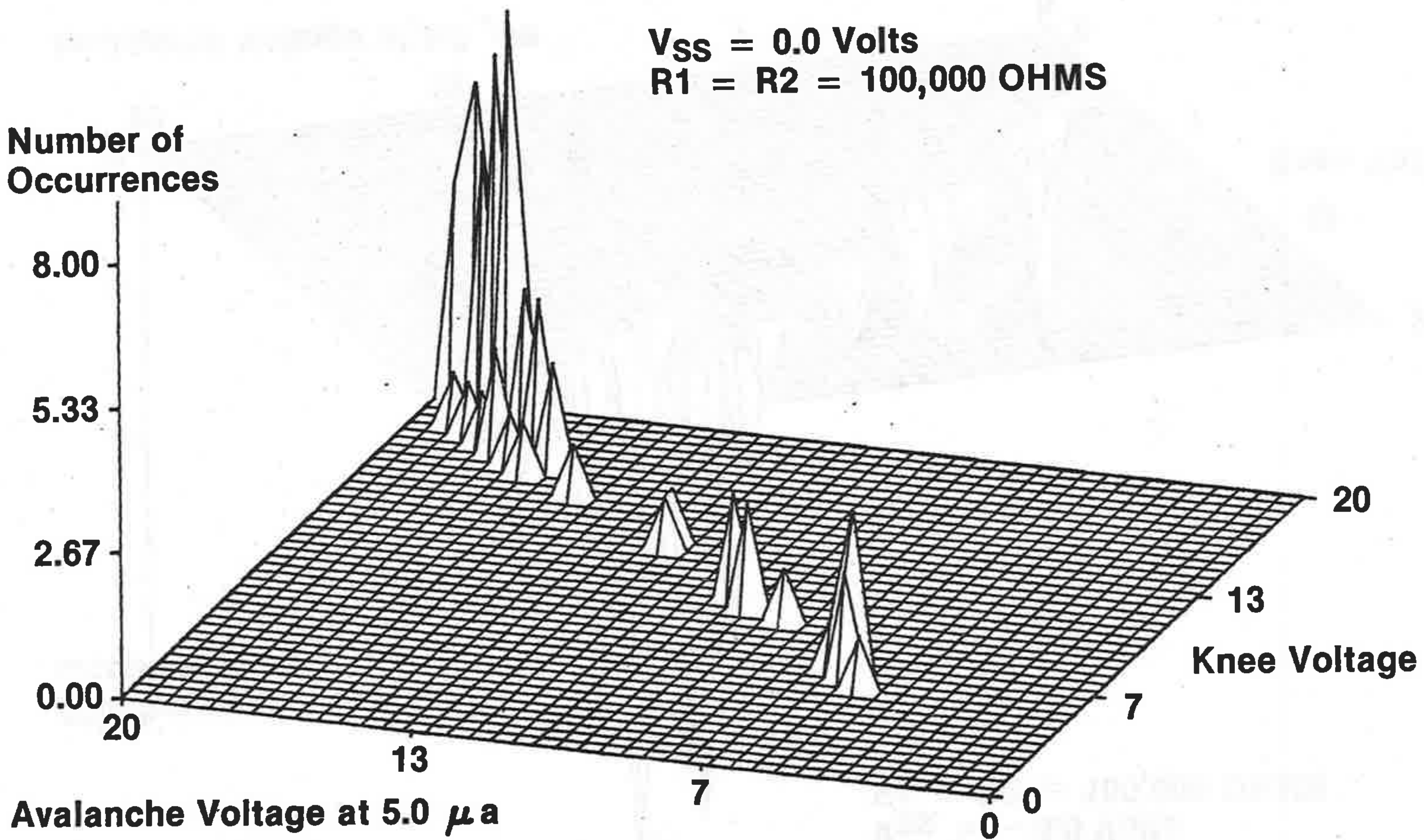


Avalanche LUTS2

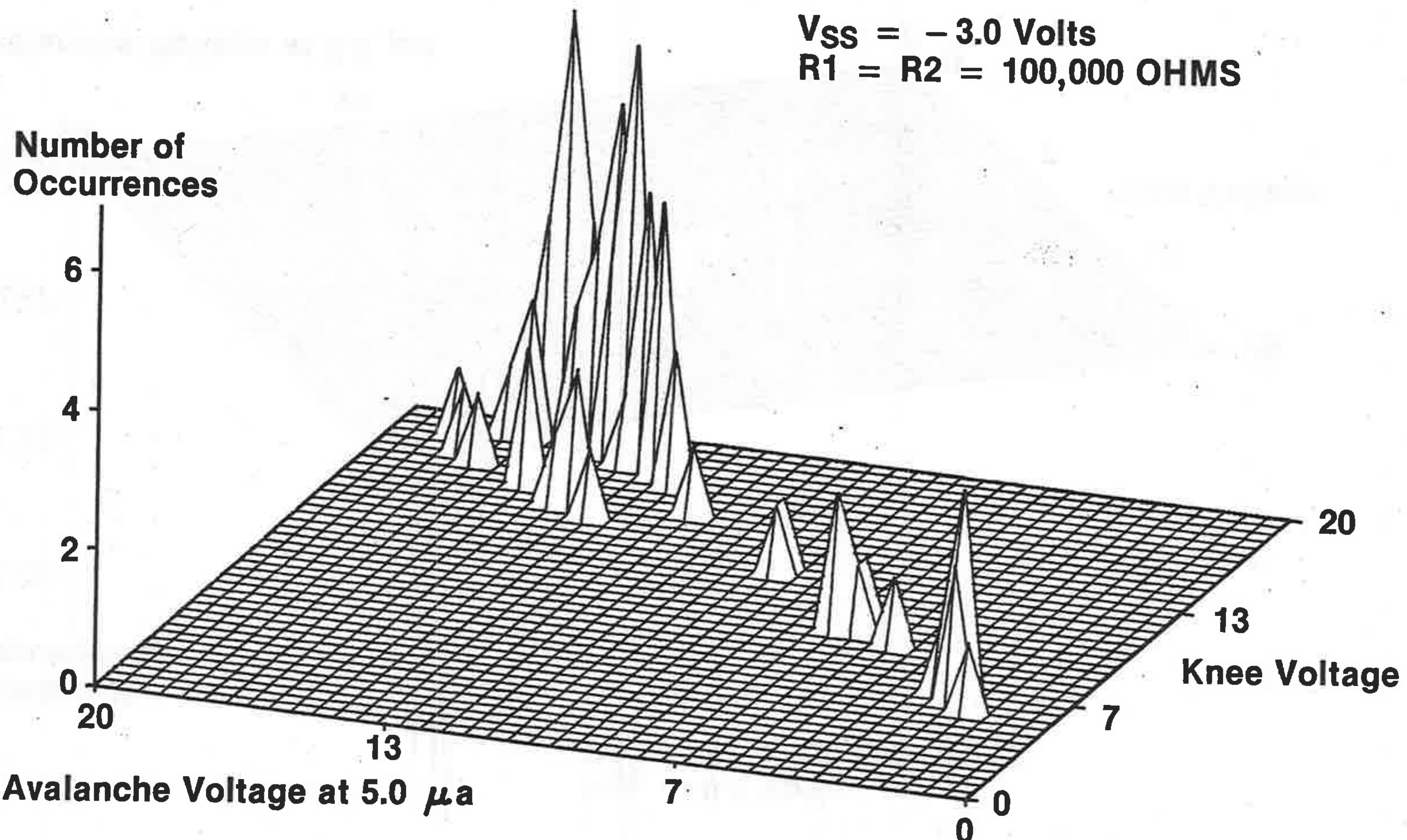




LUTS2 Latch-Up Voltages



LUTS2 Latch-Up Voltages



Summary

- Two Test Structures Specifically Designed to Test Latch-Up
- Testing Where Resistors Simulate Well and Substrate Resistance
- Precautions and Checking to Prevent Premature Latch-Up
- Two Causes of a DC Induced Latch-Up and Correlation to Punch-Through or Avalanche Current

Pre-Processor Geometry, Temperature and Parameter Modelling of Short and Narrow MOSFETS for VLSI Circuit Simulation, Optimisation and Statistics with SPICE

G. T. Wright and H. M. Gaffur
Electronic and Electrical Engineering Department
University of Birmingham

Pre-Processor Geometry, Temperature and Parameter Modelling of Short and Narrow MOSFETS for VLSI Circuit Simulation, Optimisation and Statistics with SPICE *

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University of Birmingham, Birmingham B15 2TT, England.

ABSTRACT

A parameter measurement and modelling method is described for the SPICE-2 level-3 MOSFET. Geometry dependences are modelled outside the simulator with simple polynomials which are incorporated into a pre-processor for parameter generation and circuit file construction. Operating point dependencies of threshold, body-effect and channel width are incorporated into an enhanced device model inside the simulator. The method is of general application and can be applied to any circuit simulator containing any transistor model.

1. INTRODUCTION

A major requirement for the construction and use of MOSFET models for CAD of VLSI is the provision of a sufficiently accurate but simple description of the geometry, temperature and operating point dependencies shown by many of the model parameters. A further requirement is that it should be possible to derive the model parameters themselves by straightforward measurements on a few, simple, test structures. The work to be described is based on the level-3 MOSFET model implemented in SPICE-2.[1] This is essentially the gradual-channel space-charge-limited approximation[2-6] and is a basic widely used representation.

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* This work has been described in part at the UK SPICE User Group Meetings held at Malmesbury, UK, in December 1982 and at Rutherford-Appleton Laboratory, UK, in March 1983, at the EEC Device Modelling Workshop held at Villard-de-Lans, France, in November 1983 and at the IEEE Device Modelling Workshop held at San Diego, USA, in February 1984.

Much work has been carried out and has been reported in the literature, in attempts to derive accurate, simple, closed, analytical expressions for parameter dependencies on geometry and temperature.(7-9) However, due to the essentially three-dimensional structure and complicated physical operating mechanisms of the short and narrow transistors used for VLSI circuits it is unlikely that this kind of approach will ever be successful. A practical engineering solution has been sought, therefore, by fitting simple polynomials in length and width to the parameter values obtained from measurements made at the operating temperature.

2. PARAMETER EXTRACTION

In order to use this method a satisfactory procedure for parameter extraction must be established. The interactions between parameter values are sufficient so that for any individual device there are many combinations of values which will provide a working fit to measured characteristics. It is not always clear, therefore, which are the "correct" values. If it is desired to describe device characteristics over wide ranges of length and width the procedure adopted must be capable of providing a smooth and systematic dependence of parameter values on geometry rather than the irregular variation so often obtained. It is desirable, as well, for the parameters and their values to be physically meaningful. These requirements can be satisfied by using a transistor model based on "good" physics and by a suitable sequence of measurements in which parameter values already obtained are "frozen" and used to evaluate further parameters.

The first and most basic parameters are those which determine the electrical lengths and widths of the transistors. These can be obtained from measurements of zero bias drain resistance against mask length and zero bias drain conductance against mask width.(10) MOS capacitor measurements give gate-oxide thickness and from all these results the surface-channel low-field mobility can be found. Typical sets of results for the measurement of electrical length and width are shown in Figs. 1 and 2. These were obtained on a matrix of self-aligned silicon-gate, n-channel transistors with lengths and widths on mask varying over the range from 2 to 50 micrometres. The length plots intersect as expected at the combined value of source plus drain series resistance. The width plots, however, intersect the horizontal axis at different places indicating a dependence of electrical width on gate bias. This is due to the fact that increasing gate bias inverts more of the silicon surface outward from the edges of the channel so increasing the effective channel width.

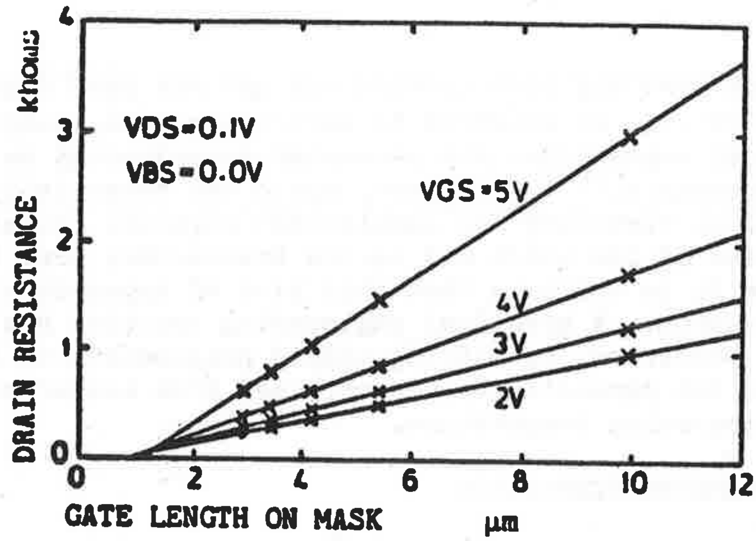

FIG.1 Drain Resistance Against Gate Length

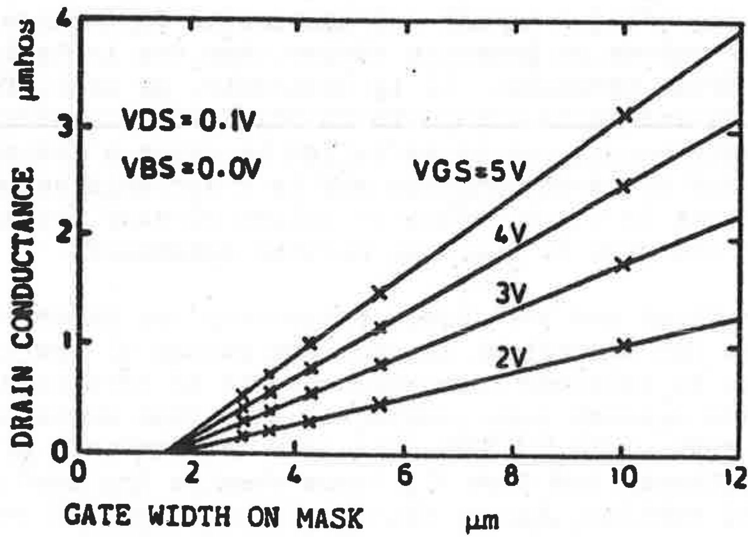

FIG.2 Drain Conductance Against Gate Width

A second group of parameters which can be measured directly and independently from gate turn on characteristics consists of the gate threshold voltage VTH, the coefficient γ for threshold dependence on substrate bias, the surface inversion potential ϕ, and the coefficient θ for the gate field reduction of surface mobility. It is well-known that VTH and γ are functions of geometry because of electrostatic end and edge fringing effects which become significant at small dimensions. This is illustrated by Fig. 3 which shows the variation of gate threshold voltage with length and width for one set of transistors used in this work.

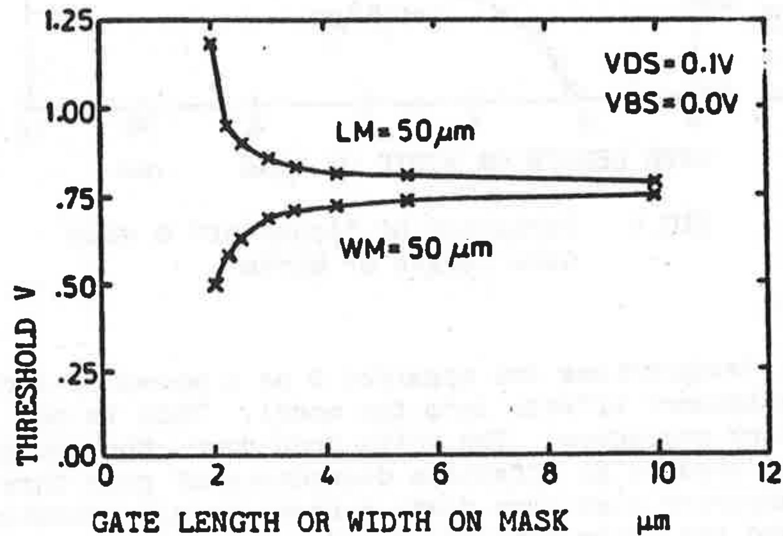

FIG.3 Variation of Threshold Voltage with Device Length or Width

However, the coefficient θ as measured also shows a dependence on geometry. This is shown in Fig. 4 in which θ is seen to rise as length falls and to fall as width falls. These variations are only apparent however; The dependence on length[11] due to the effects of source and drain series contact resistances and the dependence on width is a consequence of gate-field modulation of electrical channel width as described earlier. When these factors are taken into account the value of θ becomes constant and independent of geometry. However, the value of θ which is obtained in this way when the entire channel is virtually at source potential, is not the most suitable for use over the whole operating range. When the transistor has a significant drain voltage for example the average gate-oxide field is reduced and the effective value of θ is reduced. The optimum, average, value of θ over the full working ranges of gate, drain and substrate voltages is best

obtained in fact from the saturation characteristics of a long and wide device.

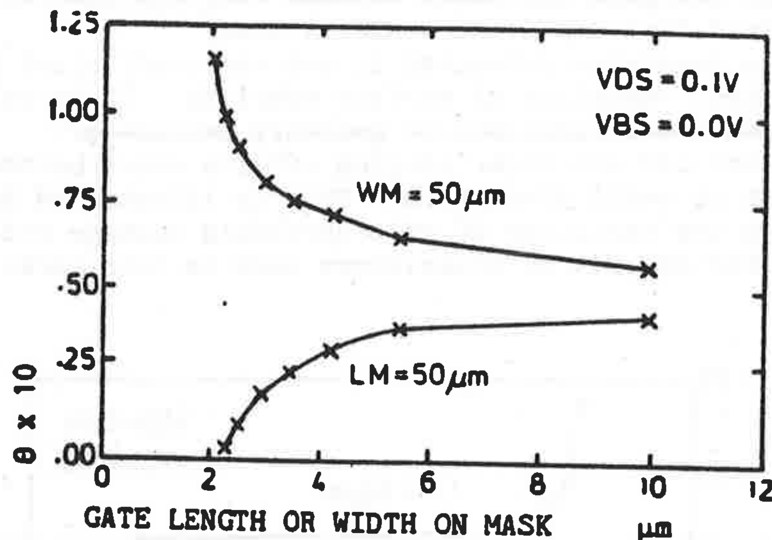

FIG.4 Variation of "Apparent" θ with Gate Length or Width

Some designers use the apparent θ as a means of including series resistance effects into the model. This is not a satisfactory procedure. The volts drop down the source resistance creates an effective dependence of gate threshold and of substrate bias upon drain current in all operating regions and the drain resistance reduces current in the triode region but has little effect in the saturation region. These effects become more noticeable and more significant as transistor dimensions become smaller. For satisfactory parameter evaluation procedures the measured characteristics of the transistor must first be corrected for source and drain resistance volts drop. If this is not done the remaining parameters, in order to compensate, show unnecessary and incorrect dependencies on geometry.

The most important remaining parameters of the level-3 model are VMAX describing drain field reduction of channel mobility, η describing drain-field modulation of the gate threshold and K describing the component of output conductance due to channel length modulation. These are intermingled in their influences upon the current-voltage characteristics of the transistor and are difficult to separate for direct measurements. The most satisfactory way to obtain them is to use least-squares curve-fitting of the full model equations to measured characteristics. With such a small number of parameters the values obtained are invariably consistent and unique.

The entire process of measurement and characterisation is carried out by an automated instrumentation system with analysis and evaluation handled by a linked, desk-top, computer system.

3. OPERATING POINT DEPENDENCE

Parameters such as gate threshold voltage, body-effect coefficient and electrical channel width vary in value as the operating point of the transistor changes. This is demonstrated by Fig. 5 which shows the dependence of gate threshold upon the square-root of substrate bias. Simple theory, based on uniform substrate doping, predicts a linear relationship between these quantities. This is not the case in practice and is a consequence of the markedly non-linear substrate doping under the surface channel caused by implantation. This is not allowed for in the level-3 model. The considerable variation of threshold shown for the narrow device is due largely to channel width modulation and this is not allowed for either.

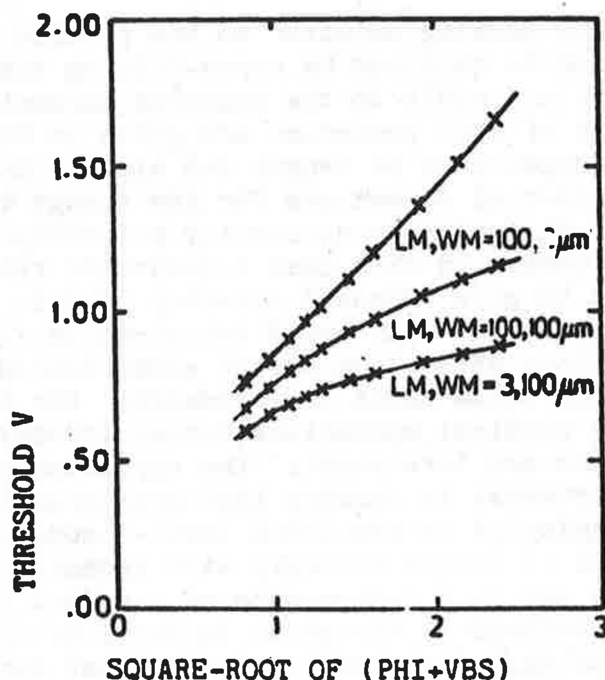

FIG.5 Threshold Voltage Against Square-Root of Substrate Bias

These mechanisms have been incorporated into the SPICE simulator by specification and use in the transistor model of three new parameters VTB, DWG and DWB.

VTB is the threshold measured at a suitable substrate bias and together with VTH and γ enable the transistor model to use quadratic fits to the measurements shown in Fig. 5. In this way the threshold

voltage of the model can be made to follow closely that of the real device. Furthermore, the body-effect coefficient γ is now determined, as it should be, by surface doping at small substrate bias and by bulk doping at large substrate bias. DWG and DWB are the coefficients of channel width dependence upon gate and substrate biases respectively.

4. GEOMETRY DEPENDENCE

Gate threshold voltage and body-effect coefficient vary in value with both channel length and width whereas VMAX, η and K vary only with channel length. Circuit simulators such as SPICE incorporate algebraic relationships of various complexities to attempt to account for the relevant physical mechanisms. This approach has not proved particularly successful, creates unnecessarily intricate models and is computationally inefficient. The problems involved in generating accurate and general analytical models will worsen as device dimensions get smaller, as physical structures become more complex and as operating mechanisms get more complicated.

A practical working solution to the problem of geometry dependencies can be obtained by curve-fitting simple polynomials in length and width to the measured parameter values. Typical results of this procedure are given in Figs. 6 and 7 for threshold dependence on length and width. Simple theory suggests a reciprocal dependence for the change in threshold with change of dimensions consequently polynomials in 1/L and 1/W have been used. In each case a quadratic relationship has been found to give adequate accuracy of fit. The corresponding results for VMAX, η and K are given in Figs. 8, 9 and 10. These latter parameters are of significance only at small dimensions below about 4 micrometre; for larger devices the associated physical mechanisms become unimportant and the parameter values are irrelevant. The variation of VMAX with length is of interest in showing that this quantity is not physically meaningful in the SPICE level-3 model. This follows because it varies strongly with geometry instead of being constant and is a consequence of the fact that current saturation is defined in the model in terms of the low-field, rather than the high-field mobility. In most cases it has been found that linear or quadratic polynomials give sufficiently accurate results, particularly if these are combined with simple functional relationships suggested by elementary theory.

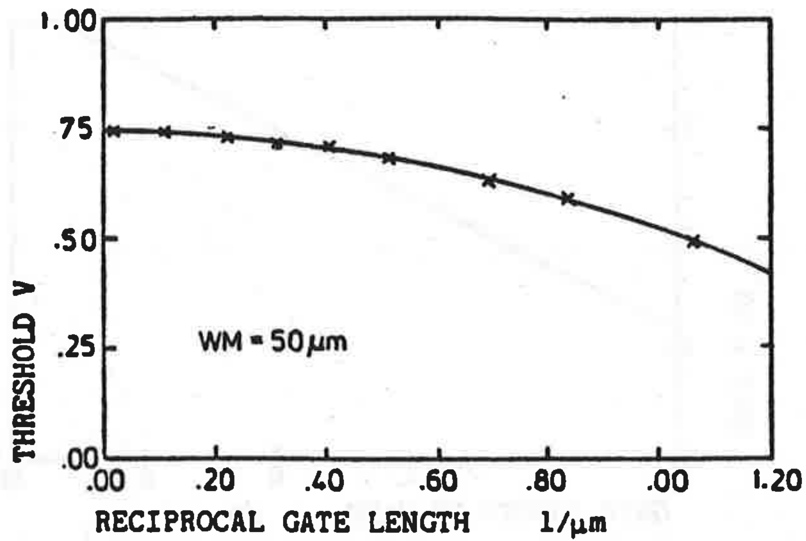

FIG.6 Threshold Voltage Against Reciprocal of Device Electrical Length.
Least-Squares Fit with Simple Quadratic

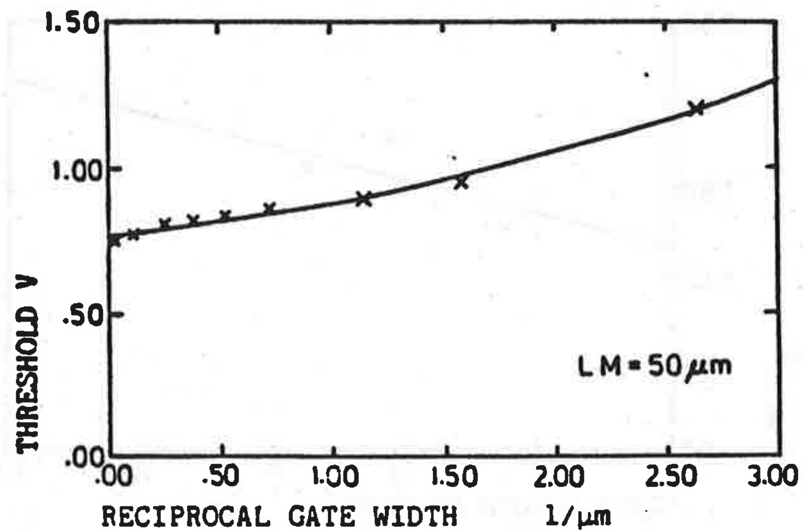

FIG.7 Threshold Voltage Against Reciprocal of Device Electrical Width.
Least-Squares Fit with Simple Quadratic

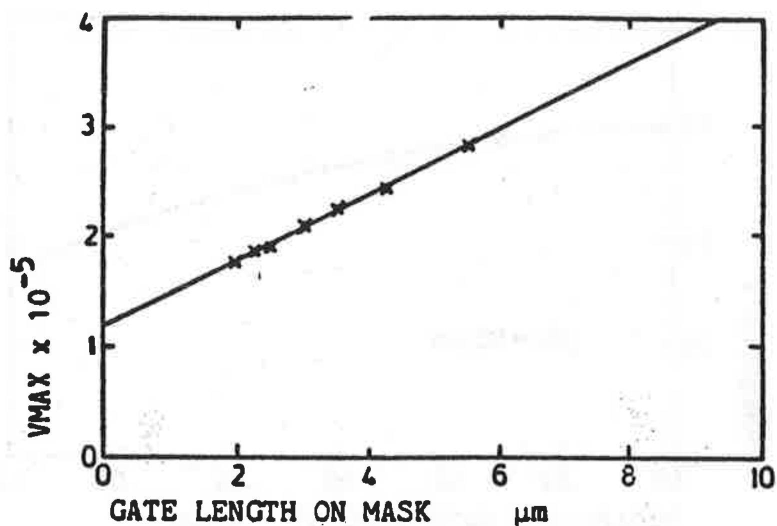

FIG.8 Variation of VMAX with Device Length for SPICE 2G.5 NMOS Level-3 Model. Least-Squares Fit with Straight Line.

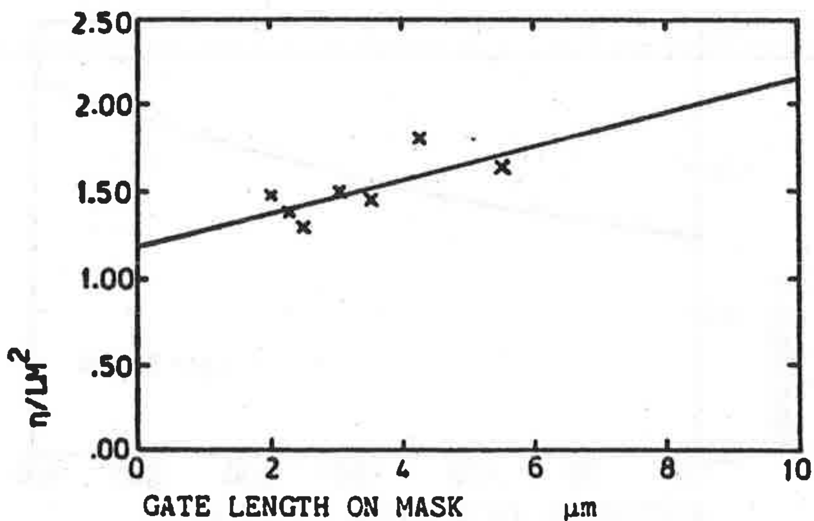

FIG. 9 Variation of η with Device Length for SPICE 2G.5 NMOS Level-3 Model. Least-Squares Fit with Straight Line.

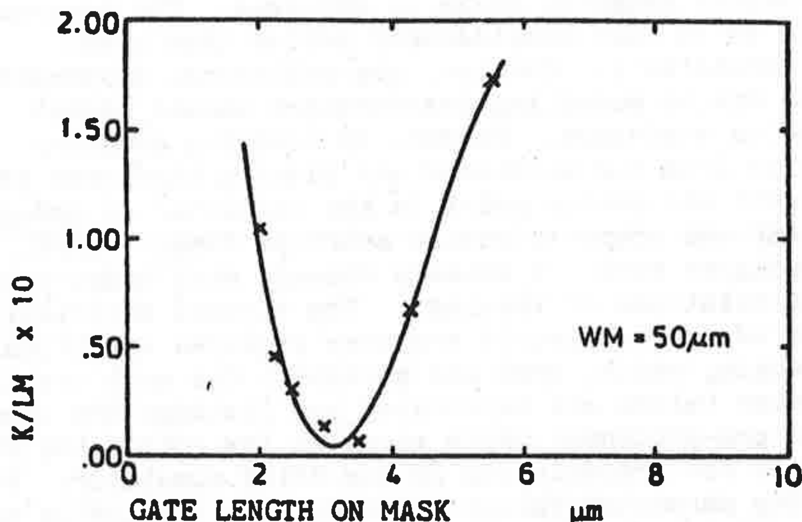

FIG. 10 Variation of K with Device Length for SPICE 2G.5 NMOS Level-3 Model. Least-Squares Fit with Cubic Polynomial.

5. PRE-PROCESSOR PARAMETER MODELLING

In order to use these results for circuit analysis and design it is necessary to make them available to the circuit simulator. If the circuit fabrication process has been established and is to be used for a considerable time then the simplest procedure is to insert the several polynomial equations into the model sub-routines of the simulator and omit the associated parameters from the circuit input file.

A more flexible and useful method is to incorporate the polynomial equations into a pre-processor which will generate the desired parameter values when required. This has been done as part of the present work. The pre-processor is constructed in FORTRAN and accepts as input any circuit file written in standard SPICE format. It reads the circuit file, calculates the entire parameter listings for each different transistor and then constructs the complete circuit file containing all parameter values for presentation to the SPICE simulator. By using these procedures a single set of parameter equations has provided a model fit of the order of 1% (average root-mean-square residual) over the range of transistor dimensions from 2 to 50 micrometres on mask in both length and width.

This methodology has several very useful advantages. First, for any given transistor model and for any given process the most accurate possible characterisation over the widest possible geometry range is obtained. The accuracy achievable is in fact considerably better than batch to batch consistency. However, any additional systematic variations due to modelling inaccuracies should always be reduced to a minimum. Second, by removing geometry dependencies from the simulator and placing them into the pre-processor the device model in the simulator is reduced to its simplest and computationally shortest form. Third, the circuit designer need not concern himself with model parameter values, calculations or listings. The circuit description file prepared by the circuit engineer requires specification of only length, width, area and periphery for each transistor; all parameter values are calculated and listings are constructed by the pre-processor which gives as its output the full circuit file for presentation to the SPICE simulator. Fourth, by measuring parameter values sequentially, physically meaningful "correct" values are obtained. This is important for reliable feedback to device designers and to process engineers. Finally, the principle outlined is completely general and can be applied to any simulator containing any model for any fabrication process.

The use of a pre-processor to carry out parameter modelling external to the circuit simulator itself improves the task of circuit analysis and design in several ways. For example, it is relatively easy and straightforward to examine the effects of parameter variation upon circuit performance. The desired changes are inserted once only into the pre-processor and this then implements the changes throughout the entire circuit description file. Further, the pre-processor and the simulator can be incorporated into an iterative loop to automatically adjust device dimensions and/or parameter values to converge on a desired circuit response or to optimise any desired aspect of circuit performance. Alternatively a cyclic loop can be used to step through a pre-determined sequence or to step through and examine the consequences of individual faults, or failures. The use of the pre-processor to examine yield statistics arising from process variations is shown in Fig. 11. This shows the statistics of propagation delay for an enhancement-depletion inverter stage caused by variations in channel length, channel width, oxide thickness and flat-band voltage. For purposes of demonstration these parameters have been assumed to have independent, normal, frequency distributions with quartiles in each case as shown on the diagram. In order to obtain these results the pre-processor and the SPICE simulator were incorporated into a cyclic loop together with routines to generate random numbers, to read and analyse the SPICE output and to store and plot the desired results. A full statistical analysis of this

kind is computationally lengthy of course particularly if a large circuit is being examined and might not often be justified. Nevertheless, the facility exists as and when needed.

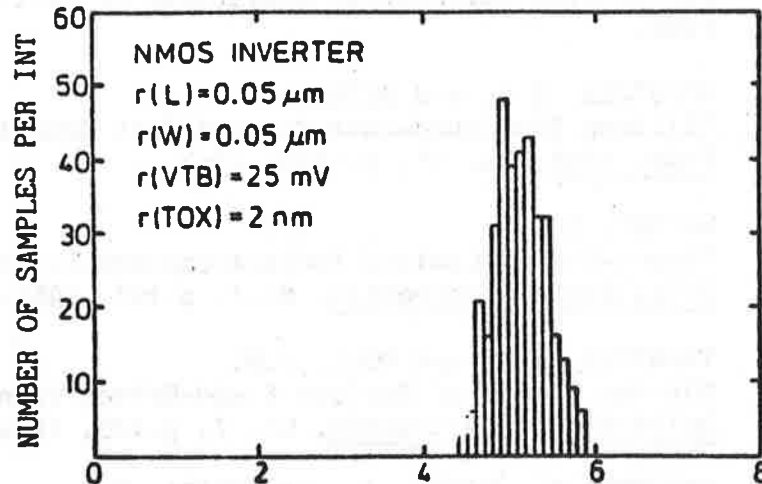

FIG. 11 Spread of Inverter Rise Times Due to Spreads of Parameter Values. Generated by SPICE 2G.5 with Statistical Parameter Pre-Processor.

6. CONCLUSIONS

A parameter measurement and extraction procedure has been described for the SPICE-2, level-3 MOSFET which provides accurate and reliable values. It has been shown that geometry dependencies can be modelled straightforwardly over wide ranges of length and width by simple polynomials. The use of a pre-processor to model parameter values outside the circuit simulator has been demonstrated. This enables the transistor model itself to be reduced to its simplest and computationally shortest form, eliminates the task of parameter listing for the circuit designer and provides a means for automatic circuit optimisation, reliability studies and yield statistics.

7. ACKNOWLEDGEMENTS

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