38th IEEE ICMTS

2026 IEEE 38th
International Conference on Microelectronic Test Structure

FINAL PROGRAM

Mar 23-26, 2026

Kunibiki-Messe, Matsue, Shimane, Japan

https://icmts.net/2026/index.html

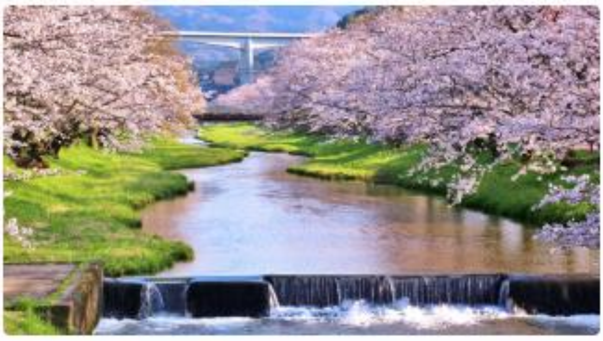
Sponsored by:
Association for Promotion of Electrical, Electrical and Information Engineering

Technical Sponsored by:
The IEEE Electron Devices Society

In cooperation with
Systems Design Lab (d.lab) Platform Device Research Division, School of Engineering, the University of Tokyo

2026 IEEE International Conference on Microelectronic Test Structure

Mar 23-26, 2026
Matsue, Japan



CHAIRMAN'S LETTER

On behalf of the steering and technical program committees, I am honored to welcome you to the **38th International Conference on Microelectronic Test Structures (ICMTS 2026)**, which will be held from **March 23 to 26, 2026**, at **Kunibiki Messe in Matsue, Shimane, Japan**.

ICMTS has a long tradition of bringing together designers and users of test structures to share recent developments and explore future directions. This year's conference continues that tradition with a **one-track program**, ensuring focused discussions and ample opportunities for networking during convivial breaks.

The technical program will feature sessions on topics such as **design methodologies, measurement techniques, reliability testing, variability analysis, and emerging applications** including advanced memory, power devices, 3D integration, MEMS, and photonic devices. In addition, we will explore the use of **machine learning and AI in data analysis**, reflecting the evolving needs of the semiconductor industry.

As in previous years, the conference will be preceded by a **tutorial short course**, offering fundamentals and advanced updates on test structure design, measurement, and analysis. An **equipment exhibition** will also be held, showcasing the latest tools and solutions from leading experts.

Matsue, known as the "City of Water," offers a unique cultural experience with its scenic beauty, historic Matsue Castle, and views of Lake Shinji. March is an ideal time to enjoy the early signs of spring in this picturesque region.

We look forward to welcoming you to Matsue for ICMTS 2026 and hope you will enjoy both the technical program and the cultural richness of this beautiful city.

Sincerely,

Yuzo Fukuzaki
General Chair, ICMTS 2026

ICMTS2026 Schedule At A Glance

Tutorial

Monday, March 23	
08:55	Tutorials Welcome
09:00	Tutorial 1
09:50	Tutorial 2
10:40	Break
11:00	Tutorial 3
11:50	Lunch
13:20	Tutorial 4
14:10	Tutorial 5
15:00	Break
15:20	Tutorial 6
16:10	Tutorial 7
17:00	Close of Tutorials
17:30	Welcome Reception for All ICMTS Attendees
19:30	Close of Welcome Reception

Technical

Tuesday, March 24	
09:00	Open Remarks
09:10	Session 1: Circuits for Test and Computation
10:30	Break
10:50	Session 2: AI and Machine Learning
12:10	Lunch
13:10	Session 3: Device Characterization
14:50	Break
15:10	Exhibitor Presentation
15:50	Session 4: Process Characterization
16:50	End of Day 1

Wednesday, March 25	
09:00	Invited Talk 1
10:00	Session 5: MEMS and Sensors
11:00	Break
11:20	Session 6: Memory
12:40	Lunch
14:00	Session 7: Reliability
15:20	Break
15:40	ICMTS 2027 Presentation
15:50	Session 8: ESD
16:50	End of Day 2
17:30	Banquet
21:00	Close of Banquet

Thursday, March 26	
08:45	Invited Talk 2
09:35	Session 9: Cryogenics
10:35	Break
10:50	Session 10: Power Devices
12:10	Best Paper Award, Closing
12:20	Excursion
17:10	Close of Excursion

Tutorials

March 23

08:30 **Registration Desk Opens**
08:55 Tutorials Welcome
Takayuki Mori (Tutorial Chair), *Kanazawa Institute of Technology*

09:00 **Fundamentals of Test Structures and Measurement**
Stewart Smith, *The University of Edinburgh*

ABSTRACT: William Thomson (Lord Kelvin) made many statements applicable to measurement as well as having his name applied to test structures and measurement techniques widely used by ICMTS attendees. Whether or not he actually said “If you can not measure it, you cannot improve it” is unclear but it definitely applies to the field of microelectronic test structures. This tutorial will begin with a short review of test structures detailing their history and hot topics over the past 40+ years. Test structures, instrumentation and measurement techniques for the resistive, capacitive and active devices will be introduced and discussed, as well as some of the measurement issues you may encounter.

Biography: Stewart Smith received the B.Eng. degree in Electronics and Electrical Engineering in 1997 and the Ph.D. degree in 2003 from the University of Edinburgh, Scotland, UK. He has published papers at almost every ICMTS conference from 1999 onwards and received the best paper award at ICMTS 2004 (Awaji, Japan). He joined the ICMTS Technical Committee in 2011 and currently serves as a Steering Committee member. Stewart is a Senior Lecturer in Electronics with the School of Engineering at the University of Edinburgh and a member of the Research Institute for Bioengineering. His research interests include development of microsystems and sensor technology for biomedical applications, integration of novel technologies with CMOS and test structures for microsystem fabrication processes.

9:50 **Device and Process technologies for advanced logic semiconductor**
Masaharu Kobayashi, *The University of Tokyo*

ABSTRACT: High performance computing enabled by semiconductor integrated circuits is the infrastructure for AI technologies. Recent advancement of generative AI technologies demand high computing performance than ever before. On the other hand, power composition accompanied by AI technologies becomes the challenge for sustainable society. Scaling of the semiconductor technology is expected to contribute to higher performance and lower power computing. In this presentation, I will overview the device and process technologies in advanced logic semiconductor, which will be the key for tackling the challenges.

Biography: 2010 Stanford University, Ph.D, 2010-2014 Research Staff Member, IBM Watson Research Center, 2014 Associate professor, Institute of Industrial Science, The University of Tokyo, 2019 Associate professor, d.lab, School of Engineering, The University of Tokyo, 2025 Professor, Institute of Industrial Science, The University of Tokyo, Dr. Kobayashi is focusing on transistor and memory technologies for energy-efficient computing. He serves as a committee member for IEDM and VLSI Symposium. He was involved in the foundation of Rapidus Corporation, where he is currently an advisor.

10:40 Break

11:00 **Advanced Packaging Technologies Enabling Chiplet-Based Systems**

Fumihiro Inoue, *Yokohama National University*

ABSTRACT: The rapid growth of cloud AI has driven extreme requirements for compute density, memory bandwidth, and energy efficiency, exposing the physical and economic limits of monolithic system-on-chip (SoC) scaling. Chiplet-based architectures have therefore emerged as a scalable integration approach, enabling functional partitioning and heterogeneous system design. In this context, advanced packaging technologies, particularly hybrid bonding, play a central role. Hybrid bonding provides ultra-fine-pitch, low-resistance interconnects with energy efficiency approaching on-die wiring, making it a key enabler for tightly coupled logic–memory integration and high-performance AI systems. This tutorial introduces advanced packaging technologies with a focus on hybrid bonding for chiplet-based integration. Core concepts of 2.5D and 3D integration are outlined, followed by discussion of hybrid bonding processes, design considerations, and reliability challenges. The impact of bonding technology on power delivery, thermal management, and system scalability is examined through examples from cloud AI accelerators. The tutorial also extends the discussion from cloud AI to edge AI systems, where power efficiency, form factor, and cost constraints further emphasize the importance of fine-pitch, low-overhead interconnect technologies. Future trends toward die-to-wafer hybrid bonding and system-level co-design are briefly discussed.

Biography: Fumihiro Inoue is an Associate Professor at Yokohama National University, specializing in 3D integration and chiplet. Before joining the university, he contributed extensively to advancing unit processes for 3D integration during his role as researcher at imec, which lasted until 2021. Since April 2024, Dr. Inoue has also served as the Vice-Director of the Semiconductor and Quantum Integrated Electronics Research Center at Yokohama National University, where he continues to lead cutting-edge research initiatives.

11:50 Lunch

13:20 **Fundamentals of RF measurements, modeling, and test structure design**

Shuhei Amakawa, *Hiroshima University*

ABSTRACT: This tutorial will cover basic concepts in RF, related to measurements, modeling, and test structure design. It will first introduce the basic physical picture of wave propagation along a transmission line in a way understandable to IC designers not necessarily specializing in RF. It will then discuss the concept of S-parameters and how measurement/simulation reference planes should be defined. Some practical measurement and modeling issues will be presented that the speaker encountered and dealt with when working with frequencies above 100 GHz, together with design recommendations.

Biography: Shuhei Amakawa received B.Eng., M.Eng., and Ph.D. degrees from the University of Tokyo in 1995, 1997, and 2001, respectively. He also received an MPhil degree in physics from the University of Cambridge. Since 2010, he has been with Hiroshima University, where he is currently a professor. His research interests include RF circuit design and microwave measurements. He serves/served as a TPC member of IMS and ISSCC, among others.

14:10 **Next Generation Power Electronics Technologies Based on Wide Bandgap Semiconductors**

Yasunori Tanaka,
National Institute of Advanced Industrial Science and Technology

ABSTRACT: The advancement of next-generation power electronics technologies based on wide-bandgap semiconductors has accelerated dramatically over the past two to three years. In particular, SiC power semiconductors, owing to their superior material properties, have been rapidly put into practical use as key devices that significantly contribute to higher efficiency and reduced size and weight of power converters in the field of electric mobility, including railway systems and electric vehicles (EVs). As a result, SiC power devices are steadily establishing their position as a fundamental technology underpinning an electrified society. In this presentation, an overview will be provided of the characteristics of next-generation power semiconductor devices, focusing on SiC, as well as related device process and design technologies.

Biography: Yasunori Tanaka received his Ph.D. in Electronic Engineering from Osaka University in 1996. In the same year, he joined the Electrotechnical Laboratory (ETL), where he engaged in research of SiC doping control technologies using ion implantation. In 2001, following the reorganization of ETL into the National Institute of Advanced Industrial Science and Technology (AIST), he started his work on the development of SiC power devices. From 2014, he was seconded to the Cabinet Office of Japan to promote a national project on next-generation power electronics technology development.

He returned to AIST in 2016 and has since been engaged in the management of national projects related to next-generation power electronics technologies. Since 2023, he has served as Director of the Advanced Power Electronics Research Center in AIST.

15:00 Break

15:20 **Key Device Technologies and Challenges for 3D Non-Volatile Memory**

Masumi Saitoh, *Kioxia Corporation*

ABSTRACT: This tutorial provides an overview of recent research trends in 3D non-volatile memory. Non-volatile memory is moving to 3D stacking for increasing the bit density to meet the demand for large datasets of AI. There are two main 3D approaches: vertical stacking (e.g. 3D flash memory) and horizontal stacking (e.g. cross-point memory). 3D flash memory has been leading aggressive multi-layer stacking of non-volatile memory. Stacked ReRAM (Resistive RAM) and PCM (Phase Change Memory) have been proposed for various applications including in-memory computing. Ferroelectric memory with ferroelectric HfO film has been widely studied for various 3D structures such as FeFET (Ferroelectric FET), FeRAM (Ferroelectric RAM), and FTJ (Ferroelectric Tunnel Junction). MRAM (Magnetic RAM) with advanced MTJ has been developed for high-speed and high-density cross-point memory. There remain key challenges such as process integration, reliability, and device variability, requiring tight collaboration between basic research and manufacturing to deliver low-cost and high-performance 3D non-volatile memory.

Biography: Masumi Saitoh received the Ph.D. degree in electronic engineering from the University of Tokyo in 2005. In 2005, he joined Corporate Research and Development Center, Toshiba Corporation, where he was engaged in R&D of ultralow-power nano-scaled transistors and emerging memory device technologies. Currently, he is a senior manager in Frontier Technology R&D Institute, Kioxia Corporation, responsible for management of R&D of emerging memory device technologies.

16:10 **Silicon quantum computer and cryo-CMOS technologies**

Takahiro Mori,

National Institute of Advanced Industrial Science and Technology

ABSTRACT: Quantum computers aim to solve some computational problems that are difficult for conventional technologies to solve. There are currently some candidates for their hardware, and we can use some prototype machines. However, their performance is insufficient to solve practical problems, so no clear winners have emerged yet, because the number of available qubits is still low. Therefore, large-scale integration is highly desired. From this perspective, silicon qubit technology is promising because we can use mature fabrication technologies developed for LSI technology. This talk introduces silicon quantum computer technology, its research trends, and its outlook. It also introduces cryo-CMOS technology, which will be used to control qubits to realize quantum gate operation.

Biography: Takahiro Mori received his B.S., M.S., and Ph.D. degrees in applied physics from Tohoku University in Sendai. He began his professional career as a postdoctoral fellow at RIKEN in Saitama and then joined the National Institute of Advanced Industrial Science and Technology (AIST) in Tsukuba as a researcher. He is currently a research team leader at Semiconductor Frontier Research Center at AIST. His team mainly works on silicon quantum devices and cryo-CMOS technologies.

17:00 Close of Tutorials

17:30 Welcome Reception

TECHNICAL PROGRAM

Tuesday, March 24

9:00 Greetings

Y. Fukuzaki (General Chair), K. Xia (Technical Program Chair)[1], T. Ohguro (Technical Program Chair)[2]
Rapidus US, LLC, USA
[1]*TSMC*
[2]*Toshiba Electric Devices & Storage Corporation*

Session 1: Circuits for Test and Computation

Session Chairs: Brad SMITH, *BeeSmith, LLC*
Larg WEILAND, *PDF Solutions, Inc.*

09:10 1.1

Ultra-low leakage power switch for RO array characterization in 18nm FD-SOI technology platform validation

C. Cagli, H. Degoirat, M. Lamy, F. Pourchon, J. B. Moulard, F. Granoux, M. Dahmani, R. Wilson
STMicroelectronics, 850 Rue Jean Monnet, Crolles, France

ABSTRACT – we proposed the architecture of a novel power switch implemented within a test chips (TC) in 18nm FD-SOI technology that provides DUT selection in ring oscillators (RO) array. We further improved the proposed selection circuit with a novel architecture that uses mainly thick-oxide NMOS with a level-shifter (LS). Although the footprint of the LS counts for 25% of the power switch area, this solution proves to decrease the leakage current substantially, bringing the signal-to-noise ratio up by more than two orders of magnitude, enabling the characterization of ultra-low leakage ROs.

09:30 1.2

Statistical Capacitance Measurement of Si Trench Capacitors Using 3D Stacked Array Test Circuit

Ryoya Nishimaki, Koga Saito, Takezo Mawaki, Rihito Kuroda
Graduate School of Engineering, Tohoku University

ABSTRACT – A 3D stacked array test circuit is demonstrated in this paper. The array test circuit and the device under test (DUT) chip were fabricated separately, and the DUT chip was stacked on the array test circuit chip using cell-wise connections using micro-bumps. DUTs can be fabricated without the need to consider their impact on the measurement circuit chip, enabling comprehensive statistical evaluation. As DUTs, Si trench capacitors (TCs) were fabricated and a total of 9,516 TCs were measured. The measured Capacitance-Voltage characteristics showed close agreement with those of a conventional analyzer, and the coefficients of variation were less than 0.31 percent. Moreover, the influence of the micro-

bump 3D interconnects was estimated and found to be negligible in this work. These results indicate the feasibility of the proposed 3D stacked array test circuit.

09:50 1.3

Influence of solder bumps-induced mechanical constraint on the performance of BJT ring oscillators

M. Dahmani, S. Gallois-Garreignot, M. Dugor, B. Van-Haaren, L. Broussous, F. Belfils, C. Cagli
STMicroelectronics, 850 Rue Jean Monnet, Crolles, France

ABSTRACT – We built four BJT-based ring oscillators (RO) in 55nm BiCMOS technology to study the impact of solder bumps deposition on the electrical performance of embedded devices (BJT and poly resistors). We observed that the PNP-based RO, embedded under solder bumps, displays an increase of frequency and power consumption in the order of 5%. We assumed this increase to the thermomechanical stress caused by the deposition thermal profile of the solder bump. To demonstrate it, we run thermomechanical simulations and showed that a resistor component in the RO is subject to enough compressive mechanical constraint that its resistance value could shift by a few % points affecting the RO oscillation frequency. The performance shift is anyway small to be of any concern for applications. Overall, our test structures prove to be very sensitive to mechanical stress and are excellent tools to evaluate the influence of solder bumps on technology performance.

10:10 1.4

Improving Robustness of Leakage-Based MOSFET Reservoir Computing Using Adaptive Pulse-Width Control

Ryuto Seki, Masami Utsunomiya, Yu-Guang Chen[1], Hiromitsu Awano, Takashi Sato
Graduate School of Informatics, Kyoto University Yoshida-honmachi, Sakyo, Kyoto, Japan
[1]Department of Electrical Engineering, National Central University, Taiwan

ABSTRACT – This paper proposes a method to enhance the robustness of Leakage-based MOSFET Echo State Network (LMESN) against environmental variations. LMESN is a hardware reservoir computing architecture that exploits MOSFET subthreshold leakage currents. The proposed method consists of two components: adaptive tuning of the minimum input pulse width based on temperature to compensate for leakage current change, and the use of Lasso regression for output-weight training to suppress errors arising from temperature-coefficient variations. Simulation results on a time-series classification task confirm that the inference accuracy is maintained across temperatures ranging from 5 to 75 ◦C without requiring retraining over this temperature range.

10:30 Break

Session 2: AI and Machine Learning

Session Chairs: Takayuki MORI,
Kanazawa Institute of Technology
Tatsuya OHGURO,
Toshiba Electric Devices & Storage Corporation

10:50 2.1

Machine Learning-Based Failure Mode Detection in 3D-DRAM Gate-All-Around Select Transistors

Jerome Mitard, Husnu Murat Kocak, Romain Ritzenthaler, Nouredine Rassoul, Eren Canga, A. Belmonte
Compute Technology Device Department, IMEC, Belgium

ABSTRACT – We present a multi level CNN that classifies four terminal I–V curves of 3D DRAM GAA select transistors on 300 mm wafers with >95% accuracy, resolving up to 14 failure modes, including all currents to the substrate, revealing process dependent patterns and unknown defect clusters to accelerate process maturity of future high density 3D DRAM memory.

11:10 2.2

Speeding Up Capacitance-Voltage Measurements Using Gaussian Processes and Active Learning

Husnu Murat Kocak, Hiroaki Arimura[1], Jerome Mitard[1], Jesse Davis
Department of Computer Science, KU Leuven, Celestijnenlaan 200A, Leuven, Belgium
[1]*Compute Technology Device Department, IMEC, Remisebosweg 1, Leuven, Belgium*

ABSTRACT – Capacitance–Voltage (C–V) measurement is an important but slow device testing technique. We introduce an active learning methodology to reduce the required number of measurement needed by using Gaussian Process Regression to predict unmeasured values. The proposed method results in a 4x reduction in the number of needed measurements while generating almost perfectly identical curves with a 0.24% capacitance equivalent thickness error, and 0.9977 R2 score.

11:30 2.3

Accelerating Load-Pull Measurements Using Attentive Neural Processes

Jui-Yang Hsu, Yu-Ting Chen, Bo-Yuan Chen, Chao-Wen Lin, Chia-Wei Chuang, Chuang-Ju Lin, Kun-Ming Chen, Guo-Wei Huang
Taiwan Semiconductor Research Institute, National Institutes of Applied Research

ABSTRACT – We propose Attentive Neural Processes (A-NPs) to accelerate load-pull measurements. Extrapolating the optimal reflection coefficient across various bias conditions is challenging due to the requirement for accurate output power measurements and time-consuming of testing. By leveraging the cross-attention in neural networks, optimal reflection coefficient can be accurately predicted using only a few measured points. This approach can reduce measurement time by approximately 65.7% per bias condition, and enabling effective integration into high-frequency load-pull measurement system.

11:50 2.4

VQ-VAE–Based Test Structure Generation for Constructing Design-Fabrication Surrogate Models

Ryugo Shimamura, Shun Yasunaga, Tomoya Nakamura, Chen Wang[1], Michael Kraft[1], Yoshio Mita
The University of Tokyo, EEIS
[1]*KU Leuven, ESAT/MNS*

ABSTRACT – In view of training fabrication surrogate models based on machine learning, we propose a semi-automated representative pattern selection pipeline to mitigate sampling bias caused by ad hoc manual selection. From an arbitrary design, a set of layout patterns is selected as a representative dataset of the design through dimensionality reduction using self-supervised representation learning with Vector Quantization-Variational Autoencoder and clustering with kcenter algorithm. A modified U-Net based surrogate model for lithography and deep reactive ion etching trained using a dataset generated with the suggested pipeline was able to predict fabrication deviations with higher accuracy compared to models trained with datasets from other semi-automated sampling methods (7.2-percentage-point improvement in boundary IoU), supporting the validity of this method.

12:10 Lunch

Session 3: Device Characterization

Session Chairs: Jerome MITARD, im*ec*
Francesco DRIUSSI,
Università degli Studi di Udine

13:30 3.1

On-Wafer Golden Devices and Layout Structures for Long-term Prober Chuck Temperature Verification and Monitoring

Wuxia Li, Kejun Xia[1], Lei Chao, Shimeng Zhang
NXP Semiconductors, Front End Innovation
[1]*TSMC, Power Management Business Development*

ABSTRACT – We report the temperature-sensing performance of seven types of on-wafer devices used for verifying prober chuck temperature after calibration, as well as for assessing chuck temperature stability and repeatability. Different types of devices show drastically different stability after twenty full temperature cycles. With optimized biasing, NMOS and its source-drain junctions are the best devices and can achieve less than 1.1°C instability for the temperature range of -40°C to 225°C. We propose binary tree test structures for bench test and 1xN pad frame for probe-card based auto test to overcome the pad wear-out. The proposed method enables easy implementation and excellent stability for long-term monitoring of prober chuck temperature control, ensuring reliable silicon data collection.

13:50 3.2

Monte Carlo simulation method for distance-dependent mismatch and comparison of common-centroid and dispersion layouts

Kejun Xia

TSMC, Power Management Business Development

ABSTRACT – We present a Monte Carlo simulation method to model distance-dependent mismatch through randomly distributed long-range imperfections, with explicit inclusion of device-size dependence. The simulation results agree well with the theoretical approximations. We compare mismatch in layouts that use either common-centroid or maximal dispersion structures. At large correlation lengths, common-centroid layouts yield the lowest mismatch, while at short correlation lengths, dispersion plays a more dominant role than common-centroid in reducing mismatch.

14:10 3.3

Optimum Setting of 1/f Noise System towards Ultra-low- noise Floor and Best Practice for Multi-finger MOSFET Noise Characterization

Lei Chao, Shimeng Zhang, Jeroen van Beurden, Andries Scholten, Wuxia Li

NXP Semiconductors, Front End Innovation

ABSTRACT – We report a step-by-step approach for on-wafer 1/f noise system optimum setting to identify and minimize the external signal impacts, to achieve the best noise floor when a system is installed at a new lab, or after a certain period of usage. We share our best practice to obtain reliable low-frequency noise spectra for MOSFETs with various gate finger numbers, which are strongly affected by parasitic resistance and thus need special attention. Our approach and results provide insights to ensure reliable 1/f noise data collection.

14:30 3.4

Evaluation of Dummy Biasing on Leakage and Noise Performance in 4-nm FinFET Process

Seunghyun Noh, Jinho Choi, Yoongeun Seun, SungJoon Park, Jooyoung Song

Samsung Electronics, Giheung-gu, Yongin-si, Republic of Korea

ABSTRACT – In this paper, we propose a dummy biasing guideline to reduce off-state leakage in a 4-nm FinFET process. To evaluate effect of dummy biasing, we compare three dummy biasing schemes using silicon measurements: conventional rail biasing, floating the

source and drain terminals, and floating the source, drain, and gate terminals. The results show that floating the source and drain terminals of dummy transistors effectively suppresses the parasitic subthreshold leakage path between active and dummy transistors. Off-state leakage is reduced by up to 62% while maintaining drive current and 1/f noise characteristics within measurement variation. However, floating the gate terminal of dummy transistor can induce an ill-defined gate potential, which can increase drive-current variation. This guideline is particularly useful for analog designs that use dummy transistors to compensate layout-dependent effects and provides an effective leakage power optimization strategy in advanced-node designs.

14:50 Break
15:10 Exhibitors

Session 4: Process Characterization

Session Chairs: Wuxia LI, *NXP Semiconductors*
Jerome MITARD, *imec*

15:50 4.1

Defect profiling of Al_2O_3-passivated InGaP layers via planar test structures

Paolo La Torraca, Pavel Kirilenko[1], Rajan Bharti, Muskan Jain, Satish Bonam, Lida Ansari, Farzan Gity, Karim Cherkaoui[2], Alexander Tonkikh[2], Dmitry Sizov[2], Paul Gore[2], Michael Grundmann, Paul K. Hurley

Tyndall National Institute, Cork, Ireland, [1]*Tyndall National Institute, Cork, Ireland* [1]*Tyndall National Institute, Cork, Ireland*
[2]*Meta Reality Labs*

ABSTRACT – The electrically active defects in Al_2O_3-passivated InGaP layers, representative of an AlInGaP red micro-lightemitting diodes (μ-LED) sidewall, are characterized by using planar metal/insulator/semiconductor (MIS) capacitors test structures. The use of a planar test structure avoids the complexity of the full μ-LED device analysis and enables the selective InGaP/Al_2O_3 system characterization. The electrically active defects of InGaP/Al_2O_3/Ni MIS test structures, subject to different surface treatments, are investigated by multifrequency capacitance-voltage (CV) and conductance-voltage (GV) curves analysis. Trap levels located in the InGaP and in the Al_2O_3 are detected and profiled. The effect of the surface treatment (either no treatment, wet etching, or dry etching) on the detected traps is reported.

16:10 4.2

Extraction of Shockley-Read-Hall lifetime at the InGaP/Al_2O_3 interface using transient capacitance relaxation

Pavel Kirilenko, Paolo La Torraca, Rajan Bharti, Muskan Jain, Satish Bonam, Lida Ansari, Farzan Gity, Karim Cherkaoui, Emanuele Pelucchi, Gediminas Juska, Alexander Tonkikh, Andreas Arnlind, Dmitry Sizov, Paul Gore, Michael Grundmann, Paul K. Hurley

Tyndall National Institute, Cork, Ireland

ABSTRACT – Shockley-Read-Hall (SRH) generation in a MOS capacitor is analyzed to extract the SRH lifetime near the InGaP/Al_2O_3 interface. The transient capacitance relaxation is dominated by electron-hole pair generation through InGaP mid-gap states within 10 nm from the InGaP/Al_2O_3 interface, confirmed using TCAD simulation. The method sensitivity to interface modification is demonstrated.

16:30 4.3

Accuracy Limits of TLM and CTLM Test Structures for Ultra-Low Contact Resistance Extraction in InGaAs/InP Technologies

Anouk Lubben, Yi Wang, Yuqing Jiao, Johan Klootwijk

Eindhoven Hendrick Casimir Institute, Eindhoven University of Technology, Eindhoven, the Netherlands

ABSTRACT – This work investigates the accuracy of Transfer Length Method (TLM) and Circular Transfer Length Method (CTLM) test structures for extracting ultra-low contact resistivities on highly doped n-InGaAs. CTLM reliably reaches the 10^{-8} Ωcm^2 regime with high reproducibility, while TLM accuracy is limited by fabrication-dependent effects such as incomplete mesa isolation and current spreading. Structure dependent deviations between TLM and CTLM are analyzed, and practical guidelines are provided for achieving reliable TLM performance at ultra-low contact resistivities.

16:50 End of Day 1

Day 2: Wednesday, Mar 25

08:30 Registration Desk Opens

09:00 **Invited Talk 1**

Micro Biomolecular Sensors: A Review and Challenges

Chih-Ting Lin

Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan

Session 5: MEMS and Sensors

Session Chairs: Yoshio MITA, *The University of Tokyo*
Stewart SMITH, *The University of Edinburgh*

10:00 5.1

A Contact-Closing Test Structure for Electrical In-Chamber Release Endpoint Detection During Vapor HF Etching

Akihiko Yoshida, Shun Yasunaga, Ryosho Nakane, Akio Higo, Yoshio Mita

The University of Tokyo

ABSTRACT – An electrical gap-closing MEMS test structure was proposed and validated to detect an endpoint of movable structure release in single-lithography silicon-on-insulator (SOI) MEMS with vapor-phase hydrofluoric acid (vHF) etching performed in an opaque process chamber. A body with the same layout as the target structure, suspended by a spiral spring, was co-fabricated on the same chip, and designed to become movable upon release and contact an adjacent fixed electrode across a small gap to generate a distinct electrical signature. Al wire bonded pads were routed to an external source-measure unit. A clear transition was observed, and release was confirmed by post-etch infrared microscopy, supporting contact closure as a practical indicator for laboratory prototyping.

10:20 5.2

Comparative Study of Transducer Materials for Sodium-Selective EGISFETs: Stability Improvement and Interference Rejection

Kai-Chun Huang, Yan-You Zhou, Chih-Ting Lin

Graduate Institute of Electronic Engineering, National Taiwan University

ABSTRACT – Real-time monitoring of trace alkali metal contamination in ultrapure water (UPW) is critical for yield management in advanced semiconductor manufacturing. This study presents a systematic optimization of transducer materials to develop a robust Extended-Gate Ion-Sensitive Field-Effect Transistor (EGISFET) for sodium sensing. We investigated the electrochemical characteristics of SiO_2, Al_2O_3, and TiO_2 sensing layers with varying thicknesses. While Al_2O_3 exhibited the highest intrinsic pH sensitivity, the 200-nm TiO_2 film was identified as the optimal interface for process control applications due to its superior device-to-device uniformity and exceptional stability, characterized by the lowest baseline drift variance (σdrift = 0.09$ pNa). Functionalized with a sodium-selective membrane, the optimized TiO_2-EGISFET achieved a Nernstian sensitivity of 53.81 mV/pNa. Crucially, mixed-ion interference tests demonstrated that the sensor maintains high selectivity against potassium ions (K^+), effectively rejecting interference even in high-background environments. These results establish the proposed TiO_2-based test structure as a viable and stable platform for inline contamination monitoring in semiconductor wet processes.

10:40 5.3

An Ultra-Thin Indium Oxide FET Test Structure for Sweat Ion Sensing

Jheng-Ru Wu, Yu-Ta Chen[1], Chien-Fu Chen

Graduate School of Advanced Technology, National Taiwan University

[1]*Nano Electromechanical Systems Research Center, National Taiwan University*

ABSTRACT –This work presents a dual-mode (back-gate and liquid-gate) 4 nm ultra-thin indium oxide (In_2O_3) field-effect transistor (FET) test structure for sweat ion sensing. Under back-gate operation, the device shows proper transistor behavior with an on/off current ratio on the order of 10^5, confirming effective channel formation and gate control. In liquid-gate configuration using an Ag/AgCl reference electrode, the drain current exhibits a concentration-dependent response to Na^+ (10–160 mM) with an average sensitivity of ~6.3 nA/mM, demonstrating ion-induced modulation of the ultra-thin In_2O_3 channel. These results establish the proposed structure as a test platform for evaluating ultra-thin oxide semiconductor channels toward wearable sweat ion sensing.

11:00 Break

Session 6: Memory

Session Chairs: Carlo CAGLI, *STMicroelectronics N.V.*
Yuzo FUKUZAKI, *Rapidus US, LLC, USA*

11:20 6.1

Read Current in Ferroelectric Tunnel Junctions: Transient versus DC Contributions and Trap Related Effects

F. Driussi, M. Segatto, M. Massarotto, L. Carpentieri1, S. Slesazeck[1], D. Esseni
DPIA, Università degli Studi di Udine, Via delle Scienze 206, Udine, Italy
[1]*NaMLab gGmbH, Nothnitzer Str. 64a, 01187 Dresden, Germany*

ABSTRACT –Ferroelectric Tunnel Junctions (FTJs) performance as memristive devices is typically represented by their Tunneling Electro-Resistance Ratio (TER), defined as the ratio between the DC current measured in the low resistance state (LRS) and in the high-resistance state (HRS) of the device. However, during characterization of the FTJ read current and hence of TER, the transient contributions to the current are often overlooked in the literature, possibly causing misleading interpretations of the experimental TER. Here we propose a new, comprehensive characterization of the readout currents of different FTJ stacks, also investigating on their transient components. We report a solid interpretation of the experiments based on the response of traps in the ferroelectric, also supported by physics-based simulations.

11:40 6.2

MRAM Wafer Level Adaptative Edge Testing for Efficient Yield and Reliability Control

Maximilian Liehr, Sean Ogden, Mark Raymond, Kyle Funk, Herve Elemva, Kilho Lee, Gen Feng, Karsten Beckmann, Antoine Chavent[1], Tien Dang Ngoc[1], Daniel Grout[1], Steven Lequeux[1],

Siamak SALIMY[1]
NY CREATES, 253 Fuller Road, Albany, NY 12203, USA
[1]Hprobe Mycronic, 4 rue Joliot Curie, 38320 Eybens, France

ABSTRACT –Magnetoresistive Random Access Memory (MRAM) offers high-speed, non-volatile storage for advanced embedded and standalone applications, yet wafer-level characterization of switching and reliability remains challenging due to the magnetic nature of device operation. This work presents synchronized magnetic–electrical wafer-level testing using the Hprobe IBEX platform integrated with a Tokyo Electron Limited Precio XL 300 mm probe station. The system enables localized three-dimensional vector magnetic field control and sub-nanosecond pulsed electrical excitation, combined with an adaptive Test/Skip methodology to reduce device stress. Experiments on 300 mm wafers with 14 MTJ pillar (RR) and bottom electrode (V0) geometries quantify resistance screening, R–H loops, DC and pulsed I–V behavior, bit error rate (BER), and endurance across pulse widths from 20 to 200 ns. Statistical analysis across multiple dies demonstrates size dependent switching voltage, yield trends, and pulse-width dependent degradation, consistent with thermal activation models for spin-transfer torque switching. Time savings of up to 28.5% were observed in this paper where overall savings depended heavily on initial device yield time. These results highlight the importance of wafer-level magnetic probing for predictive reliability assessment and scalable high-volume MRAM test methodologies.

12:00 6.3

Comparison of Addressing Methods for Memory Array Characterization

Martin Arteaga Castillo, Vincenzo Della Marca1, Marc Bocquet[1], Jeremy Postel-Pellerin1, Olivier Paulet, Loic Welter, Matthias Vidal-Dho, Baptiste Chatelier, Brice Arrazat
Department of Technology and Design Platforms, STMicroelectronics, Rousset, France
[1]Aix-Marseille University, IM2NP, CNRS, UMR 7334, Marseille, France

ABSTRACT –The development of Resistive Random-Access Memories (RRAM) technologies relies increasingly on statistical characterization of large memory arrays, due to significant device-to-device variability. However, the electrical addressing of individual cells often becomes a major bottleneck during testing, especially for sequentially decoded test vehicles. This work evaluates four practical methods for generating address signals using equipment commonly available in academic or industrial characterization laboratories. Their performance is compared in terms of switching speed, ease of integration with semiconductor parameter analyzers, implementation complexity, and long-term reliability. Experimental results show that FPGA-based solutions provide the fastest switching capabilities, closely followed by

microcontrollers, while Digital I/O ports of semiconductor analyzers offer a good compromise between speed and usability. Switching matrices, although convenient, exhibit the slowest response and potential reliability concerns when used outside their intended purpose.

12:20 6.4

On-Chip Learning with EEPROM Based Synapses: Reliability and Performance Assessment

Thibault BERGAMASCHI, Bastien IMBERT, Vincenzo DELLA-MARCA, Sebastien PERRIN, Arnaud REGNIER[1], Madjid AKBAL[1], Christian RIVERO[1], Nicolas ZAMMIT[1], Thibault KEMPF[1], Jorge-Daniel AGUIRRE-MORALES, Jean-Michel PORTAL, Marc BOCQUET
Aix-Marseille Univ, Université de Toulon, CNRS, IM2NP, Marseille, France
[1]STMicroelectronics Rousset, France

ABSTRACT –Embedded EEPROM technologies are widely used in industrial microcontrollers and offer excellent reliability, but their potential for analog operation remains under-explored due to the limited observability of cell-level electrical behaviour in standard memory arrays. This work leverages the SuperCAST test structure, a fully addressable 4k-cell EEPROM array, to perform detailed analog characterization of floating-gate devices. The architecture provides individual access to each memory cell, enabling pulse-by-pulse programming analysis, variability extraction, endurance and retention evaluation, and precise readout characterization. These measurements allow assessing the suitability of EEPROM technology for analog synaptic operation in neuromorphic systems. Finally, the experimentally extracted characteristics are incorporated into neural-network simulations to illustrate how device-level non-idealities impact learning performance. The results demonstrate that SuperCAST is a powerful platform for evaluating embedded EEPROM as a candidate for reliable analog in-memory computing.

12:40 Lunch

Session 7: Reliability

Session Chairs: Francesco DRIUSSI,
Università degli Studi di Udine
Carlo CAGLI, *STMicroelectronics N.V.*

14:00 7.1

Characterization of Non-conducting RF Hot Carrier Stress Impact on transistor noise from 10 MHz to 26.5 GHz in 5-nm FinFETs

G. Niu, X. Ding, H. Zhang1, W. Wang[1], K. Imura[1]
ECE Department, Auburn University, Auburn, AL, USA
[1]Maxlinear Inc., Carlsbad, CA, USA

ABSTRACT –This work presents, for the first time, a systematic investigation of high-frequency flicker noise degradation from 10 MHz to 26.5 GHz in commercial foundry 5-nm FinFETs subjected to non-conducting RF hot-carrier stress. The experimental results demonstrate that, even under an aggressive nonconducting RF stress condition with a maximum drain voltage of $V_{d,max} = 2V_{dd}$, the induced noise degradation exhibits a sufficiently long lifetime. These findings confirm the robustness of 5-nm FinFET technologies for RF circuit applications requiring stringent phase-noise performance.

14:20 7.2

Impact of Fluorine Incorporation on Boron Diffusion and Reliability in Advanced High Voltage FinFETs

Jia-Hong Lin, Po-Hsun Chen[1], Ling, Tang[2], Meng-Xuan Feng[3], Ting-Chang Chang[4]

Department of Physics, National Sun Yat-sen University, Kaohsiung, 80424, Taiwan

[1]Department of Electronic Engineering, I-Shou University, Kaohsiung 840, Taiwan

[2]Institute of Advanced Semiconductor Packaging and Testing, National Sun Yat-sen University, Kaohsiung, 80424, Taiwan

[3]Department of Microelectronics Engineering, National Kaohsiung University of Science and Technology, Kaohsiung, 811213, Taiwan

[4]Department of Physics, and also with College of Semiconductor and Advanced Technology Research, National Sun Yat-Sen University, Kaohsiung, 804, Taiwan

ABSTRACT –This work investigates the impact of fluorine incorporation in the lightly doped drain (LDD) region of high voltage FinFETs, with particular emphasis on device reliability under hot-carrier stress conditions. The experiment results exhibit that the device with higher fluorine doped concentration (B/F^+) shows a better hot-carrier reliability. This enhancement is primarily attributed to the formation of robust Si–F bonds at the Si/SiO_2 interface, which effectively passivate interface traps and decrease defect generation induced by high electric fields. In addition, boron will diffuse to the interface and form boron interstitial and interface shallow defect states. However, fluorine incorporation is found to suppress boron diffusion in the LDD region. As a result, both device stability and long-term reliability are substantially improved.

14:40 7.3

Parasitic Characterization of Hot-Carrier-Induced Degradation using Experimental S-Parameters for RF- MOSFETs

Chika Tanaka, Tatsuya Suzuki, Atsushi Sueoka, Fumie Fujii, Kazuya Matsuzawa

Memory Division, Kioxia Corporation, Japan

ABSTRACT –This study provides an examination of the impact of hot-carriers induced degradation on the small-signal parameters of

MOSFET. Specifically, it focuses on analyzing the source and drain resistances, as well as the gate resistance using experimental S-parameters before and after DC voltage stress. To get the trap distribution of aged MOSFET structure, 2D TCAD simulations were conducted. Observations indicate that the gate resistance of the parasitic components and the distribution of trapped charges within the device structure have changed due to hot-carrier stress, although there are no significant changes in the source and drain resistance with respect to the voltage stress. These results may inform design improvements for RF-MOSFETs through detailed modeling of AC parameters.

15:00 7.4

Reliability Comparison under Drain Bias Stress for N- and P-Type LTPS Thin-Film Transistors

Meng-Xuan Feng, Po-Wen Chang, Sheng-Po Chang, Jia-Hong Lin[1], Tsung-Ming Tsai[2]
Microelectronics Engineering, National Kaohsiung University of Science and Technology, Taiwan
[1]Department of Physics, National Sun Yat-sen University, Taiwan
[2]Department of Materials and Optoelectronic Science, National Sun Yat-Sen University, Taiwan

ABSTRACT –In the early generations of low-temperature polycrystalline silicon (LTPS) backplanes, p-channel thin-film transistors (TFTs) were predominantly employed due to their lower dopant activation requirements and superior bias-stress stability. With dimension scaling and rising current demand in micro-LED backplanes, n-type LTPS TFTs have become attractive owing to their higher carrier mobility and stronger drive capability. However, when p-type devices are directly replaced with ntype devices, we observe pronounced degradation under off state drain bias stress (OSS), including severe on-current loss and increased leakage. The degradation mechanism is systematically investigated and confirmed by C-V measurements, transfer characteristics in the saturation region, and SILVACO TCAD simulations. Hot-carrier stress (HCS) reliability is also examined and shown to suffer from similar field-induced damage.

15:20 Break
15:40 ICMTS 2027 Presentation
Francesco Driussi
Università degli Studi di Udine

Session 8: ESD

Session Chairs: Kejun XIA, *TSMC*
Jun TANIGUCHI, *Keysight Technologies, Japan*

15:50 8.1

Test Structures to Study Interconnection Metal/Via/Contact

Reliability under Transient Pulse Stresses of ESD and Surge Events

Pi-Yuan Hsiao, Chia-Tsen Dai[1], Tung-Yang Chen1, Ming-Dou Ker
Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[1]AIP Technology Corporation, Taiwan Branch

ABSTRACT –In this study, a Transmission Line Pulse (TLP) system and a Surge tester are applied to investigate damage mechanisms of metal/via/contact interconnects in a 0.18-μm CMOS technology. Results indicate that the transient thermal response of these interconnects strongly depends on pulse duration. Failure analysis reveals distinct mechanisms depending on whether damage is caused by short or long pulses. The pulse-dependent damage behavior is crucial for reliable IC design, especially in the advanced CMOS technologies.

16:10 8.2

The Influence of Skin Effect on Metal Lines in ESD Protection Circuit

Cheng-Han Chiang, Chun-Yu Lin
Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

ABSTRACT –The purpose of this paper is to investigate how the skin effect degrades the electrostatic discharge (ESD) robustness of metal interconnects. Metal lines with various widths and lengths were evaluated using an ESD tester. Based on the experimental results and the underlying skin-effect theory, a method for predicting the ESD tolerance of metal lines is proposed. The estimated ESD robustness of some test keys shows good agreement with the measured data. However, the skin effect alone cannot explain the observed trend that longer metal lines exhibit lower ESD robustness.

16:30 8.3

Investigation on ESD Robustness of SiC Devices by Transmission Line Pulse Measurement for Monolithic Integration Applications

Hung-Yu Huang, Ya-Zhi Hu[1], Ming-Dou Ker[1]
Institute of Pioneer Semiconductor Innovation, National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[1]Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

ABSTRACT –Electrostatic discharge (ESD) robustness of silicon carbide (SiC) devices using transmission line pulsing (TLP) measurements is studied in this work. The devices under examination include the gate-connected-to-ground NMOS (GGNMOS), the gate-connected-to-VDD PMOS (GDPMOS), N+/PW diode, and P+/NW diode. ESD robustness of the SiC based diodes and GDPMOS can be enhanced by increasing their device sizes under both breakdown and forward modes. In contrast, ESD robustness of SiC-based GGNMOS can be improved only by increasing total width under the forward mode. Additionally, ESD

robustness of the diodes is greater than those of the GGNMOS and GDPMOS. An ESD protection scheme is proposed that utilizes N+/PW and P+/NW diodes under forward mode to enhance protection for positive-to-VDD (PD) and negative-to-VSS (NS) stress modes. Additionally, a power-rail ESD clamp circuit is integrated to further strengthen protection for positive-to-VSS (PS) and negative-to-VDD (ND) stress modes. This approach provides comprehensive ESD protection for the SiC-based monolithic integration circuits.

16:50 End of Day 2
17:30 Banquet

Day 3: Thursday, Mar 26

08:45
Invited Talk 2

Evaluation, Operando Analysis, and Thermal Modeling of Nanosheet Gas Sensors

Ken Uchida
The University of Tokyo

ABSTRACT –Metal nanosheet and graphene gas sensors offer highly sensitive, low-power platforms that can be readily integrated into microelectronic test element groups (TEGs). Their ultrathin geometry enhances chemiresistive modulation, enabling quantitative modeling and operando analysis of surface reactions. Recent advances in self-heating allow voltage-programmable operation with minimal power. This work presents nanosheet fabrication, adsorption–desorption modeling, self-heating sensor operation, operando surface spectroscopy, thermal-aware structural optimization, and nanoscale temperature mapping. Together these methods establish a unified framework for evaluating and designing Pt-, PtRh-, Au-, and graphene-based low-power nanosheet sensors for IoT society.

Session 9: Cryogenics

Session Chairs: Stewart SMITH,
The University of Edinburgh
Wuxia LI, *NXP Semiconductors*

09:35 9.1

Impact of Contacts and Heatsinks on Heat Accumulation in Cryogenic SOI MOSFETs

Kosuke Hatta, Takayuki Mori, Shota Kondo, Hiroshi Oka[1], Takahiro Mori[1], Jiro Ida
Kanazawa Institute of Technology, Ishikawa, Japan
[1]National Institute of Advanced Industrial Science and Technology, Ibaraki, Japan

ABSTRACT –Addressing heat reduction problems of SOI

MOSFETs is important for Cryo-CMOS technology. In this paper, heat dissipation in SOI MOSFETs via the source/drain contacts and the heatsinks on the active silicon layer at cryogenic temperatures was investigated. Measurements and simulations revealed that source/drain contacts contribute to reducing the channel temperature, whereas the heatsinks showed minimal effects. Moreover, these effects at cryogenic temperatures were shown to be more pronounced than at room temperature. These findings highlight that modeling and optimizing heat dissipation pathways proximal to the heat source are critical at cryogenic temperatures.

09:55 9.2

Maintaining Constant V_{th} from 1.7 K to 390 K Using adaptive back gate bias in 22 FDX technology

Ergen Tao, Guofu Niu, Anni Zhang, Yili Wang
ECE Department, Auburn University, Auburn, AL, USA

ABSTRACT –This work demonstrates, for the first time, the maintenance of a constant threshold voltage (V_{th}) over an ultra-wide temperature range from 1.7 K to 390 K using adaptive back-gate biasing in a 22 nm FDSOI technology. Strong correlation is shown between Vth extracted from measured I_d– V_{gs} characteristics and circuit-level extracted V_{th} across the full temperature range. In addition, the closed-loop V_{th} regulation performance is experimentally validated.

10:15 9.3

Characteristics of P-type Polysilicon Resistors from Cryogenic to High Temperatures and Modeling

Yili Wang, Kejun Xia[1], Guofu Niu, Jim Xia[2], Michael Hamilton
ECE Department, Auburn University, Auburn, AL, USA
[1]TSMC, Hsinchu, Taiwan
[2]BASIS Chandler, Arizona, USA

ABSTRACT –This paper presents cryogenic-to-high-temperature characterization and compact modeling of p-type polysilicon resistors from 18.6 K to 473.15 K. Three resistor families (RPH, RP, and RPL) are characterized using four-terminal Kelvin structures across multiple geometries. RPH exhibits a strong, monotonic negative temperature coefficient of resistance (TCR) over the entire temperature range, whereas RP and RPL show geometry-dependent TCR sign changes and low temperature saturation; several layouts achieve near-zero TCR over a wide temperature span. To capture these behaviors, a Matthiessen's-rule-based double power law (DPL) temperature model is proposed, combining scattering contributions associated with grain boundaries and bulk/impurity effects. Compared with the conventional TC1/TC2 polynomial model, the proposed DPL model provides improved accuracy over the full temperature range and yields parameters that cluster by doping level and vary smoothly with geometry.

10:35 Break

Session 10: Power Devices

Session Chairs: Kohei OASA,
Toshiba Electric Devices & Storage Corporation
Kejun XIA, *TSMC*

10:50 10.1

Investigation of Crystal-Face-Resolved Gate Switching Instability in 4H-SiC UMOSFETs Enabled by a Source-Separated Single-Cell Structure

Wei-Jhe Liao, Chia-Lung Hung[1], Yi-Kai Hsiao[1], Bing-Yue Tsui
Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[1]Semiconductor Research Center, Hon Hai Research Institute, Hsinchu, Taiwan

ABSTRACT – In this work, we demonstrate the crystal-faceresolved gate switching instability in 4H-SiC UMOSFET. By employing a source-separated single-cell (SSSC) structure, we are able to characterize GSI of each crystal face and revealing reliability discrepancies arising from variations in crystal orientation, interface quality, and process-induced sidewall asymmetry.

11:10 10.2

Evaluation of Rise-Time Effects on AC-TDDB Characteristics in SiC MOSFETs Using an In-Situ Gate Leakage Measurement Technique

Shuhei Nakata, Tatsuki Sato
Kanazawa Institute of Technology, Japan

ABSTRACT – Reliability evaluation of SiC MOSFETs under realistic switching operation requires accurate characterization of gate oxide degradation during AC time dependent dielectric breakdown (AC-TDDB) stress. However, under high-frequency rectangular pulse operation with short rise and fall times, large displacement currents originating from the input capacitance obscure the leakage current component, making in-situ monitoring difficult. In this work, a numerical waveform processing technique is developed to compensate for the displacement current by modeling its gate voltage dependence and subtracting it from the measured current in real time. The proposed method enables accurate in-situ extraction of gate leakage current during AC-TDDB testing at 1 MHz with rise times ranging from 7 to 90 ns. Using commercially available SiC MOSFETs from two manufacturers, AC-TDDB behavior is systematically compared with DC-TDDB results, and the dependence on rise time is investigated. The results show that current decay under AC stress is more gradual than under DC stress, indicating longer lifetime under pulsed operation. Furthermore, shortening the rise time significantly accelerates the decay rate of the gate leakage current in both devices. Quantitative analysis based on the time interval between 90% and 75% of the peak current reveals that the rise-time dependence becomes more pronounced at lower gate voltage. These findings suggest that high-speed switching intended to reduce switching losses may enhance defect generation in the gate oxide. The proposed measurement technique provides a practical framework for dynamic reliability evaluation of SiC MOSFET gate oxides under realistic operating conditions.

11:30 10.3

Application of a three-terminal TCAD model for designing shielded field-limiting ring edge termination

Kiyoshi Takeuchi, Munetoshi Fukui, Takuya Saraya, Kazuo Itou, Toshihiko Takakura, Shinichi Suzuki, Hiroyuki Takase, Toshiro Hiramoto

Institute of Industrial Science, The University of Tokyo, Tokyo, Japan

ABSTRACT – Field-limiting ring (FLR) edge termination is widely used in Si and SiC vertical power devices to sustain high lateral off-state voltage and thereby realize strong blocking capability. However, conventional FLR structures are susceptible to fixed oxide charge, which compromises the robustness and reproducibility of termination performance. In this work, we propose a new FLR structure designed to mitigate this charge sensitivity. To efficiently explore the design space, we employ a simplified TCAD model that captures the electrostatic behavior of a representative stripe section of the FLR region.

11:50 10.4

Optimizing LDMOS Device Performance and Reliability Through Drift-Region Engineering

Po-Wen Chang, Jia-Hong Lin[1], Meng-Xuan Feng, Sheng-Po Chang, Po-Hsun Chen[2]

Department of Microelectronics Engineering, National Kaohsiung University of Science and Technology, Kaohsiung, Taiwan

[1]*Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan*

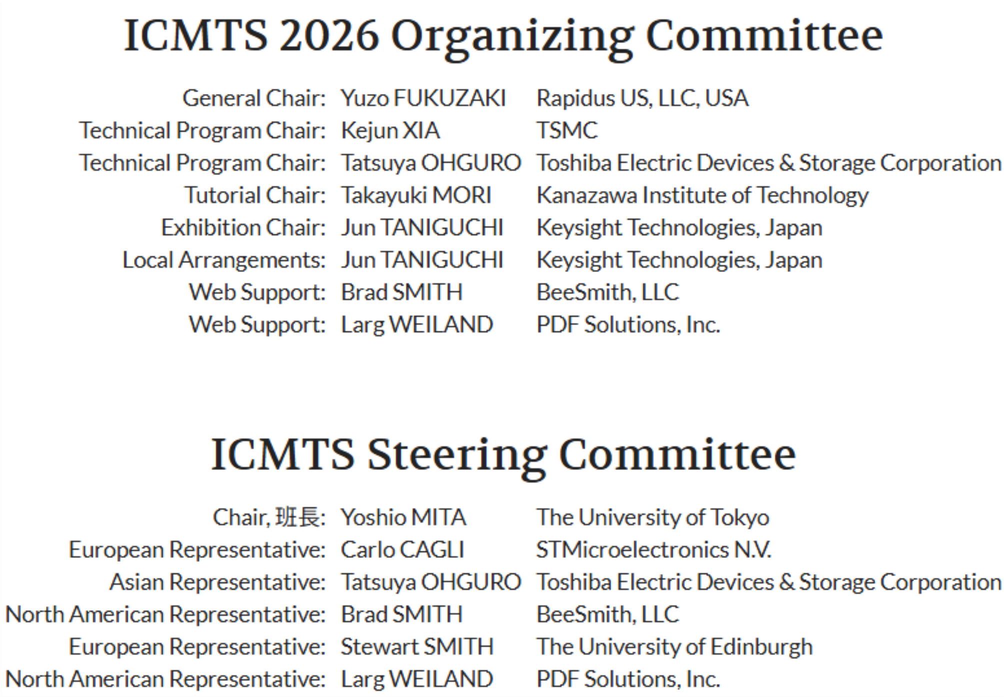
[2]*Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan*

ABSTRACT – This study investigates the impact of drift-region engineering, including junction depth and doping concentration, on the electrical performance and reliability of LDMOS devices in BCD technology. Experimental results and TCAD simulations show that while deeper drift regions generally enhance performance, the resulting peak electric field can cause strong impact ionization that damages the device. However, by balancing the electric field between the gate and drain edges, the impact ionization becomes balanced between these two sides, effectively suppressing degradation. These findings provide essential guidelines for optimizing performance and reliability in high-voltage automotive

and industrial applications.

12:10	Best Paper Award, Closing
12:20	Lunch and Excursion

CONFERENCE OFFICIALS

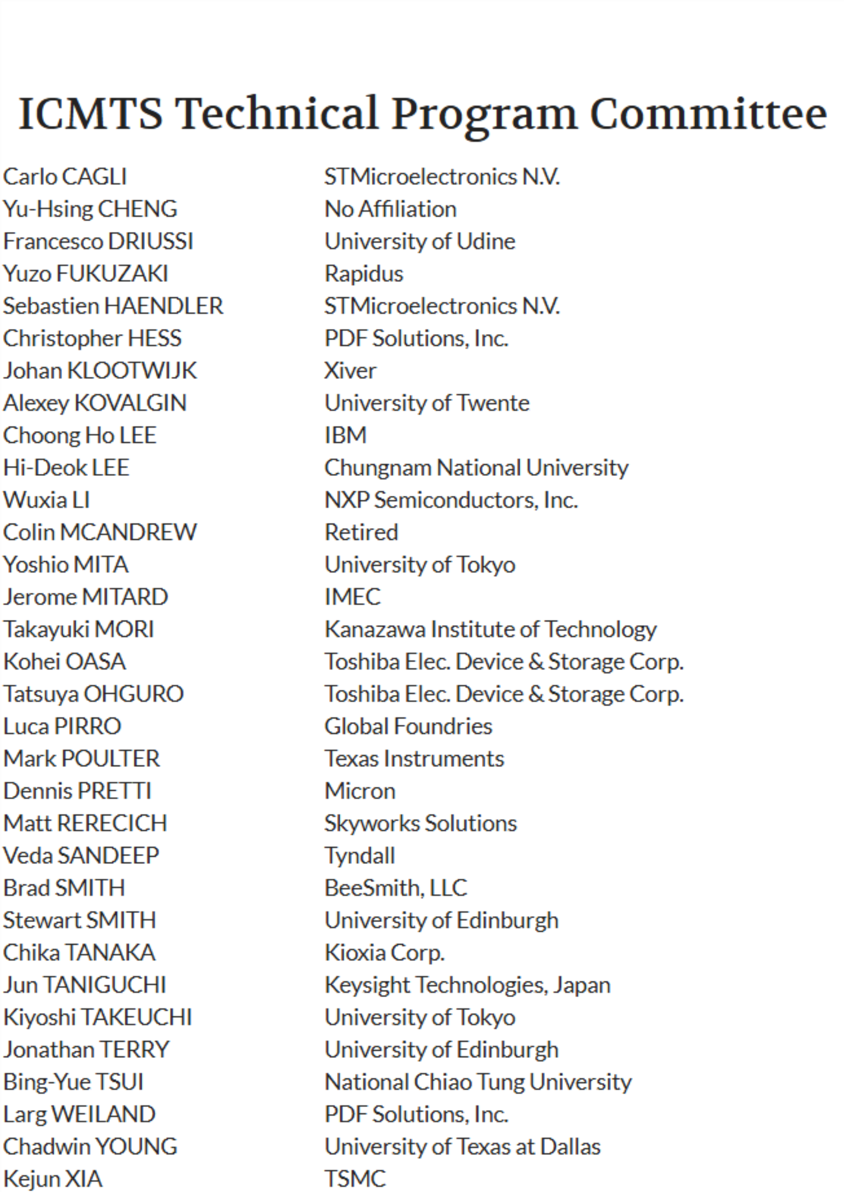


ICMTS 2026 Organizing Committee

General Chair:	Yuzo FUKUZAKI	Rapidus US, LLC, USA
Technical Program Chair:	Kejun XIA	TSMC
Technical Program Chair:	Tatsuya OHGURO	Toshiba Electric Devices & Storage Corporation
Tutorial Chair:	Takayuki MORI	Kanazawa Institute of Technology
Exhibition Chair:	Jun TANIGUCHI	Keysight Technologies, Japan
Local Arrangements:	Jun TANIGUCHI	Keysight Technologies, Japan
Web Support:	Brad SMITH	BeeSmith, LLC
Web Support:	Larg WEILAND	PDF Solutions, Inc.

ICMTS Steering Committee

Chair, 班長:	Yoshio MITA	The University of Tokyo
European Representative:	Carlo CAGLI	STMicroelectronics N.V.
Asian Representative:	Tatsuya OHGURO	Toshiba Electric Devices & Storage Corporation
North American Representative:	Brad SMITH	BeeSmith, LLC
European Representative:	Stewart SMITH	The University of Edinburgh
North American Representative:	Larg WEILAND	PDF Solutions, Inc.



ICMTS Technical Program Committee

Carlo CAGLI	STMicroelectronics N.V.
Yu-Hsing CHENG	No Affiliation
Francesco DRIUSSI	University of Udine
Yuzo FUKUZAKI	Rapidus
Sebastien HAENDLER	STMicroelectronics N.V.
Christopher HESS	PDF Solutions, Inc.
Johan KLOOTWIJK	Xiver
Alexey KOVALGIN	University of Twente
Choong Ho LEE	IBM
Hi-Deok LEE	Chungnam National University
Wuxia LI	NXP Semiconductors, Inc.
Colin MCANDREW	Retired
Yoshio MITA	University of Tokyo
Jerome MITARD	IMEC
Takayuki MORI	Kanazawa Institute of Technology
Kohei OASA	Toshiba Elec. Device & Storage Corp.
Tatsuya OHGURO	Toshiba Elec. Device & Storage Corp.
Luca PIRRO	Global Foundries
Mark POULTER	Texas Instruments
Dennis PRETTI	Micron
Matt RERECICH	Skyworks Solutions
Veda SANDEEP	Tyndall
Brad SMITH	BeeSmith, LLC
Stewart SMITH	University of Edinburgh
Chika TANAKA	Kioxia Corp.
Jun TANIGUCHI	Keysight Technologies, Japan
Kiyoshi TAKEUCHI	University of Tokyo
Jonathan TERRY	University of Edinburgh
Bing-Yue TSUI	National Chiao Tung University
Larg WEILAND	PDF Solutions, Inc.
Chadwin YOUNG	University of Texas at Dallas
Kejun XIA	TSMC

SPONSORS

ACCRETECH
TOKYO SEIMITSU

FormFactor™

KEYSIGHT
TECHNOLOGIES

MPI CORPORATION

UTokyo