



# 38<sup>th</sup> International Conference on Microelectronic Test Structures

## March 23-26, 2026, Kunibiki-Messe, Matsue, Shimane, Japan

Looking for the best opportunity to present and discuss your ideas and results about test structures, measurements, and characterization. [Join the 38<sup>th</sup> ICMTS conference.](#)

A **Tutorial Short Course** will precede the conference sessions. Several of the best measurement, equipment, design, and manufacturing experts, will participate to the **equipment exhibition** and presentations.

The conference will bring together designers and users of test structures to discuss recent developments and future directions, in a **one-track program**, with convivial breaks allowing attendees to discuss and exchange viewpoints and challenges.

A **Best Paper** award will be presented by the Technical Program Committee. The **IEEE Electron Devices Society** is the co-sponsor, and all published papers will be submitted for possible inclusion on **IEEE Xplore®**. Original papers are solicited presenting new developments in *topics relevant to ICMTS*, including but not limited to, test structures, measurements, and results, in the following areas:

- Design
  - Methodologies, Verification
  - Within-die circuits for process characterization/monitoring
  - Design enablement – Characterization and validation of digital and analog libraries
  - Devices and Circuit Modeling
- Measurement techniques
  - DC, AC and RF measurements: setup, test and analysis
  - Reliability test - including thermal stability, failure analysis, prediction, etc.
  - Statistical analysis, variability, throughput increase, smart test strategies
  - Use of machine learning and AI in analysis of data sets - parameter extraction etc.
  - Wafer probing, within-die measurements, in-line metrology
  - Throughput, testing strategies, yield enhancement and process control tests
- Applications
  - Emerging memory technologies (single cell, arrays, and application in neural networks)
  - Emerging transistor technologies for digital/analog/power applications
  - Emerging packaging technologies (3DIC, wafer-on-wafer stacking, chiplet integration)
  - Photonic devices - silicon integration, new displays (OLED,  $\mu$ -displays)
  - Flexible electronics and sensors (organic and inorganic materials)
  - M(N)EMS, actuators, sensors, PV cells and other emerging devices

The author's abstract submission consists of up to [four](#) pages in PDF format (font-embedded). The first page should include a **title**, a **50-word summary**, author name(s), full address, contact number, and e-mail of the lead author, and any preference for oral or poster session presentation. The body of the abstract should consist of one page of text (800 to 1000 words) and up to **two pages of major figures and tables**.

The selection process will be based on the technical merit and will be highly weighted in favor of abstracts with *high test structure content (including illustration) along with measurements and analysis*.

**The submission deadline is 15<sup>th</sup> November 2025.**

Abstracts can be submitted via the ICMTS website <http://www.icmts.net> using the "Submit Abstract" link on the front page.

Notice of paper acceptance will be sent to the selected authors by **17<sup>th</sup> January 2026**, with instructions for expanded manuscript preparation for the conference proceedings. The deadline for **submission of the final paper** will be **17<sup>th</sup> February 2026**.

Please join the ICMTS group at <https://www.linkedin.com/groups/3804498>, if you have an interest in all things test structure related.

Details of the venue, hotel, registration, etc. will be posted at the ICMTS 2026 official web site. ICMTS is planned to be in person with the possibility of adding an online component if necessary.

**For further technical information, please contact the technical program chairs:**

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