ICMTS 2025

Proceedings of the 2025 IEEE INTERNATIONAL CONFERENCE ON MICROELECTRONIC TEST STRUCTURES

37th ICMTS
March 24-27, 2025
The Historic Menger Hotel
San Antonio, TX, USA

Sponsored by the IEEE Electron Devices Society

Proceedings of the 2025 IEEE International
Conference on Microelectronic Test Structures.

Papers have been printed without editing as
received from the authors.

Copyright and Reprint Permission: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For reprint or republication permission, email to:

IEEE Copyrights Manager at
pubs-permissions@ieee.org

IEEE Catalog Number: CFP25MTS-PRT
ISBN: 979-8-3315-3167-6
International Standard Serial Number (ISSN):
1071-9032

All rights reserved.
Copyright ©2025 by IEEE.

Program Schedule

Registration will open at 08:00 each day

Monday, March 24, 2025

09:00 Welcome
09:10 Tutorial 1
10:40 Tutorial 2
11:50 Tutorial 3
12:40 Lunch
14:00 Tutorial 4
15:10 Tutorial 5
16:20 Tutorial 6
17:10 Close
17:30 Reception for All Attendees

Program Schedule

Registration will open at 08:00 each day

Tuesday, March 25, 2025

09:00	-	09:10	Welcome
09:10	-	10:30	Session 1: Application
10:30	-	11:00	Break
11:00	-	12:40	Session 2: Reliability
12:40	-	14:00	Lunch
14:00	-	15:00	Invited Talk: Brian Hoskins (*Natcast R&D*)
15:00	-	15:40	Exhibitor Presentations
15:40	-	16:10	Break
16:10	-	17:30	Session 3: Device Characterization
17:30			End of Day

Program Schedule

Registration will open at 08:00 each day

Wednesday, March 26, 2025

09:00	-	10:20	Session 4: Design & Layout
10:20	-	10:50	Break
10:50	-	12:00	Session 5: RF & Power
12:00	-	13:20	Lunch
13:20	-	14:20	Invited Talk: Shuhei Amakawa (*Hiroshima University)*
14:20	-	15:20	Session 6: Cryogenic Measurements
15:20	-	15:50	Break
15:50	-	16:00	ICMTS 2026 Presentation
16:00	-	17:20	Session 7: Process Characterization
17:20			End of Day
18:30			Banquet

Program Schedule

Registration will open at 08:00 each day

Thursday, March 27, 2025

09:00	-	10:40	Session 8: Test Optimization
10:40	-	11:10	Break
11:10	-	12:10	Session 9: MEMS & Sensors
12:10	-	12:20	Best Paper Announcement, Conference Close
12:20	-	13:30	Lunch
13:30	-	15:30	Excursion: Cruise and Stroll Tour

Table of Contents

Session 1: Applications

1.1 Power switch improvement for RO array characterization in 18nm FD-SOI technology platform validation 3
C. Cagli, F. Pourchon, H. Degoirat, J. B. Moulard, F. Granoux, M. Dahmani, R. Wilson
STMicroelectronics, 850 Rue Jean Monnet, Crolles, France

1.2 Comparative Study of Switching Dynamics in Ferroelectric-based Capacitors with Different Design Options 7
Francesco Driussi, Enrico Rocco, Marco Massarotto, Suzanne Lancaster[1]
DPIA, Università degli Studi di Udine, Italy
[1]*NaMLab gGmbH, Dresden, Germany*
[2]*Chair of Nanoelectronics, IHM, TU–Dresden, Germany*

1.3 Enhancement of Synaptic Properties using $Ta_2O_5/ZnO/Ta_2O_5$ Tri-layer Device 12
Chae-Min Yeom, Sung-Ho Kim, Yu-Bin Kim, Dong-Min Kim, Kil-Sun Roh[1], Young-Su Kim[1], Yong-Goo Kim[2], Hyuk-Min Kwon[3], Hi-Deok Lee
Department of Electronics Engineering, Chungnam National University, Daejeon, Korea
[1]*LAB of Nano Process Technology, National Nanofab Center, Daejeon, Korea*
[2]*Department of Green Semiconductor System, Korea Polytechnic, Daegu, Korea*
[3]*School of Electronic & Electrical Engineering, Hankyong National University, Anseong, Korea*

Session 2: Reliability

2.1 The Hot Carrier Injection Induced Degradation in MOS Transistors with Subthreshold Hump and the Corelated Impacts on Low Frequence Noise for Low Power Analog Designs 19
Wuxia Li, Kejun Xia[1], Rayne Xu[2], Lie Chao[2]
NXP Semiconductors, Tianjin AIoT Lab
[1]*TSMC, Power Management Business Development*
[2]*NXP Semiconductors, Front End Innovation*

2.2 On-Wafer Characterization of HCI/BTI-induced Threshold Voltage Degradation based Measured Frequency Shift of Ring-Oscillator Circuits 24
Chika Tanaka, Nobuyuki Momo, Fumie Fujii, Osamu Kobayashi
Memory Division, Kioxia Corporation, Yokohama, Japan

2.3 SiC DMOSFET Real Wafer Level HTRB and HTGB Evaluation 29
Ng Hong Seng, Tan Ai Heong[1], Beh Shun Xiar[1], Lee Johhny[2], Lin Jai Wei[1]
X-FAB Sarawak, Kuching, Malaysia
[1]*Nexustest, Singapore*
[2]*X-FAB Texas, Lubbock, TX, USA*

2.4 Novel Fractal Points Implementation for Electron Beam Inspection (EBI) and Data Analysis 33
Po Jen Mo, Tsan Yu Ho[1], Tomoya Asano[1], Xing Ji[2]
Micron Technology, Taichiung City, Taiwan, R.O.C.
[1]*Micron Technology, Higashi Hiroshima-shi,Japan*
[2]*Micron Technology, Singapore, Singapore*

2.5 Withdrawn

Session 3: Device Characterization

3.1 Withdrawn

3.2 D-Mode GaN/AlGaN/GaN MOS-HEMT Test Structures for Evaluating Gate Dielectric Impact on Device Performance 43
Andres S. Aguirre-Sanchez, Rajni Aggarwal, Chadwin D. Young, Rodolfo A. Rodriguez-Davila, Jonathan Anderson[1], Edwin L. Piner[1], Manuel A. Quevedo
Materials Science & Engineering, University of Texas at Dallas, Richardson, TX, USA
[1]*Materials Application Research Center Texas State University, San Marcos, TX, USA*

3.3 TACHI: Tests as a Chip Identifier 47
Ryosuke Sada, Ryo Shirai, Michihiro Shintani[1], Takashi Sato
Kyoto University, Kyoto, Japan
[1]*Kyoto Institute of Technology, Kyoto, Japan*

3.4 Reducing Short-Circuit current of CMOS Inverter circuits with “PN-Body Tied SOI-FET” 53
Kazuki Nakahashi, Takayuki Mori, Jiro Ida
Kanazawa Institute of Technology, Nonoichi, Japan

Session 4: Design & Layout

4.1 Layout experiments and test structures to characterize Local Layout Effects due to mechanical stress in FinFET transistors 59
Angelo Rossoni, Tomasz Brozek[1], Sharad Saxena[2], Rajesh Khamankar[2], Christopher Hess[1], Jurcy Huang[3], Yuchen Teng[3], Zsolt Kovacs-Vajna[4], Michele Quarantelli
PDF Solutions, Inc., Brescia, Italy
[1]*PDF Solutions, Inc., Santa Clara, CA, USA*
[2]*PDF Solutions, Inc., Dallas, TX, USA*
[3]*PDF Solutions, Inc., Hsinchu, Taiwan*
[4]*Dept. of Information Engineering, University of Brescia, Brescia, Italy*

4.2 Estimating Verticality Parameters in Deep Reactive Ion Etching using MEMS Oscillators 63
Shun Yasunaga, Yoshio Mita
The University of Tokyo, Tokyo, Japan

4.3 Non-uniformities in MOSFET-array characteristics caused by probe-induced mechanical stress 68
Pablo Sarazá-Canflanca, Xue Fan[1], Simon Van Beek, Erik Bury, Ben Kaczer
imec, Leuven, Belgium
[1]*Chengdu Technological University, Sichuan, China*

4.4 Methodology and Test Structures for Studying β-Ga_2O_3 Dielectric and Contact Interfaces 74
A. A. Gruszecki, J. Roy, K. S. Agrawal[1], P. La Torraca[1], K. Cherkaoui[1], P. K. Hurley[1], R. M. Wallace, C. D. Young
Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, TX, USA
[1]*Tyndall National Institute, University College Cork, Cork, Ireland*

Session 5: RF & Power

5.1 A new test structure for charge pumping current measurement in vertical Si power device 83
Tatsuya Ohguro, Kohei Oasa, Takuya Yasutake, Takuma Hara, Tatsuya Nishiwaki, Kenya Kobayashi, Hiroaki Kato
Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage Corporation

5.2 A Novel Separated Source Electrodes Kelvin (SSEK) Structure for Extracting Channel Mobility in the 4H-SiC VDMOSFET 87
Wen-Shu Chen, An-Ching Li, Chia-Lung Hung[1], Yi-Kai Hsiao[1], Bing-Yue Tsui
Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan, R.O.C.
[1]*Semiconductor Research Center, Hon Hai Research Institute, Hsinchu, Taiwan, R.O.C.*

5.3 Modified Angelov Model with Improved Accuracy for RF GaN-on-Si HEMTs 91
David C. Chen, Min Li Chou, Kerwin Lin, Mike Hsieh, Perry Lin, Heng Ching Lin, Kevin Lee, Alex Hou, Barry Lin, M. C. Lai
Wavetek Microelectronics Corporation (WTK), HsinChu, Taiwan

5.4 Passive and Causal Modeling of 300-GHz-Band IC Capacitors Using Rational Polynomial Approximation 95
Shun Beppu, Yuto Hirayama, Shinsuke Hara[1], Akifumi Kasamatsu[1], Yoshio Mita[2], Kyoya Tkano
Department of Electrical Engineering, Tokyo University of Science, Chiba, Japan
[1]*National Institute of Information and Communications Technology, Tokyo, Japan*
[2]*Department of Electrical Engineering, Tokyo University of Science, Tokyo, Japan*

Session 6: Cryogenic Measurements

6.1 Oscillation in Cryogenic DC Measurements of High Power LDMOS Devices and Solution 101
Yili Wang, Kejun Xia[1], Guofu Niu, Michael Hamilton, Xu Cheng[2]
Alabama Micro/Nanoelectronics Science and Technology Center, Auburn University, Auburn, AL, USA
[1]*TSMC, Taiwan, R.O.C.*
[2]*NXP Semiconductors, Arizona, USA*

6.2 Measurement of Subthreshold Current Variability at 1.5 K Using Addressable MOSFET Array 106
Tomoko Mizutani, Kiyoshi Takeuchi, Takuya Saraya, Hiroshi Oka[1], Takahiro Mori[1], Masaharu Kobayashi[2], Toshiro Hiramoro
Institute of Industrial Science, The University of Tokyo, Tokyo, Japan
[1]*National Institute of Advanced Industrial Science and Technology (AIST), Ibaraki, Japan*
[2]*Systems Design Lab (d.lab), The University of Tokyo, Tokyo, Japan*

6.3 Hysteresis-Induced Neuromorphic Behavior in 180nm Bulk PMOS Devices at 3K 111
Fiheon Imroze, Bhavani Yalagala, Meraj Ahmad, Mostafa Elsayed, Robert Graham, Giuseppe Colletta, Hadi Heidari, Martin Weides
James Watt School of Engineering, University of Glasgow, Glasgow, United Kingdom

Session 7: Process Characterization

7.1 A Test Structure for Analyzing Self-Heating Induced Distortion in On-Chip Current Sensing Resistors 119
Heng Ma, Shoubhik Karmakar, Huajun Zhang, Yuyan Liu, Haidong Guo[1], Marco Berkhout[2], Qinwen Fan
Delft University of Technology, Delft, The Netherlands
[1]*ams OSRAM, Plano, TX, USA*
[2]*Monolithic Power Systems, Enschede, The Netherlands*

7.2 Novel Test Structures for 3D NAND Array Plasma Damage Monitoring 124
Keerti Kalia, Roberta Rita Bottini[1], Ken Marr, Allen Mcteer, Cheah Zhin Mow[2], James Davis
Micron Technology, Inc., Boise, ID, USA
[1]*Micron Technology, Inc., Vimercate, Italy*
[2]*Micron Technology, Inc., Singapore*

7.3 Advantage and Challenge of Electrical Critical Dimension Test Structures for Electroplated High Aspect Ratio Nano Structures (HARNS) on Insulating Materials 129
Yoshio Mita, Ayako Mizushima, Noriko Kawai[1], Tsuboi Shinji[1], Yurie Inoue[1], Etsuko Ohta[1], Shun Yasunaga, Ryosho Nakane[1], David Bourrier[2], Amel Beghersa[2], Hugues Granier[2], Akio Higo[1]
Department of Electrical Engineering and Information Systems, the University of Tokyo, Tokyo, Japan
[1]*Systems Design Lab (d.lab), School of Engineering, the University of Tokyo, Tokyo, Japan*
[2]*LAAS-CNRS, Toulouse, France*

7.4 Fabrication of NbO_2 based IMT Selector Devices via 300mm Based Memory Test Vehicle 133
Karsten Beckmann, Martin Rodgers, Theodore Wallach[1], Ross Paries[1], Nathaniel Cady[1]
NY CREATES, Albany, NY, USA
[1]*College of Nanotechnology, Science, and Engineering, University at Albany, Albany, NY, USA*

Session 8: Test Optimization

8.1 Smart Diagnostics for 3D CFET: A Machine Learning Approach to Failure Analysis 143
Jerome Mitard, Husnu Murat Kocak[1], Thomas Chiarella, Cassie Sheng[2], Steven Demuyck[2], Naoto Horiguchi[2]
Compute Technology Device Department, IMEC, Belgium
[1]*Imec & Department of Computer Science, KU Leuven, Belgium*
[2]*Process Integration Department, IMEC, Belgium*

8.2 Automatic PSP MOSFET model card extraction powered by deep learning 147
Alba Ordonez Rodriguez, Fabien Gilibert, Francois Paolini, Alan Gerard;Elouan Vincent, Nicolas Derrier, Matthieu Quoirin, Pascal Urard, John Samuel, Remy Cellier[1], Lioua Labrak[1], Nacer Abouchi
STMicroelectronics, Crolles, France
[1]*CPE Lyon - LIRIS CNRS UMR 5205, University of Lyon, Lyon, France*

8.3 Active Sampling of Electrical Characterization Parameters for Efficient Measurement 151
Husnu Murat Kocak, Jerome Mitard[1], Ahmet Teoman Naskali[2], Jesse Davis
Department of Computer Science, KU Leuven, Belgium
[1]*Compute Technology Device Department, IMEC, Belgium*
[2]*Department of Computer Engineering, Galatasaray University, Turkey*

8.4 Test Accuracy Improvement of Ensemble Gaussian Process-based IC Outlier Detection Using Temporal Similarity among Wafers 157
Daisuke Goeda, Tomoki Nakamura[1], Masuo Kajiyama[1], Makoto Eiki[1], Hajime Takayama, Takashi Sato[2], Michihiro Shintani
Graduate School of Science and Technology, Kyoto Institute of Technology, Kyoto, Japan
[1]*Sony Semiconductor Manufacturing Corporation, Isahaya-shi, Japan*
[2]*Graduate School of Informatics, Kyoto University, Kyoto, Japan*

8.5 Evaluation of Rapid Vt testing of Wafer-Level MOSFETs. 163
Michael H. Herman, Ben Morris
Parametric Test Group, Advantest America, San Jose, CA, USA

Session 9: MEMS & Sensors

9.1 Microheater integration in gate dielectric functionalized IGZO thin film transistors for methanol sensing 173
M. Calderon-Gonzalez, M.L. Tietze[1], S. Mondal, E. Georgitzikis, D. Cheyns[1], R. Ameloot[2], J. Genoe
imec, Leuven, Belgium
[1]Department of Microbial and Molecular Systems (M2S), KU Leuven, Belgium
[2]Department of Electrical Engineering (ESAT) KU Leuven, Belgium

9.2 Enhanced Permittivity in PEALD Al_2O_3/TiO_2 Nanolaminates: Investigating Maxwell-Wagner and Interfacial Polarization in IDEs 179
Z. Mousavi Karimi, J. A. Davis
Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA

9.3 Planar FDSOI Reconfigurable Schottky Barrier FETs for Gas Sensing 183
Andreas Kramer, Tillmann Krauss, Maximilian Reuter, Julian Kulenkampff, Dominic Korner, Klaus Hofmann
Integrated Electronic Systems Lab, Technical University of Darmstadt, Darmstadt, Germany

Author Index 188

Technical Program Committee

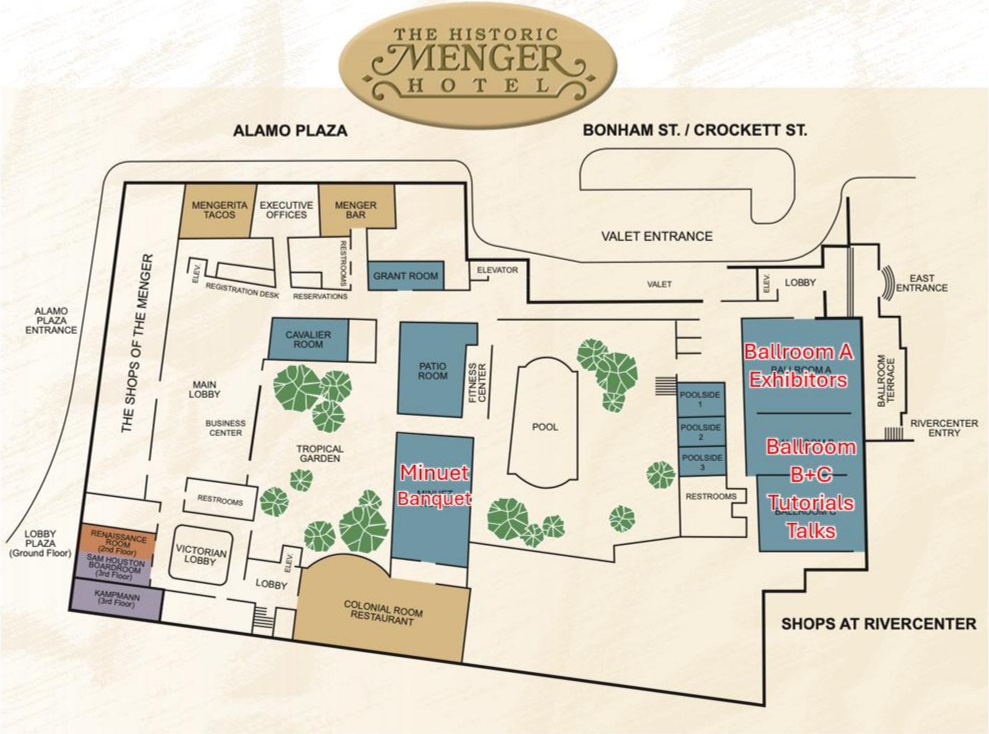
Alexey	KOVALGIN	U. Twente
Bing-Yue	TSUI	National Chiao Tung U.
Chadwin	YOUNG	U. Texas Dallas
Choong ho	LEE	IBM
Christopher	HESS	PDF Solutions
Colin	MCANDREW	NXP Semiconductors
Dennis	PRETTI	Micron
Francesco	DRIUSSI	U. Udine
Hi-Deok	LEE	Chungnam National U.
Jerome	MITARD	IMEC
Johan	KLOOTWIJK	Philips Research
Jonathan	TERRY	U. Edinburgh
Jun	Taniguchi	Keysight Japan Int’l.
Kejun	XIA	TSMC
Kevin	MCCARTHY	U. College Cork
Kiyoshi	TAKEUCHI	U. Tokyo
Luca	Pirro	Global Foundries
Mark	POULTER	Texas Instruments
Matt	RERECICH	Skyworks Solutions
Sebastien	HAENDLER	STMicroelectronics
Takayuki	MORI	Kanazawa Inst. of Tech.
Veda	Sandeep	Tyndall
Wuxia	LI	NXP Semiconductors
Yu-Hsing	CHENG	On Semi
Yuzo	FUKUZAKI	Rapidus

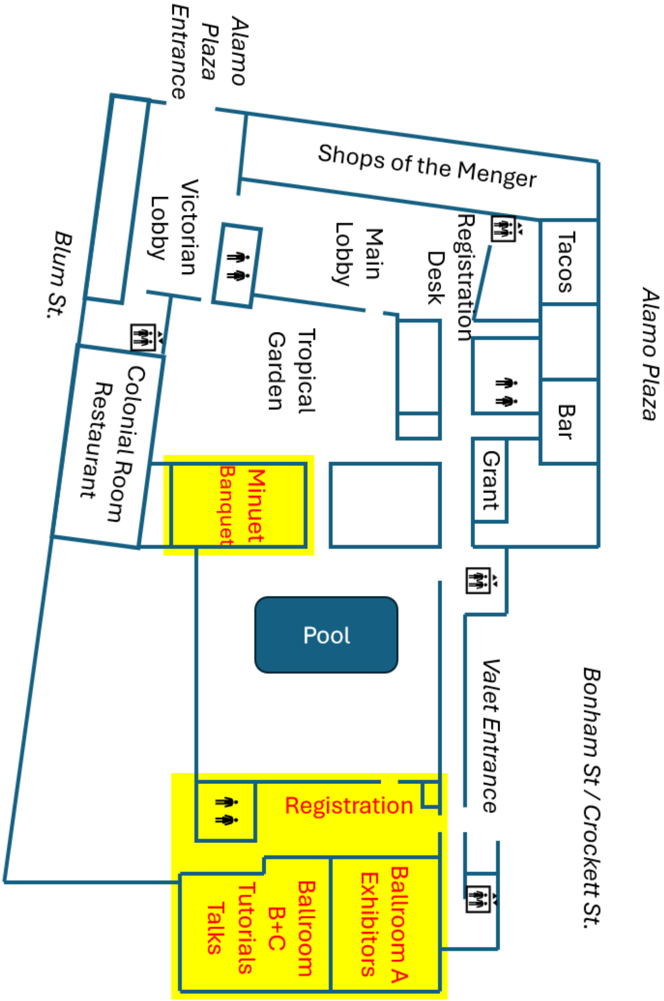
Steering Committee

Bill	VERZI	Emeritus
Brad	SMITH	Emeritus
Carlo	CAGLI	STMicroelectronics
Larg	WEILAND	PDF Solutions
Stewart	SMITH	U. Edinburgh
Tatsuya	OHGURO	Toshiba Corp.
Yoshio	MITA	U. Tokyo

2025 Executive Committee

General Chair	Chadwin Young (Univ. of Texas at Dallas)
Technical Prog Chair	Dennis Pretti (Micron)
Tutorial Chair	Kejun Xia (TSMC)
Exhibition Chair	Ben Morris (Advantest Corporation)
S Steering Committee	Bill Verzi (ICMTS Steering Committee)
S Steering Committee	Larg Weiland (PDF Solutions)
Website	Brad Smith (Emeritus)


THE HISTORIC
MENGER
HOTEL
ALAMO PLAZA
BONHAM ST. / CROCKETT ST.
VALET ENTRANCE
ALAMO PLAZA ENTRANCE
THE SHOPS OF THE MENGER
MENGERITA TACOS
EXECUTIVE OFFICES
MENGER BAR
ELEV.
REGISTRATION DESK
RESERVATIONS
RESTROOMS
GRANT ROOM
ELEVATOR
VALET
ELEV.
LOBBY
EAST ENTRANCE
CAVALIER ROOM
PATIO ROOM
FITNESS CENTER
POOL
MAIN LOBBY
BUSINESS CENTER
TROPICAL GARDEN
RESTROOMS
Minuet Banquet
POOLSIDE 1
POOLSIDE 2
POOLSIDE 3
RESTROOMS
Ballroom A Exhibitors
BALLROOM A
Ballroom B+C
Tutorials
Talks
BALLROOM TERRACE
RIVERCENTER ENTRY
LOBBY PLAZA (Ground Floor)
RENAISSANCE ROOM (2nd Floor)
SAM HOUSTON BOARDROOM (3rd Floor)
KAMPMANN (3rd Floor)
VICTORIAN LOBBY
ELEV.
LOBBY
COLONIAL ROOM RESTAURANT
SHOPS AT RIVERCENTER



Shops at Rivercenter
(Large shopping area with access to RiverWalk)