36th ICMTS

2024 IEEE International Conference on Microelectronic Test Structures

April 15–18, 2024

Sponsored by:
The IEEE Electron Devices Society

THE UNIVERSITY *of* EDINBURGH
School of Engineering

Contents

WELCOME LETTER

Dear Colleagues,

On behalf of the organising committee of the 2024 IEEE International Conference on Microelectronic Test Structures I would like to thank you for your interest in the conference. As many of you will know the 2020 conference was originally intended to take place in Edinburgh before we forced to move to an online meeting by the global pandemic. I am very grateful to the ICMTS steering committee, which I have recently joined, for the opportunity to have another chance to chair the conference in the city I call home.

The conference is being run in co-operation with the University of Edinburgh and is co-sponsored by the IEEE Electron Devices Society. As in 2020 we have had invaluable support from the EDS, and the IEEE Meetings and Conferences Team, in organising the event. I would also like to thank the other members of ICMTS Steering Committee and our local organising team in the School of Engineering for their help, it would not have been possible without them.

My first ICMTS was Göteborg in 1999 when I was a first year PhD student and a very nervous public speaker. I have attended all but one of the (in person) conferences since then and it's always a high point of the year for me. Over the last three decades the conference has provided an invaluable forum for designers and users of test structures while the microelectronics industry has matured and changed. The biggest change in the conference content is probably the increasing number of papers focussing on the fabrication of micro and nano-systems including micromechanical systems, novel sensors etc. alongside the more traditional topics concerning advanced microelectronic processes. Other hot topics in recent years have included non-volatile memories and memristor technologies, silicon photonics and, most recently the application of artificial intelligence and machine learning techniques to semiconductor test and measurement. The ability of ICMTS delegates to apply their expertise in test and measurement to new technologies and applications is extremely exciting to see and bodes well for the future of the conference.

I look forward to welcoming authors, delegates and exhibitors to Edinburgh for ICMTS 2024. Thank you again for your support in making the conference a success.

Sincerely,

Stewart Smith,
General Chair.

GENERAL INFORMATION

Conference Information

The 2024 IEEE International Conference on Microelectronic Test Structures is financially sponsored by the IEEE Electron Devices Society. The conference is also being supported by the School of Engineering at the University of Edinburgh. The purpose is to bring together designers and users of test structures to discuss recent developments and future directions.

Website and Email Contacts

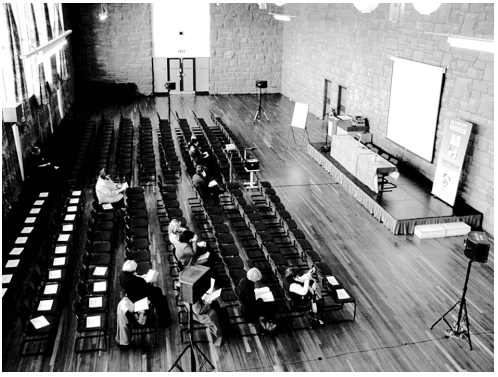
ICMTS Website:
www.icmts.net

Email Contact:
icmts@ed.ac.uk

Presentations

The official language of the conference is English. This year all presentations will be oral and the time allowed for each speaker is 15 minutes. Extended invited presentations will be around 30 minutes.

Both the tutorial and the technical sessions will be held at the University of Edinburgh's South Hall Complex, on the Pollock Halls campus.



South Hall Complex

A PC with Microsoft Powerpoint and Adobe DC will be available in the conference hall. It is highly recommended that this PC is used to facilitate smooth transitions between presentations. All presentation materials should be sent to icmts@ed.ac.uk before the 29th March 2024. In addition, all presenters are requested to bring the original files as backup. For compatibility reasons please use .pptx or .pdf formats for presentations.

Best Paper Award

The best paper will be announced shortly after the end of the conference and the award will be made at ICMTS 2025.

Conference Proceedings

The conference proceedings will be published in electronic format and as an optional printed proceedings. PDF files of all accepted papers will be available to those who have registered. Printed copies of the proceedings may be ordered as an optional extra when registering for the conference for £20 per copy. Limited numbers of printed proceedings will be available to purchase on site at the conference.

Conference Registration

Registration Fees

Advanced Registration (Before March 7th, 2024)

	Member*	Non Member	Student**
Tutorial	£250	£270	£120/£150
Technical Sessions	£450	£500	£250/£300

Regular Registration (Before March 29th, 2024)

	Member*	Non Member	Student**
Tutorial	£250	£270	£120/£150
Technical Sessions	£500	£550	£300/£350

* Must be a member of the IEEE

** Lower prices for student members of IEEE

Registration fees include admission to the tutorial or technical sessions, equipment exhibits, morning and afternoon coffee breaks, the welcome reception and other social events, lunches (Monday – tutorial, Tuesday, Wednesday and Thursday – conference) and the conference banquet. It also includes a copy of the proceedings on a USB drive.

Payment of Registration Fees

Payment should be made using the University of Edinburgh's on-line payments system:

ePay Website

The conference epay page can also be accessed via a link on the ICMTS website:

www.icmts.net

There is an option to request payment via invoice which will be available until the 14th of March. After this date only card payments will be available until registration closes. Registration after 29th of March cannot be guaranteed, please contact registration.ICTMS@ed.ac.uk before this date if you need more time.

Registering for the conference will allow you to add the option of a printed proceedings. There will also be the option to sign up for the optional excursion for no extra charge.

Equipment Exhibition

During the conference an equipment exhibition will be held in the Kirkland Room at South Hall. The exhibition will display equipment and systems closely associated with the design, fabrication, analysis and characterisation of test structures. This equipment exhibition will permit one-on-one discussions between exhibitors and conference attendees on the latest test equipment. The exhibition opening times are given below along with a preliminary list of exhibitors. The full list will be distributed at the conference.

April 15	13:00–17:00	Set up – Tutorial
April 16, 17	9:00–17:00	Conference
April 18	9:00–12:00	Conference and Close-down

Exhibitors and Sponsors List

Gold Sponsors

- Advantest Corporation
- Suzhou Eoulu System Integration Co., Ltd.
- Celadon Systems Inc.

Standard Sponsors

- FormFactor Inc.
- Keysight Technologies
- MPI Corporation
- HProbe GmbH

Information correct at time of press.

Conference Banquet

The conference banquet will take place on Wednesday 17th of April at the Dovecot Studios, Infirmary Street, Edinburgh. This building was formerly a public swimming baths built in 1885 and taken over by the Dovecot tapestry studios trust, reopening in 2008 in the current form.

The conference registration fees include one banquet ticket. Guest tickets will be available for sale at the registration desk for £90.

Excursion

Following the end of the conference on Thursday the 18th of April there is the chance to take part in an excursion, a bus tour to sites of interest near Edinburgh, including the Falrkirk Wheel canal boat lift, the Kelpies sculptures and the Forth bridges view point. The current plan is to leave at after lunch at around 13.30, returning to the conference venue around 18.00.

If you would like to take part in the excursion please express an interest when registering for the conference.

Edinburgh Information

The historic city of Edinburgh is dominated by the Castle, standing high above the surrounding area on the Castle Rock. This is one of two extinct volcanos in the city, the other being Arthur's Seat. Princes Street lies directly beneath the castle with Princes Street gardens separating the two. This makes Edinburgh perhaps unique with its main shopping street having buildings on only one side of the road.

At opposite ends of the famous Royal Mile are the Castle and Holyrood Palace. The Palace is the Edinburgh home of the British Royal Family and is open to visitors when they are not in residence.

Being the capital city, Edinburgh has all the expected amenities such as museums, art galleries, theatres, and gardens as well as being surrounded by a large number of golf courses. Within a short drive is beautiful countryside and coastline together with many historic houses and castles. A few hours drive away is the North of Scotland with the magnificent scenery provided by the mountains, lochs, and islands of the West coast.

Edinburgh City Map

The Edinburgh city map on the next page shows the main buildings of Edinburgh University, including the College of Science and Engineering at the King's Buildings to the south of the city centre.

The conference venue is at the south end of the Pollock Halls site. Google Maps Link, What3Words:picked.skills.riches

Accommodation

There are many hotels, guest houses, and bed and breakfasts located close to the conference venue. In addition there are two hotels, The Scholar and The Scott, on the Pollock Halls campus. More details can be found here: https://www.uoecollection.com/. Conference delegates may be able to get a discounted rate by using the promotion code "EVENT" when booking, but this is subject to availability.

Climate

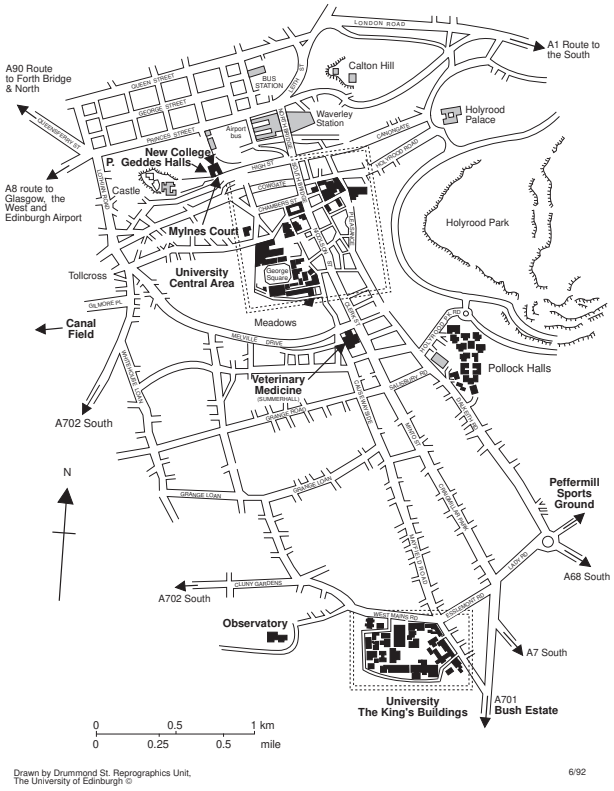
The Scottish climate is not renowned for being the most consistent in the world and the temperature in Edinburgh in early April can vary from around 11°C (52 F) to as low as 4°C (39 F) so it is worth bringing warm clothing. Being in the East, the rainfall is much lower than on the West coast of the UK, averaging around 39mm/1.5" in April. That coupled with the fact that Edinburgh can be quite windy means that an umbrella may not be terribly useful.

Transportation

Air

Edinburgh International Airport has regular services to many UK and international destinations. There are regular bus services (Airlink 100) into the city centre (£5.50 single, £8.00 return). There is also a tram service from the Airport to the City Centre (£7.50 single, £9.50

THE UNIVERSITY OF EDINBURGH
Map 1 : the University and the city



return) More information on the airport and transport links can be found at:

www.edinburghairport.com
www.lothianbuses.com/our-services/airport-buses/
edinburghtrams.com

Rail

All trains arrive at Waverley Station in the centre of the city, although some trains also stop at Haymarket, which is a smaller station in the West end. Walking from Waverley to the central University areas takes approximately 15 minutes, and there are good bus connections to take you further afield.

For comprehensive train information: www.nationalrail.co.uk

Edinburgh Waverley information: www.scotrail.co.uk/plan-your-journey/stations-and-facilities/edb

Travel Within the City

Lothian Buses provide the main bus services within the City of Edinburgh. Their website (www.lothianbuses.com/) provides a journey planner. The buses do not give any change - the single flat rate fare for anywhere in the city is £2 while a day ticket is £5.00. Depending on your bank card you may be able to pay using a contactless payment, this is capped at a maxmimum of £4.80 per day.

Buses that run close to Pollock Halls include the 2, 14, 30 and 33 on Dalkeith Road, and a number of different buses which run along Newington Road (A701), such as the 3, 5, 7, 8, 29, 31, 37, 47 and 49.

TUTORIALS

Tutorial Lecturer Biographies

Prof Yoshio Mita

Professor Yoshio Mita (Senior Member, IEEE) is a full professor of the University of Tokyo, department of Electrical Engineering and Information Systems. He obtained his Bachelor, Master, and Ph.D all from Department of Electrical Engineering of the University of Tokyo in 1995, 97, and 2000. He has been working for 30 years on intelligent integrated CMOS-MEMS VLSI systems. While leading his research work, he has also created a big open-use cleanroom facility of the University of Tokyo with VLSI Design and Education Centre (VDEC, now Systems Design Lab., d.lab). He is an active committee member of ICMTS since 2004, and currently is also serving as a steering committee member.

Prof Daniel Alquier

Daniel Alquier has more than 25 years' experience in micro- and nano-electronics. He is working on wide band semiconductors (SiC / GaN) for power devices and acoustic MEMS (Si /SiC). He has worked or led for GREMAN (Tours University/CNRS) more than 30 research projects (@ Europe, national (ANR, PIA) or regional levels). He has also a long experience of research management both in projects or as former lab director and research vice-president. He is author or co-author of more than 180 papers in international journals, 25 invited talks in international conferences and 8 patents (with 5 on cMUT technology). Google Scholar

Prof Themis Prodromakis

Themis holds the Regius Chair of Engineering at the University of Edinburgh and is Director of the Centre for Electronics Frontiers. His work focuses on developing metal-oxide Resistive Random-Access Memory technologies and related applications and leads an interdisciplinary team comprising 40 researchers with expertise across materials process development to electron devices and circuits and systems for embedded applications. He holds an RAEng Chair in Emerging Technologies and is Adjunct Professor at UTS Australia and Honorary Fellow at Imperial College London. He is Fellow of the Royal Society of Chemistry, the British Computer Society, the IET and the Institute of Physics. He served as the Director of the Lloyds Register Foundation International Consortium for Nanotechnology and Co-Director of the UKRI Centre for Doctoral Training in Machine Intelligence for Nano- Electronic Devices and Systems (MINDS). In 2015, he established ArC Instruments Ltd that delivers high-performance testing infrastructure for automating characterisation of novel nanodevices in over 21 countries and in 2019 he founded SoneT.ai that is building new power-efficient AI hardware solutions. His contributions in memristive technologies and applications have brought this emerging technology one step closer to the electronics industry for which he

was recognised as a 2021 Blavatnik Award UK Honoree in Physical Sciences and Engineering.

Dr Elisa Vianello

Elisa is a senior scientist at CEA-Leti. Her primary research interests revolve around the development of new technologies for bio-inspired neuromorphic computing, with a particular focus on resistive switching memory devices. In 2022, Elisa was awarded an ERC Consolidator Grant for her research on "Heterogeneous integration of imprecise memory devices to enable learning from a very small volume of noisy data". She she has been a member of the VLSI Technical Program Committee (TPC) since 2023.

Elisa obtained her Ph.D. in Electrical Engineering jointly from the Università degli Studi di Udine (Italy) and the Grenoble Institute of Technology (INPG, France) in 2010.

Dr Andrej Rumanstiev

Andrej Rumiantsev received Diploma-Engineer degree (with highest honors) in Telecommunication systems from the Belarusian State University (BSUIR), Minsk, Belarus, and the Dr.-Ing. Degree (with summa cum laude) in Electrical Engineering from Brandenburg University of Technology (BTU) Cottbus, Germany, in 1994 and 2014, respectively.

He joined SUSS MicroTec Test Systems (from 2010 Cascade Microtech) in 2001, where he held various engineering product management and marketing positions. He significantly contributed to developing the RF wafer probes, wafer-level calibration standards, calibration software, and probe systems. Dr. Rumiantsev is currently with MPI Corporation, holding the position of Director of RF Technologies of the Advanced Semiconductor Test Division. His research interests include RF calibration and wafer-level measurement techniques for advanced semiconductor devices.

Dr. Rumiantsev is a member of the IEEE MTT-3 Microwave Measurements Committee, the chair of IEEE MTT-S P2822 Working Group "Recommended Practice for Microwave, Millimeter-wave and THz On-Wafer Calibrations, De-Embedding and Measurements" and the ExCom member of the Automatic RF Techniques Group (ARFTG). He holds multiple patents in wafer-level RF calibration and measurement techniques. His doctoral thesis "On-Wafer calibration techniques enabling accurate characterization of high-performance silicon devices at the mm-wave range and beyond" was awarded as "Best Dissertation of 2014 at Brandenburg University of Technologies".

Dr Alexandru Romanescu

Alexandru Romanescu received his Eng. degree from the Technical University of Bucharest, Romania (2008) and Ph.D. from the University of Grenoble, France (2011). He started his industrial career in ST Microelectronics as Characterization and Modelling Engineer. Later, he joined GlobalFoundries as Device Integration Engineer, working on 28nm & 22nm CMOS process development, with focus on Analog & RF applications. In 2015 he moved to the Netherlands, working on RF

Power technology development and transfer between foundries. Since 2018, he is with SMART Photonics, working to build the 1st InP pure play foundry targeting volume manufacturing. He is currently leading the Design Enablement group.

Tutorial Program

Monday, April 15th

Location: South Hall

08:00–17.00 Registration

09:00 Welcome and Introduction
Johan Klootwijk, Tutorial Chair, *Philips Research, Netherlands*

09:10

1. Fundamentals of Measurement and Test Structures
Prof Yoshio Mita, *University of Tokyo, Japan*
Semiconductor electronics have continuously benefited from mass production due to miniaturization and gave variety of application fields. To increase semiconductor manufacturability, researchers and engineers had to know "what is occurring" in the microelectronic devices. To efficiently measure an extract, in other words, to know through measurements (door meten tot veten), researchers and engineers have developed a variety of test structures. Professor Yoshio Mita, who is known among students to give lectures in an enthusiastic manner, will introduce the history of test structures to inspire researchers and engineers for the future.

10.00 – Coffee

10.30

2. Interest of cMUT technologies : from materials and processes to applications
Prof Daniel Alquier, *Université de Tours GREMAN UMR-CNRS 7347, France*
After introducing MEMS technologies available today, the talk aims to present the history as well as the developments of capacitive Micromachined Ultrasonic Transducer (cMUT) during the last 30 years. We will review device fabrication, investigate the crucial steps through the various processes available to achieve such structures and obtain vibrating systems. We will try to better understand how the technological stages impact on cMUT devices and how to ensure device functionality and reliability. Further, we will review the first application of cMUT devices i.e., medical imaging and, hence, present many others that cMUT's can address successfully. cMUT prospective as well as key issues on new material developments based on SiC technologies and dissemination of cMUT in harsh environment applications, developed in our group, will be presented.

11.20 – Short Break

11:30

3. Memristive Technologies: Testing, Modeling and Applications
Prof Themis Prodromakis, Regius Chair of Engineering,
Centre for Electronics Frontiers, Institute for Micro Nano Systems, University of Edinburgh
Artificial Intelligence (AI) is destined to transform our society, affecting every aspect of our lives. However, a key bottleneck

towards the proliferation of the technology is the lack of efficient hardware that will allow us to embed AI everywhere – well beyond the cloud's reach. Up until now, the processing and storage of data in electronics has relied on assemblies of vast numbers of transistors that have got smaller and smaller to meet the increasing demands of modern societies, but have nowadays reached their physical limits.

A novel nanoelectronic technology, known as the memristor, proclaims to hold the key to a new era in electronics and AI, being both smaller and simpler in form than transistors, low-energy, and with the ability to retain data by 'remembering' the amount of charge that has passed through them – akin to the behaviour of synaptic connections in the human brain. In this tutorial Professor Prodromakis will present the attributes of memristive technologies that make this emerging technology attractive for a variety of applications, along with the tools and techniques developed by his group for exploiting this in wide range of applications –from bio-inspired memories to compressing sensing and AI hardware accelerators.

12.20 – Lunch

13:40

4. The Multifaceted Impact of Resistive Memories on Neuromorphic Systems

Dr Eliza Vianello, *CEA-LETI, France* Resistive random access memory (RRAM) technologies, commonly known as memristors, hold immense potential for revolutionizing neuromorphic and in-memory computing systems. These systems offer significant advantages, such as improved parallelism, reduced power consumption, and minimal latency, particularly in AI workloads. However, practical challenges arising from device variability hinder the implementation of such computational paradigms.

In this presentation, we delve into the exploration of efficient and reliable nanosystems that leverage imprecise devices, blending the fields of neuroscience, computer science, electrical engineering, and device physics. We begin by investigating the incorporation of organizing computational principles inspired by the brain into neuromorphic circuits and architectures. Second, we introduce Bayesian inference, which, although not directly inspired by the brain, has compelling evidence of its utilization in biological intelligence. For example, Bayesian inference is employed in honeybees' decision-making processes, optimizing their food search. Bayesian neural networks, renowned for their ability to handle limited data and uncertainty, offer significant advantages in sensory processing tasks. To address concerns regarding computational intensity arising from their probabilistic nature, we propose harnessing the potential of resistive memory devices. For instance, the variability in memristor resistance can be exploited to represent weight probability distributions.

14.30 – Short Break

14:40

5. Fundamentals of Accurate Wafer-Level Characterization at the RF and mm-Wave Frequencies

Dr Andrej Rumiantsev, *MPI Corporation*
In this workshop presentation, we will be discussing the fundamental principles of making accurate and reliable RF measurements at the wafer-level. We'll delve into the requirements for the probe system architecture, integration of the measurement instrumentation, and related system accessories. Our focus will be on the accuracy of the RF system calibration, which can be impeded by several effects, including unoptimized boundary conditions of calibration standards, unwanted modes propagating in the substrate, the parasitic coupling of calibration standards and RF probe with neighboring elements, specifics of the calibration algorithm used, the impact of temperature, system operator and the laboratory environment, and others. We'll review concepts and essential differences in widely used RF calibration methods and their sensitivity to various parasitic effects. Finally, we'll look at several examples of how to improve the confidence of measured data at the mm-wave frequency range.

15.30 – Coffee

16:00

6. Devices for Photonic Integrated Circuits: from Characterization to Test
Dr Alexandru Romanescu, *SMART Photonics* A process for manufacturing Photonic Integrated Circuits (PICs) is made available for Circuit Design through the means of a PDK (Process Design Kit), comprising a library of Photonic Devices. During the Technology Development phase, these devices are characterized, with the purpose of both optimizing their behaviour, as well as extracting all the information relevant to the design process. This information makes its way in the PDK as raw data, quantitative plots in the Design Manual or Compact Models. During the production phase, the functionality of these devices must be assessed for each manufactured wafer. Efficient test methods are developed to capture the critical-to-quality parameters of each device. Their purpose is to validate the manufactured material (with significantly less resources than a full characterization), as well as to offer statistical means of monitoring and root-cause-analysis during the production ramp-up phase. This course will propose a framework for developing a characterization and test plan, as well as methods to execute these plans, specific to photonic devices.

16.50 – Closing Remarks

WELCOME RECEPTION

Monday, April 6th

Location: South Hall Complex

17:30–19:30 Welcome Reception
All tutorial and conference attendees are welcome to take part in the welcome reception in the exhibition space.

TECHNICAL PROGRAM

Tuesday 16th April

Location: South Hall Complex

08:00–16.00 Registration

09:00 Opening Remarks
Stewart Smith, General Chairman
Francesco Driussi, Technical Program Chairman

SESSION 1: Layout Dependent Effects

09:10–10:10
Co-Chairs: Yoshio Mita, *University of Tokyo, Japan*
Yuzo Fukazaki, *Rapidus US, USA*

09:10

1.1 – Layout Dependent Effects Of Passive Devices And Their Impact On Analog Integrated Circuits
A. Jayakumar, M. van Dort, M. Vertregt, G.D.J. Smit, R. Lander, I. Liu & P. Volf
NXP Semiconductors B.V, Nijmegen, The Netherlands

Analog blocks on products built using advanced CMOS technologies were seen to have deviating behavior on silicon than estimated by post layout simulations, especially in circuits used for biasing and reference generation. Circuit investigations pointed towards trimming resistor banks used for bias and reference current derivation. To detect possible unmodelled silicon effects experienced by these trimming resistor banks having different configurations in various analog blocks on products, a scribe-line test structure was implemented, aimed to capture major product design use-cases and study their effects. The outcome of this study is presented in this paper.

09:30

1.2 – Test structures for studying the impact of the intrinsic contact metallization on the performance and stress sensitivity of SiGe HBTs
O. Dieball[1], H. Tuinhout[1] & Jeroen Zaal[2]
[1]*NXP Semiconductors, Eindhoven, The Netherlands.*
[2]*NXP Semiconductors, Package Innovation, Nijmegen, The Netherlands.*

Based on various layout realizations of a typical SiGe HBT, the electrical impact of the intrinsic contact metallizations as well as their mechanical stress sensitivities are explored. This investigation provides valuable insights into performance shifts, important for design of modelling test structures as well as for high-precision circuit design.

09:50

1.3 – A Step-by-step Layout Transformation Approach for Differentiating the Layout Dependent Effects on Device DC Performance
L. Lu[1], K. Xia[2], R. van Langevelde[1], C. C. McAndrew[1] & W. Li[1]

[1] *NXP Semiconductors, Front End Innovation, China.*
[2] *TSMC, Power Management Business Department*

The ring oscillator is an important component of the electronic device. Its performance, however, is sensitive to parasitic effects when the device sizes scale down to sub-microns. We present a method, utilizing a series of test structures which step-by-step transforms the ring oscillator layout into a single-device modeling layout, to differentiate and quantify the impact of individual layout dependent effects (LDEs) on the device level DC performance. A specially tuned model that fits to the DC performance of the devices in a ring oscillator can give correct timing behavior.

10:10–10:40 Coffee Break

Invited Presentation 1

10:40–11:20
Chair: Stewart Smith

10:40

What do we mean by measurement and can we trust it? - A commentary on the application of measurement process and its association with truth
Prof Pete Loftus
Royal Academy of Engineering Visiting Professor of Instrumentation, Applied Metrology, and Sensing, The University of Edinburgh

The topic of measurement underpins so much of our lives in science and everyday live that it can easily be taken for granted. As tests, and the equipment used in them, become more complex it is difficult to ensure the integrity of the conclusions that we draw from them. In this talk, Pete will draw on over 40 years working on aspects of measurement with a wide variety of stakeholders to take a step back from the applications and to consider measurement itself - what it is, why we do it, and whether we can trust it.

SESSION 2: Reliability

11:20–12:20
Co-Chairs: Francesco Driussi, *Università di Udine, Italy*
Brad Smith, *NXP Semiconductor, USA*

11:20

2.1 – A novel test structure with two active areas for eNVM reliability studies
K. Alkema[1,2], F. Melul[1], V. Della Marca[2], M. Bocquet[2], M. Akbal[1], A. Regnier[1], S. Niel[3] & F. La-Rosa[1]
[1] *STMicroelectronics, Rousset, France.*
[2] *Aix-Marseille University, CNRS, Marseille, France.*
[3] *STMicroelectronics Crolles, France.*

This paper presents a test structure with a poly floating gate shared on two actives areas. Programming and erase can be

split toward these two regions with a specific arsenic implantation. The aim is to study the tunnel oxide degradation and the injection efficiency of embedded charge storage memory cells.

11:40

2.2 – Test Structures of Cross-Domain Interface Circuits with Deep N-Well Layout to Improve CDM ESD Robustness

H.-M. Huang & M.-D. Ker

National Yang Ming Chiao Tung University, Hsinchu, Taiwan

Charged-device model (CDM) electrostatic discharge (ESD) is a complex reliability issue for integrated circuits in advanced CMOS technology. Cross-domain interface circuits are particularly susceptible to CDM ESD during cross-domain ESD events. In this study, CDM ESD robustness of cross-domain interface circuits with deep N-well was investigated through test structures fabricated in a 0.18-µm CMOS technology.

12:00

2.3 – A 4H-SiC Trench MOS Capacitor Structure for Sidewall Oxide Characteristics Measurement

H.-L. Huang, L.-T. Hsuesh, Y.-C. Tu & B.-Y. Tsui

National Yang Ming Chiao Tung University, Hsinchu, Taiwan

Test structure for evaluating gate oxide properties on the trench sidewall in 4H-SiC is proposed. Using the thick bottom oxide and poly-Si spacer structure, we are able to measure the C-V characteristics directly and extract the interface state density. It is observed that typical NO annealing process cannot passivate the trench etching induced defects effectively.

12:20–13:50 Lunch

Exhibitor Session

13:50–14:20 - Presentations by Exhibitors

SESSION 3: Cryogenic Characterisation

14:20–15:20

Co-Chairs: Stewart Smith, *The University of Edinburgh, UK*
Wuxia Li, *NXP Semiconductors, China*

14:20

3.1 – Transistor Matrix Array for Measuring Variability and Random Telegraph Noise at Cryogenic Temperatures

T. Mizutani[1], K. Takeuchi[1], T. Saraya[1], H. Oka[3], T. Mori[3] & M. Kobayashi[1,2]; T. Hiramoto[1]

[1]*Institute of Industrial Science, The University of Tokyo, Tokyo, Japan.*

[2]*Systems Design Lab (d.lab), School of Engineering, The University of Tokyo, Japan.*

[3]*National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Ibaraki, Japan.*

Addressable transistor arrays using 65 nm bulk technology were fabricated and tested at cryogenic temperatures. It was confirmed that variability vs. $1/\sqrt{LW}$ relationships at 1.5 K slightly

degrades compared with 300 K. Random telegraph noise (RTN) was also measured and existence of extremely slow RTN at 1.5 K was confirmed using a quasi-parallel measurement technique.

14:40

3.2 – Gaussian process-based device model toward a unified current model across room to cryogenic temperatures

M. Shintani[1], T. Iwasaki[1] & T. Sato[2]
[1] *Graduate School of Science and Technology, Kyoto Institute of Technology Matsugasaki, Sakyo-ku, Kyoto, Japan.*
[2] *Graduate School of Informatics, Kyoto University Yoshida-hon-machi, Sakyo, Kyoto, Japan*

We apply a Sparse Gaussian process to build a compact model for CMOS circuits operating at cryogenic temperatures. The Sparse Gaussian process prevents overfitting problem unlike neural networks. Evaluation using measurement results of nMOS transistor fabricated by 65 nm demonstrate that the I-V characteristics from 4 K to 300 K are accurately modeled.

15:00

3.3 – A Testbed for Cryogenic On-wafer Noise Measurement Using Cold Source Method with Temperature-Dependent Loss Correction

G.-W. Huang, B.-Y. Chen, Y.-S. J. Shiao, C.-W. Chuang, L.-C. Shen, K.-M. Chen & C.-S. Chiu
Taiwan Semiconductor Research Institute, Hsinchu, Taiwan.

On-wafer noise measurement at cryogenic temperatures is challenging due to complexity of temperature gradient distributions in cryostats. With proposed correction formulas, the cold source method may work properly for cryogenic on-wafer noise measurement and be a good fit for which involves of a large number of samples, e.g., Known-Good-Die Testing.

15:20–15:50 Refreshment Break

Invited Presentation 2

15:50–16:30

Chair: Francesco Driussi, *Università di Udine, Italy*

15:50

Characterization of ferroelectric HfOx-based devices – methods and test structures

Dr Stefan Slesazeck
NaMLab, Dresden, Germany

The discovery of ferroelectricity in doped hafnium oxide that was firstly published in 2011 by Böschke et al. strongly increased the interest in ferroelectric memory devices. The polarization reversal in these thin films is used to store information in three flavors of ferroelectric memory devices – FeCAP, FeFET and FTJ. While the programming of all three devices is performed simply by applying an electrical field being larger than the ferroelectric coercive field, the read operation is very different. Hence, the electrical characterization methodology of

these devices is strongly influenced by the whole device design and material stack, rather than being dictated by the properties of the ferroelectric layer itself. In my talk I will discuss the specific requirements for the ferroelectric device characterization and corresponding test structure designs.

SESSION 4: Dielectrics and Ferroelectrics

16:30–17:30

Co-Chairs: Kjell Jeppson
Chalmers University of Technology, Sweden
Chadwin Young,
University of Texas at Dallas, USA

16:30

4.1 – Analysis and compensation of the series resistance effects on the characteristics of ferroelectric capacitors

M. Massarotto[1], F. Driussi[1], M. Bucovaz[1], A. Affanni[1], S. Lancaster[2], S. Slesazeck[2], T. Mikolajick[2,3] & D. Esseni[1]
[1]*DPIA, University of Udine, Udine, Italy.*
[2]*NaMLab gGmbH, Dresden, Germany.*
[3]*IHM TU Dresden, Dresden, Germany.*

Ferroelectric device optimization requires a dependable characterization of the ferroelectric (FE) material. Here, we highlighted how series resistance (R_S) impacts the I-V characteristics of Metal-Ferroelectric-Metal (MFM) stacks with peculiar distortions, possibly leading to an inaccurate extraction of the FE parameters and a misleading interpretation of its switching dynamics. For the first time to our knowledge, we here propose a procedure for an improved extraction of the FE parameters even in presence of a significant series resistance.

16:50

4.2 – Impedance Measurement Platform for Statistical Capacitance and Current Characteristic Measurements of Arrayed Cells with Atto-order Precision

K. Saito, T. Suzuki, H. Mitsuda, T. Nozaki, T. Mawaki & R. Kuroda
Tohoku University, Sendai, Japan

A novel impedance measurement platform that enables high-precision statistical measurements of C-V and I-V characteristics is presented. The platform consists of $366^{\mathrm{H}} \times 228^{\mathrm{V}}$ cell array and a common readout circuit, and the pre-formed device under test (DUT) cells were measured to verify its measurement performance. The results demonstrated that for about 5,000 DUTs, the C-V measurement can measure fF-order capacitance with 0.06% precision and the I-V measurement can measure fA-order current with 0.6% precision.

17:10

4.3 – Compact expression to model the effects of dielectric absorption on analog-to-digital converters

S. Saro[1], P. Palestri[2], E. Caruso[3], P. Toniutti[3] R. Calabro[3], S. Terokhin[3] & F. Driussi[1]
[1]*DPIA, University of Udine Udine, Italy.*

[2] *University of Modena and Reggio Emilia, Modena, Italy.*
[3] *Infineon Technologies, Villach, Austria*

An analytical model for the dielectric absorption on capacitors and its impact on the errors induced in ADC conversion is here proposed. The reported simulations are consistent with the results of the R-C model widely used in the literature and demonstrate that a large set of experiments can be fitted just calibrating a single model parameter.

Exhibitor and Sponsor Reception

17:30 – 19:30 - South Hall

All conference attendees are invited to take drinks and snacks in the Exhibition Space.

Wednesday 17th April

Location: South Hall Complex

08:30–16.00 Registration

Bonus Talk

09:00 – How to write excellent papers
Dr Carlo Cagli,
STMicroelectronics, France

Invited Presentation 3

09:30–10:10
Chair: Jonathan Terry, *The University of Edinburgh, UK*

09:30

Empowering MEMS Innovation: Bridging Access through EU Access Programmes
Dr Veda Sandeep Nagaraja
Tyndall National Institute, Cork, Ireland

The talk will give a brief introduction to the PiezoMEMS research work being carried out in Tyndall National Institute, Ireland. It will dwell into the technology being developed by the group in various areas like space technology, communication systems and packaging.

The talk will also dwell into how researchers across the globe could be brought together by bridging gap that exists for researchers in terms of research infrastructure availability. Tyndall National Institute is part of many EU Infrastructure access programmes. This talk will give an insight into three such platforms namely:

1. EUROPRACTICE: The platform is popular and provides services on chargeable basis to users. The platform in available for Microelectronics, photonics, packaging and also MEMS.
2. ASCENT+: This is a free of charge infrastructure access programme. Tyndall is the coordinator and the platform provides not just infra structure access but allows the user to collaborate with the access provider.
3. INFRACHIP: This is also a free of charge infrastructure access programme which has commenced from Jan 2024 and will be available for 4 years. This platform provides access to more infrastructure across Europe than ASCENT+. Like ASCENT+ this platform also allows the user to collaborate with access provider and in a larger term than ASCENT+

More details on what is available on each platform and how to access them will be given during the talk.

10:10–10:40 Coffee Break

SESSION 5: MEMs and Sensors

10:40– 12:00

Co-Chairs: Johan Klootwijk, *Philips Research, Netherlands*
Yosio Mita, *University of Tokyo, Japan*

10:40

5.1 – Test structure for chemiluminescence measurement in aqueous solutions: initial design

A. A. Moreno-Guerrero, C. Dunare, A. Walton, P. Lomax, J. Terry & I. Underwood
School of Engineering, The University of Edinburgh, Edinburgh, UK

On-chip integration of sensitive sensors is in high demand due to their extensive applications in chemical analysis. This research introduces a novel test structure for easy opto-electrical integration in microfluidic systems. The architecture has proven versatile for validating the fabrication process and as a final sensor for Luminol-based analysis.

11:00

5.2 – Droplet Impact Sensing with Low Noise Coplanar Reverse-Electrowetting Test Structures

A. Moyo[1], M. W. Shahzad[1], S. Smith[2], J. G. Terry[2], Y. Mita[3], J. Lewis[1] & Y. Li[1]
[1] *Northumbria University, Newcastle, UK.*
[2] *The University of Edinburgh, Edinburgh, UK.*
[3] *The University of Tokyo, Tokyo, Japan.*

Reverse electrowetting on dielectric (REWOD) has emerged to be a promising sensing technology for low frequency vibrations and deformations. This study aims to use test structures to study the parasitic elements in characterising the coplanar electrode (CREW) configuration of REWOD. This allows for better understanding in device design and optimization.

11:20

5.3 – Analysis methodology of Deep Trench Isolation Field-Effect Passivation techniques for Image Sensors through dedicated test structures

S. Tlemsani[1,2], S. Ricq[1], O. Marcelot[2] & P. Magnan[2]
[1] *STMicroelectronics Crolles, France.*
[2] *ISAE, Toulouse, France.*

In this work a new methodology is proposed to characterize the Deep Trench Isolation field-effect passivation thanks to dedicated test structures. Two deep trench isolations are studied and quantitatively compared: an electrically active trench and an innovative passive trench using a charged Al_2O_3/SiO_2 stack. The results show that the best passivation is achieved here with the active trench.

11:40

5.4 – Parametric Optimization of RF MEMS Variable Capacitor with high linearity for C-Band Application

S. Shaheen; P. Lomax; T. Arslan
School of Engineering, The University of Edinburgh, Edinburgh, UK

A design methodology is proposed to obtain a linear C-V response and large capacitance tuning ratio by avoiding the pull-in effect. The study includes structural optimization of RF Microelectromechanical system (MEMS) varactor, using simulation tools ANSYS and HFSS. The optimized design shows better isolation at 4.2 GHz which makes it appropriate for C-Band applications.

12:00–13:30 **Lunch**

13:30–13:40 **ICMTS 2025 Presentation**

SESSION 6: Wafer Measurements

13:40–15:00

Co-Chairs: Francesco Driussi, *Università di Udine, Italy*
Kiyoshi Takeuchi, *University of Tokyo, Japan*

13:40

6.1 – Efficient Characterization Methodology for Low-Frequency Noise Monitoring

L. Pirro[1], T. Chohan[1], P. Liebscher[1], M. Juettner[1], F. Holzmueller[1], R. Jain[1], Y. Raffel[2], K. Seidel[2], R. Olivo[2], A. Zaka[1] & J. Hoentschel[1]

[1] *GlobalFoundries, Dresden, Germany.*

[2] *Fraunhofer-IPMS, Dresden, Germany*

In this work, a novel methodology to characterize the Low-Frequency Noise LFN on large device statistics is proposed. The maximum drain current fluctuations over time are measured. The slope of the LFN distribution is modeled with physical equations related to the basic device properties. The approach is validated by studying the impact of transistor geometry (different gate width, number of fingers and length) as well as gate oxide thickness and characterization temperature. In conclusion, the proposed methodology is tested evaluating different process integration elements. The outcome is compared to classical 1/f read-out for final confirmation.

14:00

6.2 – Rapid MOSFET threshold voltage testing for high throughput semiconductor process monitoring

M. H. Herman, T. T. Nguyen, K. Wong, J. Johnson & B. Morris

Advantest Corporation, San Jose, USA.

We describe a rapid method for testing MOSFET threshold voltage (V_t). Multiple spot I_{ds} measurements are compared to stored reference data. Each spot measurement gives an independent V_t, and multiple V_t estimates are used to generate quality metrics. Two spot measurements permit an accurate V_t within 7 ms.

14:20

6.3 – Statistical investigation of SnOx RRAM memories for switching characteristics

A. G. Panca, A. Serb, S. Stathopoulos & T. Prodromakis

School of Engineering, The University of Edinburgh, Edinburgh, UK

Resistive Random Access Memory (RRAM) has seen significant developments in the past years. An important improvement is to solve the device-to-device variability that limits RRAM implementation. A proposed solution is to measure a high number of devices to statistically identify trends and evidences behind the cause. Here, we present a method to characterise the RRAM switching behaviour and analyse a large dataset of SnOx RRAM, in a statistical fashion for further optimization and modelling.

14:40

6.4 – Making Accurate and Consistent Wafer Measurements with Next Generation Guarded True-Kelvin MEMS DC Probes

C. B. Sia, Y. Funatoko, I. Kunioka, M. Watanabe, P. Andrews, K. Dawson, M. Sameshima, T. Saeki, J. Yang, J. Li, X. Li, S. Guo, L. Fan, W. M. Lim, E. Wilcox, A. Lord, S. Lastella, N. Kawamata, J. Klattenhoff, J. Kister, M. Losey & M. Slessor
FormFactor Inc., Singapore.

As silicon-based transistor scales down, it becomes increasingly challenging for test engineers to perform precise and repeatable waferb measurements. Reducing aluminium-capped copper test pads to 30 µm × 30 µm and smaller means that new test strategies with novel true Kelvin MEMS probes are needed to overcome these emerging test challenges.

15:00–15:20 Coffee Break

Invited Presentation 4

15:20–16:00

Chair: Stewart Smith, *The University of Edinburgh, UK*

15:20

3D interconnects characterization: basic test structures and electrical measurement

Mr M. Stucchi
imec, Leuven, Belgium

3D stacking technology is based on vertical interconnects, as Through-Silicon Vias (TSV), Hybrid Bonding (HB) pads, microBumps (uB). Their function is providing electrical connections among dies stacked vertically for power supply delivery, signal propagation, clock distribution. Low-resistive electrical continuity is the primary requirement of these vertical interconnects; however, parasitic components as resistance at metal interfaces, capacitance between interconnects, leakage current, need to be carefully characterized as well and benchmarked with the requirements of system-level applications of the 3D stacked dies. Furthermore, results of the 3D interconnect characterization are essential information for the optimization of 3D architectures (interconnect dimensions and materials) and processing.

This talk presents examples of 3D interconnect test structures and their relative measurement methodologies; their important role for 3D technology optimization is highlighted by examples of applications and case studies.

SESSION 7: S-Parameters and De-Embedding

16.00–17:00

Co-Chairs: Tatsuya Ohguro *Toshiba Corp., Japan*
Carlo Cagli *CEA-Leti, France*

16:00

7.1 – Understanding the substrate effect on de-embedding structures fabricated on SOI wafers using electromagnetic simulation

B. Neckel Wesling[1,2], M. Deng[2], C. Mukherjee[2], T. Mikolajick[1], J. Trommer[1] & C. Maneux[2],
[1]*NaMLab, Dresden, Germany.*
[2]*IMS, Talence Cedex, France.*

In this paper, we present the fabrication, characterization and electro-magnetic (EM) simulation of open pad test-structures, emphasizing the impact of substrate properties on RF performance. We demonstrate that a high-resistivity substrate is essential to minimize losses and capacitances in RF measurements for technologies using Silicon on Isolator (SOI) wafers.

16:20

7.2 – Modified Bisection Thru-Only Deembedding Algorithm for Long Test Fixtures

A. Quint, L. Valenziano, J. Hebeler, T. Zwick & A. Bhutani
Karlsruhe Institute of Technology, Karlsruhe, Germany

Thru-only deembedding is a simple deembedding method using a single deembedding structure. Common thru-only deembedding methods often have overshoots in the deembedded S-parameters when the deembedding structure is $\lambda/2$ long. This is caused in the bisection step. A modified approach is presented, which extracts the phase of the S-parameters of the deembedding structure before the bisection step, performs the bisection on the magnitude of the S-parameters and applies the phase afterwards again, therefore eliminating the overshoots. The accuracy of the proposed algorithm is verified on measured test structures.

16:40

7.3 – Evaluation of Lab-based Lithium Niobate Surface Acoustic Wave Test Structure Using Efficient Maskless Lithography and SMA Connection Approach for Microfluidic Applications

M. S. Parvez, S. Hussain, M. Goeckner, C. D. Young & J.-B. Lee
The University of Texas at Dallas, Richardson, USA.

Surface Acoustic Wave (SAW) devices, particularly those made of Lithium Niobate ($LiNbO_3$), are extensively used in telecommunications and microfluidic applications. This work describes the fabrication of a $LiNbO_3$-based SAW test structures using maskless photolithography for rapid device dimension changes as well as introduces a cost-effective technique to solder SMA connectors to delicate substrates such as $LiNbO_3$-based SAWs, without the need to fully create printed circuit boards. The SMA connected device facilitated improved characterization results compared to simple copper tape connections. The characterization accuracy is then validated through simulation.

17.00 **End of Session 7**

19.00 **Banquet**

Thursday 18th April

Location: South Hall Complex

09:00–11.00 Registration

SESSION 8: Gallium Nitride Technology

09:30–10:50

Co-Chairs: Johan Klootwijk, *Philips Research, Netherlands*
Kejun Xia, *TSMC, USA*

09:30

8.1 – Test Structures to Investigate ESD Robustness of GaN Devices for Applications of Circuit Integration

W.-C. Wang & M.-D. Ker

National Yang Ming Chiao Tung University, Hsinchu, Taiwan.

ESD robustness of E-HEMT GaN devices was investigated through test structures fabricated in a GaN-on-Silicon process. The experimental results showed that the ESD robustness is proportional to the device dimension when it was operating in the forward mode. In addition, with the gate-coupled design, the ESD level of E-HEMT GaN device can be further improved.

09:50

8.2 – Method for GaN HEMT IV Characterization Without Trap-Related Memory Effects

J. Bremer, N. Rorsman & M. Thorsell

Chalmers University of Technology, Gothenburg, Sweden.

A new method to perform IV output characterizations of FETs is presented, which minimizes the influence of trap-related memory effects. This is achieved by minimizing the charging effects caused by the electric fields of preceding measurement points. The proposed method provides rudimentary IV characteristics, useful for technology evaluation and modeling purposes.

10:10

8.3 – A Neural Network-based Manufacturing Variability Modeling of GaN HEMTs

F. Chavez[1], D. Bavim[1], N. C. Miller[2] & S. Khandelwal[1]

[1] *Macquarie University, Macquarie Park, Australia.*

[2] *Michigan State University, USA.*

A new technique to accurately model the manu- facturing variability of GaN HEMT using neural network (NN) is presented. PCA is used to automatically generate parameters from variations in I-V data, which are then used to train the NN. The trained NN model captures the I-V behavior of 115 GaN HEMT with excellent accuracy.

10:30

8.4 – Use of DC Probes for Multi-MHz Measurements of Crosstalk and Substrate Coupling in Gallium Nitride Power Integrated Circuits

M. Cui & S. Lam

Xi'an Jiaotong-Liverpool University, Suzhou, China.

With simple compact pads, DC probes were used for measurements of crosstalk and substrate coupling in gallium-nitride power integrated circuits. By proper calibration, a crosstalk

voltage down to 4.4 mV and substrate coupling up to −38 dB were measured up to 25 MHz, using an oscilloscope and spectrum analyzer respectively.

10:50–11:20 **Coffee Break**

SESSION 9: Process/Material Monitoring

11:20–12:20

Co-Chairs: Jonathan Terry, *The University of Edinburgh, UK*
Chadwin Young,
University of Texas at Dallas, USA

11:20

9.1 – An add-in Test Structure Chip to Unitedly Assess PVD Material Properties in University Open Nanotechnology Platform

S. Yasunaga, K. Misumi, A. Mizushima, A. Toyokura, E. Ota, Y. Inoue, M. Fujitawa, N. Kawai, M. Yoda, S. Tsuboi, T. Sawamura, A. Higo, R. Nakane, Y. Ochiai & Y. Mita

The University of Tokyo, Tokyo, Japan.

Open nanotechnology platform at universities and research institutes is becoming an essential tool for agile and rapid microelectronic devices research and development. To further extend its capability with more users, process data acquisition and digital transformation (DX) is of high priority. In order to uniformly acquire process data in an open platform, where users' process charts are all different, we are developing an add-on test structure chip. In the conference, we would like to share a chip design and measurement results to assess material parameters deposited by physical vapor deposition (sputtering and evaporation) materials.

11:40

9.2 – Electrical behaviour of ALD-molybdenum films in the thin-film limit

K. van der Zouw, S. D. Dulfer, A. A. I. Aarnink & A. Y. Kovalgin

University of Twente, Enschede, The Netherlands.

The thin-film electrical properties of molybdenum layers grown by atomic layer deposition were determined. Among others, four-point collinear probe, Van der Pauw, and (circular) transfer length method [(C)TLM] structures were designed and fabricated, which allowed to determine the sheet resistance (R_{sh}), temperature coefficient of resistance (TCR), contact resistance (R_c), transfer length (L_T), and the field effect in a few nm thin Mo films.

12:00

9.3 – Test Structure to Assess Bump Shape Influence on Hybrid Bonding

A. Mizushima[1], K. Misumi[1], S. Yasunaga[1], A. Higo[1], R. Nakane[1], K. Tsumura[2], K. Higashi[2], Y. Ochiai[1] & Y. Mita[1]

[1] *The University of Tokyo, Tokyo, Japan.*

[2] *TOSHIBA CORPORATION, Kawasaki, Japan*

Bump bonding is widely used in CMOS-MEMS integration. As compared to the other technology (planar bonding), bump

bonding is more interesting for its simplicity and applicability to wide range of device types. Towards higher density and reliability improvement, the authors have designed and fabricated a test structure. Our new contribution is to intentionally structuralize shapes of bumps to not only a flat head but concave as well as convex ones, expecting better occlusion and passive alignment. To experiment our new idea, the first test structure has been fabricated to assess alignment accuracy and resistance.

12:20 **Best paper announcement and closing remarks**

12:30 **Lunch**

13:30 **Excursion**

CONFERENCE OFFICIALS

Conference Committee

General Chair:

Stewart Smith
Institute for Bioengineering
School of Engineering, The University of Edinburgh
SMC, Alexander Crum Brown Road
Edinburgh, EH9 3FF
Scotland, UK
Tel: +44-(0)-131-650-7471
E-mail: Stewart.Smith@ed.ac.uk

Technical Chair:

Francesco Driussi
DPIA, Università di Udine
Via delle Scienze, 206
33100 UDINE Italy
E-mail: francesco.driussi@uniud.it

Exhibition Chair and Local Arrangements:

Jonathan G. Terry
Institute for Integrated Micro and Nano Systems
School of Engineering, The University of Edinburgh
SMC, Alexander Crum Brown Road
Edinburgh, EH9 3FF
Scotland, UK
Tel: +44-(0)-131-650-5607
E-mail: Jon.Terry@ed.ac.uk

Tutorial Chair:

Johan Klootwijk
Philips Research
High Tech Campus 4
5656 AE Eindhoven,
The Netherlands
E-mail: johan.klootwijk@philips.com

Special thanks to:

Laura Smith, Karen Brocklehurst and Kimberly Ross – *School of Engineering, The University of Edinburgh*
Tracy Marshall – The University of Edinburgh Hospitality and Events Collection

Steering Committee

Yoshio Mita	University of Tokyo	Japan
Carlo Cagli	ST Microelectronics	France
Brad Smith	NXP Semiconductor	USA
Stewart Smith	University of Edinburgh	Scotland
Larg Weiland	PDF Solutions	USA

Technical Committee

Carlo Cagli	CEA-Leti	France
Yu-Hsing Chen	On Semi	USA
Francesco Driussi	Università di Udine	Italy
Yuzo Fukuzaki	Rapidus US	USA
Sébastien Haendler	STMicroelectronics	France
Christopher Hess	PDF Solutions Inc.	USA
Kjell Jeppson	Chalmers University of Technology	Sweden
Chang Yong Kang	Nvidia Corp.	USA
Johan Klootwijk	Philips Research Europe	The Netherlands
Alexey Kovalgin	Univ. of Twente	The Netherlands
Choong-ho Lee	IBM	USA
Hi-Deok Lee	Chungnam National Univ.	Korea
Wuxia Li	NXP Semiconductors	China
Colin McAndrew	NXP Semiconductors	USA
Kevin McCarthy	University College Cork	Ireland
Yoshio Mita	University of Tōkyo	Japan
Jerome Mitard	IMEC	Belgium
Shigetaka Mori	Sony Corp.	Japan
Takayuki Mori	Kanazawa Institue of Technology	Japan
Tatsuya Ohguro	Toshiba Corp.	Japan
Mark Poulter	National Semiconductor	USA
Matthew Rerecich		USA
Brad Smith	NXP Semiconductors	USA
Stewart Smith	University of Edinburgh	Scotland
Kiyoshi Takeuchi	University of Tokyo	Japan
Jonathan Terry	University of Edinburgh	Scotland
Bing-Yu Tsui	National Chiao Tung University	Taiwan, R.O.C.
Larg H. Weiland	PDF Solutions Inc.	USA
Kejun Xia	TSMC	USA
Chadwin Young	University of Texas at Dallas	USA

ICMTS History

No.	Year	Dates	Location	Country
WS	1979	Feb 6–7	San Jose	USA
WS	1984	Feb 20–21	San Diego	USA
WS	1986	Feb 17–18	Long Beach	USA
1	1988	Feb 22–23	Long Beach	USA
2	1989	Mar 13–14	Edinburgh	UK
3	1990	Mar 5–7	San Diego	USA
4	1991	Mar 18–10	Kyoto	Japan
5	1992	Mar 16–19	San Diego	USA
6	1993	Mar 22–25	Barcelona	Spain
7	1994	Mar 21–24	San Diego	USA
8	1995	Mar 22–25	Nara	Japan
9	1996	Mar 25–28	Trento	Italy
10	1997	Mar 17–20	Monterey	USA
11	1998	Mar 23–26	Kanazawa	Japan
12	1999	Mar 15–18	Göteborg	Sweden
13	2000	Mar 13–16	Monterey	USA
14	2001	Mar 19–22	Kobe	Japan
15	2002	Apr 8–11	Cork	Ireland
16	2003	Mar 17–20	Monterey	USA
17	2004	Mar 22–25	Awaji	Japan
18	2005	Apr 4–7	Leuven	Belgium
19	2006	Mar 6–9	Austin	USA
20	2007	Mar 19–22	Tokyo	Japan
21	2008	Mar 24–17	Edinburgh	UK
22	2009	Mar 30–Apr 1	Oxnard	USA
23	2010	Mar 22–25	Hiroshima	Japan
24	2011	Apr 04–07	Amsterdam	Netherlands
25	2012	Mar 19–22	San Diego	USA
26	2013	Mar 26–28	Osaka	Japan
27	2014	Mar 25–27	Udine	Italy
28	2015	Mar 24–26	Phoenix	USA
29	2016	Mar 29–31	Yokohama	Japan
30	2017	Mar 28–30	Grenoble	France
31	2018	Mar 20–22	Austin	USA
32	2019	Mar 19–21	Kita-Kyushu	Japan
33	2020	May 4–18	Virtual	UK
34	2022	Mar 21–Apr 29	Virtual	USA
35	2023	Mar 27–30	Tokyo	Japan
36	**2024**	**Apr 15-18**	**Edinburgh**	**UK**

ICMTS 2024 AT A GLANCE

Monday, April 15

08:00	Registration
09:00	Tutorial Welcome
09:10	Tutorial 1
10:00	Break
10:30	Tutorial 2 & Short break
11:30	Tutorial 3
12:30	Lunch
13:40	Tutorial 4 & Short break
14:40	Tutorial 5
15:30	Break
16:00	Tutorial 6
16:50	Closing Remarks
17:30	Welcome Reception

Tuesday, April 16

08:00	Registration
09:00	Opening Remarks
09:10	Session 1 - Layout Dependent Effects
10:10	Break
10:40	Invited Talk 1
11:20	Session 2 Reliability
12:20	Lunch
13:50	Exhibitor Presentations
14:20	Session 3 - Cryogenic Characterisation
15:20	Break
15:50	Invited Talk 2
16:30	Session 4 - Dielectrics and Ferroelectrics
17:30	Exhibitor Reception

Wednesday, April 17

08:30	Registration
09:00	Bonus Talk
09:30	Invited Talk 3
10:10	Break
10:40	Session 5 - MEMs and Sensors
12:00	Lunch
13:30	ICMTS2024
13:40	Session 6 Wafer Measurements
15:00	Break
15:20	Invited Talk 4
16:00	Session 7 *S*-Parameters and De-Embedding
17:00	End of Session 7
19:00	Banquet

Thursday, April 18

09:00	Registration
09:30	Session 8 Gallium Nitride Technology
10:50	Break
11:20	Session 9 Process/Material Monitoring
12:20	Closing remarks
12:30	Lunch
13:30	Excursion