2023 35th International Conference on Microelectronic Test Structures

Tutorial and Technical Program

March 27-30, 2023

Takeda Hall, the University of Tokyo, Tokyo, Japan

CHAIRMAN'S LETTER

On behalf of the steering and technical program committees, I take pleasure in welcoming you to the 2023 International Conference on Microelectronic Test Structures (ICMTS 2023) at the University of Tokyo in Tokyo, Japan on March 27-March 30, 2023. It is the 35th ICMTS as an international conference and the first in-person ICMTS after the remote ICMTS 2021 and ICMTS 2022 due to COVID-19. The in-person style is much-awaited for many ICMTS lovers since the conference's purpose is to bring together designers and users of test structures to discuss recent development and future directions.

In the past, many topics of the ICMTS were so-called advanced logic or memory technologies related. Many ideas for new test structures and new results were proposed and discussed in the ICMTS for the technologies. I think it was meeting the needs of the times. However, as the semiconductor role is becoming more important and is becoming more diversified, many researchers, engineers, and students have selected different topics for their research. As a result of the changes, topics of the ICMTS have become diversified. Topics of the ICMTS 2023 are the result of the changes and are meeting the needs of the time.

The technical program is scheduled to be held from March 28 to March 30 and consists of nine sessions containing thirty-six contributed papers. The nine sessions cover emerging memory, noise, power devices, measurement technique, matching & variability, yield and device optimization, MEMS & sensors, modeling, and novel materials. In addition to the thirty-six papers, two lecture presentations will be provided on March 29 for young researchers that have not familiar with making better papers and presentations.

On March 27, the conference is preceded by a one-day tutorial short course providing seven topics by a leading expert in each field, which many people are interested in. Two topics cover an introduction to test structure design, measurement, and analysis. The five topics cover the latest update in each field that includes advanced CMOS, Gallium oxide for power devices, CMOS image sensors, 2D/3D Flash memory, and MEMS. The tutorial course will be the best place for many attendees to learn fundamentals on test structures and to catch up on advanced topics in the field.

Tokyo is an endlessly interesting city for everyone. There are many historical places to watch, many artistic places to feel something, many modern and traditional places to find something different from your place, and many places to enjoy eating. Since The University of Tokyo is located in the center of Tokyo, you can easily access the interested places quickly and easily. In addition to the places, the week of the ICMTS 2023 is the typical week that you can enjoy seeing the cherry trees in full bloom.

I look forward to seeing you at the ICMTS 2023 in Tokyo.

Sincerely,

Satoshi Habu

General Chairman

Timetable

Monday, March 27	
8:50	Welcome Address
9:00	Tutorial 1
10:00	Tutorial 2
11:00	Tutorial 3
11:55	Lunch
13:25	Tutorial 4
14:25	Tutorial 5
15:25	Tutorial 6
16:25	Tutorial 7
17:50	Welcome Reception

Tuesday, March 28	
8:50	Greetings
9:00	Session 1: Emerging Memory
11:10	Session 2: Noise
12:10	Lunch
13:40	Exhibitor Presentation
14:10	Session 3: Power Devices
16:20	Session 4: Measurement Technique

Wednesday, March 29	
8:30	Bonus Track 1; How to write better abstracts
9:00	Session 5: Matching & Variability
10:50	Session 6: Yield and Device Optimization
12:10	Lunch
13:40	Bonus Track 2; Making Good Presentations
14:10	ICMTS 2024
14:55	Session 7: MEMS & Sensors
	Banquet

Thursday, March 30	
9:00	Session 8: Modeling
10:30	Session 9: Novel Materials
11:30	Closing
12:00	Excursion tour

Conference

The 2023 35th ICMTS will be held at the University of Tokyo, in Tokyo Japan on March 27 to March 30, 2023. The technical program, which will consist of nine sessions of contributed papers will be held on March 28 to March 30, 2023. A Tutorial Short Course will precede the conference sessions. Several of the best measurement, equipment, design, and manufacturing experts, will participate in the equipment exhibition and presentations.

The ICMTS is the industry's only conference that focuses on test structure design, measurement, and usage. The single-session format allows for interaction with your fellow participants that's not practical at larger conferences.

Presentation

The official language of the conference is English and it will be used for all presentations and printed materials. Only a projector connected to a laptop PC will be available for your presentation. The presentation slides (PDF or PowerPoint files) should be sent to the technical chair by March 23, so that they can be loaded on the PC in advance for a smooth transition between consecutive talks. Please also store the slides in a USB media and bring them by yourself for backup. The speakers are asked to contact to the session chair 10 minutes before the session starts.

Conference Proceedings

Conference proceedings will be prepared. Registered participants for the technical sessions will receive one copy of the proceeding in both printed and electronic forms. Information for downloading the electronic forms will be provided at the registration desk in front of the tutorial & program room. Additional copies will be available for extra fees.

Lecture presentations

Two lecture presentations will be provided on March 29 for young researchers that have not familiar with making better papers and presentations.

Best Paper Award

One paper will be selected as the best paper of the year by the technical committee members and will be announced in the closing session on March 30. The prize will be awarded at the next ICMTS in 2024.

Equipment Exhibition

During the conference, an equipment exhibition will be held beside the conference room. The exhibition will permit one-to-one discussions between exhibitors and conference attendees on the latest equipment and software.
The exhibition will be open as follows:

March 27, 13:00-17:00
March 28, 9:00-17:00
March 29, 9:00-16:30

Presentation by the exhibitors will be presented on March 28.

Conference Reception

A welcome reception will be provided that will start at 17:50 on March 27 at the same place as the tutorial and the technical program. Light meals and drinks will be served.

Banquet

A banquet will be held on March 29 evening at Hotel Chinzanso Tokyo. Following is the web address of the hotel.
https://www.hotel-chinzanso-tokyo.com
Transportation bus from/to the Takeda-hall to/from the hotel will be provided. The bus will leave Takeda-hall at 17:30 to the hotel and will leave the hotel at 21:10 to the Takeda-hall. Travel time is estimated to be 20mins.

Excursion

An excursion tour will be held just after the ICMTS 2023 on March 30. You can check the detail of the tour by checking the following web address.
https://sec.tobutoptours.co.jp/2023/icmts2023/excursiontour.pdf

Registration Fee

Early bird ; 9th Dec to 20th Feb [JPY]

Program	IEEE member	IEEE non member	Student
Tutorial incl. one textbook	21,000	25,000	10,000
Technical incl. one proceeding book & one banquet ticket	44,000	52,000	26,000
Tutorial + Technical incl. one textbook & one proceeding book & one banquet ticket	63,000	75,000	34,000
Extra Baquet Ticket	10,000	10,000	10,000
Excursion Tour	9,800	9,800	9,800

Extra proceeding book will be available for purchase on site at JPY5,000.
To register, Please visit: https://sec.tobutoptours.co.jp/web/evt/icmts2023/

Excursion tour will be held! If you wish to participate, please also purchase a tour ticket when you register. (You can apply for the tour separately. The application deadline for the excursion tour will be announced shortly.)

Regular ; 21st Feb to 20th March [JPY]

Program	IEEE member	IEEE non member	Student
Tutorial incl. one textbook	25,000	29,000	12,000
Technical incl. one proceeding book & one banquet ticket	49,000	57,000	30,000
Tutorial + Technical incl. one textbook &	72,000	84,000	40,000

one proceeding book & one banquet ticket			
Extra Baquet Ticket	10,000	10,000	10,000
Excursion Tour	9,800	9,800	9,800

Extra proceeding book will be available for purchase on site at JPY5,000.
To register, Please visit: https://sec.tobutoptours.co.jp/web/evt/icmts2023/

Excursion tour will be held! If you wish to participate, please also purchase a tour ticket when you register. (You can apply for the tour separately. The application deadline for the excursion tour will be announced shortly.)

On Site ; on 27 March and 28 March [JPY]

Program	**IEEE member**	**IEEE non member**	**Student**
Tutorial incl. one textbook	28,000	33,000	14,000
Technical incl. one proceeding book & one banquet ticket	54,000	62,000	33,000
Tutorial + Technical incl. one textbook & one proceeding book & one banquet ticket	80,000	93,000	45,000
Extra Baquet Ticket	10,000	10,000	10,000
Excursion Tour	9,800	9,800	9,800

Extra proceeding book will be available for purchase on site at JPY5,000.
To register, Please visit: https://sec.tobutoptours.co.jp/web/evt/icmts2023/

Excursion tour will be held! If you wish to participate, please also purchase a tour ticket when you register. (You can apply for the tour separately. The application deadline for the excursion tour will be announced shortly.

Tutorial Short Course

March 27

08:50 Welcome Address

09:00 **Challenges and solutions for characterization of semiconductor device matching and variability**

Hans Tuinhout:

This tutorial will discuss techniques for characterization of small parametric differences of semiconductor components for high-precision analog electronic circuit design. After an introduction on the required orders of magnitude for modeling and characterization, way to look at measurement accuracy and short-term repeatability capabilities of semiconductor test equipment will be discussed. Then, the possibilities and limitations of statistics will be briefly touched upon, after which the focus will be on the tradeoff of measurement time vs. repeatability for high precision parametric device measurement for characterization of matching.

09:55 Break

10:00 **Advanced CMOS Technologies including 3D-Stacked 2D-FETs**

Hitoshi Wakabayashi

10:55 Break

11:00 **Current status of gallium oxide material and device technologies**

Masataka Higashiwaki

Gallium oxide (Ga2O3) has excellent material properties especially for power device applications that are represented by the extremely large bandgap of 4.5 eV and the high breakdown field over 7 MV/cm. It is also attractive from an industrial viewpoint since large-size, high-quality wafers can be manufactured from single-crystal bulks synthesized by melt-growth methods. These two features have drawn much attention to Ga2O3 as a new ultrawide bandgap semiconductor following SiC and GaN. In this talk, after a brief introduction of the material properties, state-of-the-art Ga2O3 material and device technologies will be discussed, including (1) bulk melt growth, (2) thin-film epitaxial growth, (3) FETs, and (4) Schottky barrier diodes.

11:55 Lunch

13:25 **Test Structures: The Intersection of Design and Test**

Brad Smith

This talk will cover the basics of test structure design and test, emphasizing how the two are inter-related. Often, there are no “right” answers in test structure design, only trade-offs. Methods for how to make those decisions will be covered, the most important of which is letting the desired output of a test structure define its design and testing.

14:20 Break

14:25 **Recent progress in CMOS image sensor technology and future prospect**

Masashi Bando

This presentation will begin with a brief introduction on the history of CMOS image sensor from device-structure perspective and expansion of application fields in the market. The presentation will include issues and imaging technologies associated with accelerated pixel scaling especially in mobile application, as well as global shutter and dynamic range expansion technology required for industry, security, and automotive application. Explanation will also be given for depth sensing, event-based vision sensing, and the concept for intelligent vision sensor as examples for “beyond 2D imaging” technology.

15:20 Break

15:25 **History of 2D/3D Multi-Level Flash Memory Design Technology**

Noboru Shibata

Currently, Multi-Level-Cell Flash Memory is used in a wide range of applications as a high-capacity, low-cost memory and has become indispensable in modern life. The first prototype of the Multi-Level-Cell NAND Flash Memory only stored 128Mbit with 2 bits per cell. Since commercialization in 2001, the Multi-Level-Cell NAND Flash memory has increased by over 10,000 times to 1.33Tbit memory density with 4 bits per cell (QLC). This tutorial will go over the challenges faced in shrinking down the size of memory cells and stacking multi-layers in 3D, how these obstacles were overcome to ensure reliability, and achieve higher capacity and faster memory. The transition and development of multi-level cell circuit design technology, cell characteristics and reliability will also be introduced.

16:20 Break

16:25 **Design and test for MEMS vibrational energy harvesters**

Hiroshi Toshiyoshi

A vibrational energy harvester is developed using MEMS (microelectromechanical systems) technology to generate more than 1 mW of power from ambient vibrations with sub-gravity levels of acceleration at frequencies around 100 Hz. Electrets or permanent charges are formed on the surface of micro electrodes that generate electrostatically induced current from mechanical vibrations. In this tutorial lecture, we look into an analytical model of power generation using an equivalent circuit model, and discuss a methodology for using electret potential to tune the electromechanical conversion efficiency to maximize output power. We also discuss an automated method to experimentally determine the electret potential.

17:20 Break

17:50 **Welcome Reception**

Technical Program

Day 1 - March 28

Session 1: Emerging Memory

Chair: Larg Weiland, PDF Solutions Inc., USA

09:00 1-1 **Discrete current limiting circuit for emerging memory programming**

Léo Laborie[1], Paola Trotti[1], Killian Veyret[1], Carlo Cagli[2]

[1] Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France
[2] STMicroelectronics, Grenoble, France

09:20 1-2 **Test Methodology Development for Investigating CeRAM at Elevated Temperatures**

A. A. Gruszecki[1], R. Prasad[1], S. V. Suryavanshi[3], G. Yeric[3], and C. D. Young[1,2]

[1] Electrical and Computer Engineering Department, The University of Texas at Dallas, Richardson, Texas, USA
[2] Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, Texas, USA
[3] Cerfe Labs, Austin, Texas, USA

09:40 1-3 **Real-time electrical measurements during laser attack on STT-MRAM**

Nicole Yazigy[1], Jeremy Postel-Pellerin[1], Vincenzo Della Marca[1], Ricardo. C. Sousa[2], Anne-Lise Ribotta[3], Gregory Di Pendina[2], Pierre Canet[1]

[1] Aix-Marseille Université, IM2NP, CNRS, UMR 7334, 5 rue Enrico Fermi, 13397 Marseille, France
[2] SPINTEC, University Grenoble Alpes, CNRS, CEA, SPINTEC, 38000 Grenoble, France.
[3] Mines Saint-Etienne, CEA, Leti, Centre CMP, 13541 Gardanne, France

10:00 1-4 **Automated RRAM measurements using a semi-automated probe station and ArC ONE interface**

Alin G. Panca[1], Alexantrou Serb[1], Spyros Stathopoulos[1], Suresh K. Garlapati[2], Themis Prodromakis[1]

[1] Institute for Integrated Micro and Nano Systems, University of Edinburgh, UK
[2] Materials Science And Metallurgical Engineering, Indian Institute of Technology Hyderabad, Telangana, India

10:20 1-5 **Analysis of Critical Schottky Distance Effect and Distributed Set Voltage in HfO2-based 1T-1R Device**

Shih-Kai Lin[1], Ting-Chang Chang[2,3], Wei-Chen Huang[2], Yung-Fang Tan[4], and Chen-Hsin Lien[1]

[1] Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan
[2] Department of Physics, National Sun Yat-Sen University, Kaohsiung, Taiwan
[3] College of Semiconductor and Advanced Technology Research, National Sun Yat-Sen University, Kaohsiung, Taiwan
[4] Department of Materials and Optoelectronic Science, National Sun Yat-Sen University, Kaohsiung, Taiwan

10:40

Session 2: Noise

Chair: Kiyoshi Takeuchi, The University of Tokyo, Japan

11:10 2-1 **Static and LFN/RTN Local and Global Variability Analysis Using an Addressable Array Test Structure**

Owen Gauthier[1,2], Sébastien Haendler[1], Ronan Beucher[1], Patrick Scheer[1], Quentin Rafhay[2], and Christoforos Theodorou[2]

[1] STMicroelectronics, Crolles, France
[2] Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, CNRS, Grenoble INP, IMEP-LAHC, Grenoble, France

11:30 2-2 **An Extended Method to Analyze Boron Diffusion Defects in 16 nm Node High-Voltage FinFETs**

Ting-Tzu Kuo[1], Ying-Chung Chen[1], Ting-Chang Chang[2], Fong-Min Ciou[3], Chien-Hung Yeh[4], Po-Hsun Chen[5], and Simon M. Sze[6]

[1] Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan
[2] Department of Physics, and also with College of Semiconductor and Advanced Technology Research, National Sun Yat-Sen University, Kaohsiung, Taiwan
[3] Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan
[4] Department of Photonics, National Sun Yat-sen University, Kaohsiung Taiwan
[5] Department of Applied Science, R.O.C. Naval Academy, Kaohsiung Taiwan
[6] Department of Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

11:50 2-3 **Vss-Bias-Based Measurement of Random Telegraph Noise in Hybrid SRAM PUF after Hot Carrier Injection Burn-In**

Kunyang Liu, Yichen Tang, Shufan Xu, and Hirofumi Shinohara

Graduate School of Information, Production and Systems, Waseda University, Kitakyushu, Japan

12:10 Lunch

13:40 **Exhibitor Presentation**

Advantest, Celadon Systems, FormFactor, Keysight Technologies, MPI Corporation

Session 3: Power Devices

Co-Chairs: Brad Smith, NXP Semiconductor, USA
Hi-Deok Lee, Chungnam National University, Korea

14:10 3-1 **Distributed field plate effects in split-gate trench MOSFETs**

R. Tambone[1,2], A. Ferrara[1], F. Magrini[3], A. Hoffmann[3], A. Wood[1], G. Noebauer[1], E. Gondro[3], and R.J.E. Hueting[2]

[1] Infineon Technologies Austria AG, Siemenstrasse 2, 9500 Villach, Austria
[2] University of Twente, Drienerlolaan 5, 7522 NB Enschede, The Netherlands
[3] Infineon Technologies AG, Am Campeon 1, 85579 Neubiberg, Germany

14:30 3-2 **Measuring of parasitic resistance of stacked chip of Si power device**

Tatsuya Ohguro[1], Hideharu Kojima[1], Takuma Hara[1], Tatsuya Nishiwaki[2], and Kenya Kobayashi[1]

[1] Toshiba Electronic Devices & Storage Corporation, 1-1, Iwauchi-Machi, Nomi, Ishikawa, Japan
[2] Toshiba Electronic Devices & Storage Corporation, 580-1, Horikawa-Cho, Saiwai-Ku, Kawasaki, Kanagawa, Japan

14:50 3-3 **New Extraction Method for Intrinsic Qrr of Power MOSFETs**

T. Hara, S. Nakajima, T. Ohguro and K. Miyashita

Advanced Semiconductor Device Development Center, Toshiba Electronic Devices & Storage Corporation

15:10 3-4 **On-Resistance Measurements of Low Voltage MOS-FET at wafer level**

Kohei Oasa[1], Tatsuya Nishiwaki[1], Tatsuya Ohguro[2], Yasunobu Saito[1], and Yusuke Kawaguchi[2]

[1] Toshiba Electronic Devices & Storage Corporation, 580-1, Horikawa-Cho, Saiwai-Ku, Kawasaki, Kanagawa, Japan
[2] Toshiba Electronic Devices & Storage Corporation, 1-1, Iwauchi-Machi, Nomi, Ishikawa, Japan

15:30 3-5 **Comparative study on characteristics of GaN-based MIS-HEMTs with Al2O3 and Si3N4 gate insulators under Hot Carrier Degradation**

Pei-Yu Wu[1], Xin-Ying Tsai[2], Ting-Chang Chang[3], Tsung-Ming Tsai[1] and Simon M. Sze[2]

[1] Department of Materials and Optoelectronic Science, National Sun Yat-Sen University, Kaohsiung, Taiwan
[2] Department of Electronics Engineering, National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[3] Department of Physics, and also with College of Semiconductor and Advanced Technology Research, National Sun Yat-Sen University, Kaohsiung, Taiwan

15:50 Break

Session 4: Measurement Technique

Co-Chairs: Satoshi Habu, Keysight Technology, Japan
Francesco Driussi, University of Udine, Italy

16:20 4-1 **The Pressing Probe Needle Technique for Characterizing Mechanical Stress Sensitivity of Semiconductor Devices**

Hans Tuinhout, Oliver Dieball

NXP Semiconductors, Eindhoven, The Netherlands

16:40 4-2 **A multi-contact six-terminal cross-bridge Kelvin resistor (CBKR) structure for evaluation of interface uniformity of the Ti-Al alloy/p-type 4H-SiC contact**

Yen-Ling Chen, Shih-Hao Lai, Jian-Hao Lin, and Bing-Yue Tsui

Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

17:00 **Test Structure for Evaluation of Pad Size for Wafer Probing**
4-3

Brad Smith[1], Donald Hall[1], and Garrett Tranquillo[2]

[1] NXP Semiconductors, Austin, TX, USA
[2] Celadon Systems, Inc., Burnsville, MN, USA

17:20 **Test Bench for Biopotential Instrumentation Amplifier using Single-Ended to Differential Amplifiers**
4-4

Surachoke Thanapitak, Pongsatorn Sedtheetorn, Pornchai Chanyagorn, Tatcha Chulajata, Somnida Bhatranand, and Phattanard Phattanasri

Department of Electrical Engineering, Faculty of Engineering, Mahidol University Nakhon Pathom, Thailand

17:40

Day 2 - March 29

Session 5: Matching & Variability

Chair: Hans Tuinhout, NXP Semiconductor, The Netherland

09:00 **Measurement of Temperature Effect on Comparator Offset Voltage Variation**
5-1

Yuma Iwata, Takehiro Kitamura, and Mahfuzul Islam

Department of Electrical Engineering, Graduate School of Engineering, Kyoto University, JAPAN

09:20 **Variability of MOSFET Series Resistance Extracted from Individual Devices: Is Direct Variability**
5-2 **Measurement Possible?**

Kiyoshi Takeuchi[1], Tomoko Mizutani[1], Takuya Saraya[1], Masaharu Kobayashi[2,1], and Toshiro Hiramoto[1,2]

[1] Institute of Industrial Science, The University of Tokyo, Tokyo, Japan
[2] Systems Design Lab(d.lab), School of Engineering, The University of Tokyo, Tokyo, Japan

09:40 **Variability Evaluation of MOS-gated PNPN Diode for Hardware Spiking Neural Network**
5-3

Toshihiro Takada, Takayuki Mori, and Jiro Ida

Division of Electrical Engineering, Kanazawa Institute of Technology, Ishikawa, Japan

10:00 **Effect of Quadruple Size Transistor on SRAM Physically Unclonable Function Stabilized by Hot**
5-4 **Carrier Injection**

Shufan Xu, Kunyang Liu, Yichen Tang, Ruilin Zhang, and Hirofumi Shinohara

Graduate School of Information, Production and Systems, Kitakyushu, Japan

10:20

Session 6: Yield and Device Optimization

Co-Chairs: Chadwin Young, University of Texas at Dallas, USA
Takayuki Mori, Kanazawa Institute of Technology, Japan

10:50 6-1 **Test Circuit Design for Accurately Characterizing Cells' Output Currents in a Read-Decoupled 8T SRAM Array for Computing-in-Memory Applications**

Hao-Chiao Hong[1,2], Long-Yi Lin[1,3], and Bo-Chang Chen[2]

[1] Institute of Electrical and Computer Engineering,
[2] Institute of Electrical and Control Engineering, National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[3] Novatek MicroElectronics Corp., Hsinchu, Taiwan

11:10 6-2 **Design and Analysis of Discrete FET Monitors in 7nm FinFET Product for Robust Technology Validation**

V.Vidya[1], N. Zamdmer[1], T. Mechler[1], K. Onishi[1], D. Chidambarao[1], B. W. Jeong[2], Y. G. Ko[2], C. H. Lee[1], J. Sim[1], M. Angyal[1], E. Crabbe[1]

[1] IBM Systems, IBM Corp, 2070 Route 52, B300-A, Hopewell Junction, NY 12533, USA
[2] Samsung Electronics Co. Ltd, San#16, Banweol-Dong, Hwasung-City, Gyeonggi-Do, 445-701, Republic of Korea

11:30 6-3 **An Electrical Inline-Testable Structure to Monitor Gate-Source/Drain Short Defect Caused by Imperfect Fin-Cut Patterning in FinFET Technology**

Hai Zhu[1], Katsunori Onishi[1], Stephen Wu[1], Adam Yang[1], Byoung-Wook Jeong[2], Seong-Joon Lim[2], Nan Jing[1], Choong-Ho Lee[1], David Conrady[1], and Dureseti Chidambarrao[1]

[1] IBM Systems, IBM Corp, 2070 Route 52, B300A, Hopewell Junction, NY 12533, USA

[2] Samsung Electronics Co. Ltd., San#16, Banweol-Dong, Hwasung-City, Gyeonggi-Do, 445-701, Republic of Korea

11:50 6-4 **Wafer Level Reliability Monitoring of NBTI Using Polysilicon Heater Structures for Production Measurements**

Yu-Hsing Cheng

Central Engineering, Onsemi 1900 South County Trail, East Greenwich, RI 02818, USA

12:10

Session 7: MEMS & Sensors

Co-Chairs: Yoshio Mita, The University of Tokyo, Japan
Jonathan Terry, The University of Edinburgh, UK

14:55 7-1 **Application of Greek cross structures for process development of electrochemical sensors**

M. Zhang, S. Zhang, C. Dunare, J.R.K. Marland, J.G. Terry and S. Smith

The School of Engineering, The University of Edinburgh

15:15 7-2 **Test Structures for Studying Coplanar Reverse- Electrowetting for Vibration Sensing and Energy Harvesting**

Anotidaishe Moyo[1], Muhammad Wakil Shahzad[1], Jonathan G. Terry[2], Stewart Smith[2], Yoshio Mita[3], Yifan Li[1]

[1] Department of Mechanical and Construction Engineering, Faculty of Engineering and Environment, Northumbria University, UK
[2] School of Engineering, Institute for Integrated Micro and Nano Systems, The University of Edinburgh, UK
[3] Department of Electrical Engineering and Information Systems, The University of Tokyo, Japan

15:35 7-3 **Damage Assessment Structure of Thermal-Annealing Post-Processing on CMOS LSIs**

Yuki Okamoto[1], Natsumi Makimoto[1], Kei Misumi[2], Takeshi Kobayashi[1], Yoshio Mita[2], Masaaki Ichiki[1]

[1] Sensing System Research Center, National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Japan
[2] School of Electrical Engineering, The University of Tokyo, Tokyo, Japan

15:55 7-4 **Improving Performance of FBARs by Advanced Low-Temperature High-Pressure Technology**

Yu-Fa Tu[1], Ting-Chang Chang[2,3], Kuan-Ju Zhou[2], Wei-Chun Hung[2], Ting-Tzu Kuo[4], and Chen-Hsin Lien[1]

[1] Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan
[2] Department of Physics, National Sun Yat-sen University, Kaohsiung, Taiwan
[3] Center of Crystal Research, National Sun Yat-sen University, Kaohsiung, Taiwan
[4] Department of Electrical Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan

16:15 7-5 **Solderable Multisided Metal Patterns Enables 3D Integrable Direct Laser Written Polymer MEMS**

Landon Ivy and Amit Lal

The SonicMEMS Laboratory, School of Electrical and Computer Engineering, Cornell University, USA

16:35

17:30 Bus for the hotel of the banquet leave Takeda-Hall

18:00 Banquest at Hotel Chinzanso Tokyo

Day 3 - March 30

Session 8: Modeling

Chair: Tatsuya Ohguro, Toshiba Electronic Devices & Storage Corporation, Japan

09:00 8-1 **Accurate Gate Charge Modeling of HV LDMOS Transistors for Power Circuit Applications**

Xiaorui Jie, Ronald van Langevelde, Kejun Xia[*], Lei Chao, Colin C. McAndrew, Qilin Zhang, Matthew Bacchi[†], and Wuxia Li

NXP Semiconductors, Front End Innovation
[*] TSMC, Special Technology Product Engineering
[†] NXP Semiconductors, Business Line Advanced Analog

09:20 8-2 **Introducing Transfer Learning Framework on Device Modeling by Machine Learning**

Kota Niiyama, Hiromitu Awano, and Takashi Sato

Graduate School of Informatics, Kyoto University

09:40 8-3 **Technology-Dependent Modeling of MOSFET Parasitic Capacitances for Circuit Simulation**

Dondee Navarro, Chika Tanaka, Kanna Adachi[1], Takeshi Naito, Kenshi Tada, and Akira Hokazono

Memory Division, KIOXIA Corporation, Yokohama, Japan
[1] Institute of Memory Technology Research and Development, KIOXIA Corporation, Yokohama, Japan

10:00

Session 9: Novel Materials

Chair: Stewart Smith, The University of Edinburgh, UK

10:30 9-1 **Bridging Large-Signal and Small-Signal Responses of Hafnium-Based Ferroelectric Tunnel Junctions**

M. Massarotto[1], M. Segatto[1], F. Driussi[1], A. Affanni[1], S. Lancaster[2], S. Slesazeck[2], T. Mikolajick[2,3], D. Esseni[1]

[1] DPIA, University of Udine, Udine, Italy
[2] NaMLab gGmbH, Dresden, Germany
[3] Chair of Nanoelectronics, IHM, TU–Dresden, Germany

10:50 9-2 **Demonstration of frequency doubler application using ZnO–DNTT anti-ambipolar switch device**

Yongsu Lee, Hyeon Jun Hwang, and Byoung Hun Lee

Center for Semiconductor Technology Convergence, Department of Electrical Engineering, Pohang University of Science and Technology, Pohang, Gyeongbuk 37673, Republic of Korea

11:10 9-3 **Identifying nano-Schottky diode currents in silicon diodes with 2D interfacial layers**

Tihomir Kneževic[1], Lis K. Nanver[2]

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11:30 Best Paper Presentation and Closing Remarks

Closing Session

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