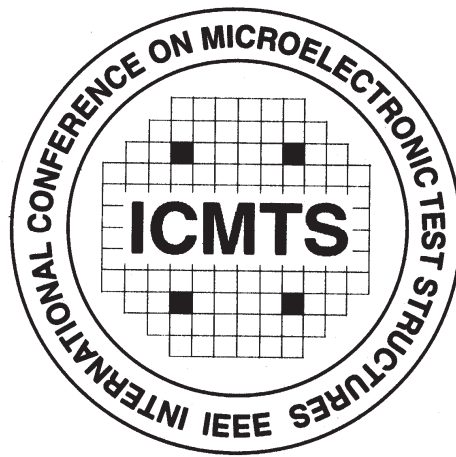


# **2019 IEEE 32<sup>nd</sup> International Conference on Microelectronic Test Structures**



**2019 IEEE 32<sup>nd</sup> ICMTS Conference Proceedings**

**March 18-21**

**Kitakyushu International Conference Center,  
Kitakyushu City, Fukuoka Prefecture, Japan**

Sponsored by:

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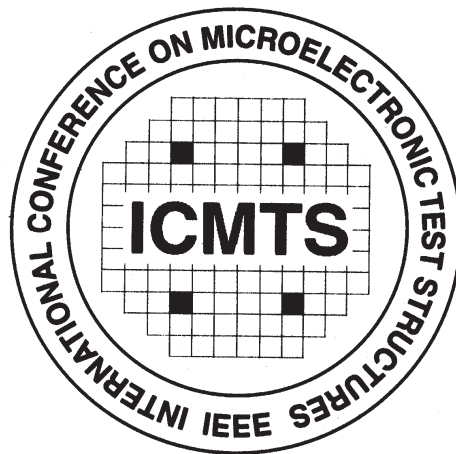
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## CHAIRMAN'S LETTER

Dear ICMTS Colleagues,

“When you can *measure* what you are speaking about and *express it in numbers* you know something about it” - this is the famous expression of Lord Kelvin [1] that the ICMTS folks know. Now in the 21<sup>st</sup> century, a century later from Lord Kelvin's days, “*express in number*” may include modeling using equation as well expressing in computer. Indeed, this is particularly true in microelectronic world because we, engineers, researchers and / or students in industries, academics and research institutes must cope with problems on issues of fabrication every day. Typical questions include “hey, what was wrong with this device?”, “was my fabrication correct?”, “what are and how to extract key parameters of this device and material?” To answer such questions, I would propose to continue the expression: “when you can *compare* which have difference in design and *extract the difference* in measurement you know something about it”. To help such comparative study, particular patterns are put somewhere on the device substrate wafer. We call them “Test Structures”.

The purpose of the ICMTS is to bring about engineers and researchers on all the domains concerning microelectronic devices to exchange recent findings on test structure, test methods using structures, and modeling. An emphasis is put on what we call “real silicon” – measurement on existing structures. Therefore we the ICMTS folks must be proud of having “measured” something “real”, and participants of the ICMTS can testify some “numbers” that contain the truth of the nature. Thirty-eight papers including three invited talks will be presented in ten Sessions: 1: Photonic Test Structures, 2: Yield & Reliability, 3: Novel Process Characterization, 4: Resistive Materials, 5: Power Device, 6: Matching & Variability, 7: Measurement Technique, 8: Noise, 9: Packaging, and 10: TFTs.

This year in 2019, the ICMTS is celebrating its 32<sup>nd</sup> edition. Clearly, “32<sup>nd</sup>” is the magic word for us electronic engineers, because 32 is 0x20 in hexadecimal. Starting from 1988 as a successor of workshops held in west-coast cities in the US, the ICMTS is now entering its 6<sup>th</sup>-bit era. The conference turns around the United States, Asia, and Europe. The 2019 version is held in Kita-Kyushu City, Fukuoka Prefecture. The city is known to be a city of the industrial Revolution in Japan. In 1901, a modern iron smelting furnace was constructed in Yawata area, by taking advantage of coal field in north of Kyushu Island. The City of Kitakyushu and Kitakyushu Convention Bureau financially supported the 32<sup>nd</sup> ICMTS; the participants of the conference will certainly enjoy the best hospitality of the region of north Kyushu Island. Indeed, networking and discussing with colleagues while seeing the city and eating altogether is the best smelting furnace to get inspired for future.

Now the bell is ringing: Welcome to the test structure world!

Dr. Yoshio Mita, the University of Tokyo  
General Chairman

[1] Lord Kelvin, “Popular Lectures and Addresses: Constitution of matter”, London: MacMillan, p.80 (1891).

## **Invited Talk 1:**

**2019 Mar 19, 9:10 – 9: 40**

Chair: Akio Higo, *The University of Tokyo, Japan*

**9:00 Electronic photonic IC technology - challenges of on-wafer characterization and test**

**Invited1** [Invited] .....2

Lars Zimmermann, *IHP – Leibniz-Insitut für innovative Mikroelektronik, Germany*

## **Session 1: Photonic Test Structures**

**2019 Mar 19, 9:40 – 11: 00**

Co-Chairs: Alexey Kovalgin, *University of Twente, The Netherland*

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<sup>1</sup>*VLSI Design and Education Center, The University of Tokyo, Japan*

<sup>2</sup>*Graduate School of Engineering, The University of Tokyo, Japan*

<sup>3</sup>*Yokohama National University, Japan*

**10:00 PbS Quantum Dot / ZnO Nanowires Hybrid Test Structures for Infrared**

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<sup>1</sup>*Research Center for Advanced Science and Technology, The University of Tokyo, Japan*

<sup>2</sup>*VLSI Design and Education Center, The University of Tokyo, Japan*

<sup>3</sup>*Graduate School of Engineering, The University of Tokyo, Japan*

<sup>4</sup>*Graduate School of Art and Science, the University of Tokyo, Japan*

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<sup>1</sup>*MESA+ Institute for Nanotechnology, University of Twente, The Netherlands*

<sup>2</sup>*Department of Materials and Production, Aalborg University, Denmark*

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Ye Wang, Hanyi Ding, Barry Blakely, Aidong Yan

*Department of Silicon Photonics Test Development, GLOBALFOUNDRIES*

## SESSION 2: Yield & Reliability

2019 Mar 19, 11:20 – 12:20

Co-Chairs: WEILAND, Larg, *PDF Solutions, USA*

MORI, Shigetaka, *SONY Corporation, Japan*

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	<sup>1</sup> <i>Department of Electrical Engineering, Faculty of Science and Technology, Tokyo University of Science, Japan</i>	
	<sup>2</sup> <i>Department of Electronics, Graduate School of Science and Technology, Kyoto Institute of Technology, Japan</i>	
<b>11:40</b>	<b>Extremely Low Voltage Operatable On-Chip-Monitor-Test Circuit for Plasma Induced</b>	
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	<sup>1</sup> <i>STMicroelectronics, France</i>	
	<sup>2</sup> <i>IMS, Université Bordeaux I, France</i>	

### Invited Talk 2:

2019 Mar 19, 13:35 – 14:05

Chair: Tsuyoshi Sekitani, *Osaka University, Japan*

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Yasuo Koide

*Research Network and Facility Services Division, National Institute for Materials Science (NIMS), Japan*

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	<i>MESA+ Institute for Nanotechnology, University of Twente, The Netherlands</i>	

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	<sup>1</sup> <i>Graduate School of Engineering, The University of Tokyo, Japan</i>	
	<sup>2</sup> <i>VLSI Design and Education Center, The University of Tokyo, Japan</i>	
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	<sup>1</sup> <i>School of Engineering, Institute for Integrated Micro and Nano Systems, The University of Edinburgh, UK</i>	
	<sup>2</sup> <i>School of Engineering, Institute for Bioengineering, The University of Edinburgh, UK</i>	
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	<i>NXP Semiconductors, The Netherlands</i>	

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Co-Chairs: SMITH, Stewart, *U. Edinburgh, UK*

HESS, Christopher, *PDF Solutions, USA*

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<sup>1</sup>*Graduate School of Engineering, Tohoku University, Japan*

<sup>2</sup>*School of Engineering, Tohoku University, Japan*

<sup>3</sup>*New Industry Creation Hatchery Center, Tohoku University, Japan*

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*Univ. Grenoble Alpes, France*

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Khim Hong Ng, Dennis Ciplickas, Rakesh Vallishayee, Christoph Dolainsky, Larg H. Weiland

*PDF Solutions Inc., USA*

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**Invited Talk 3:**

**2019 Mar 20, 09:00 – 09:30**

Chair: Yoshio Mita, *The University of Tokyo, Japan*

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**2019 Mar 20 9:30 – 10:30**

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### **SESSION 6: Matching & Variability**

**2019 Mar 20 10:50 – 12:10**

Co-Chairs: Hans P. Tuinhout, *NXP Semiconductor, The Netherlands*  
FUKUZAKI, Yuzo, *Sony Corporation*

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### **SESSION 7: Measurement Technique**

**2019 Mar 20 13:30 – 15:10**

Co-Chairs: DRIUSSI, Francesco, *University of Udine – DPIA, Italy*  
VERZI, Bill, *Keysight, USA*



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## **SESSION 8: Noise**

**2019 Mar 20 15:30 – 16:30**

Co-Chairs:      Kiyoshi Takeuchi, *The University of Tokyo, Japan*  
                      Hirofumi Shinohara, *Waseda University, Japan*

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	<sup>1</sup> <i>Graduate School of Engineering, Kyoto University, Japan</i>	
	<sup>2</sup> <i>Graduate School of Informatics, Kyoto University, Japan</i>	
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	<sup>1</sup> <i>Saginomiya Seisakusho, Inc., Japan</i>	
	<sup>2</sup> <i>Institute of Industrial Science, The university of Tokyo, Japan</i>	
	<sup>3</sup> <i>Shizuoka University, Japan</i>	

### **SESSION 9: Packaging**

**2019 Mar 21 9:20 – 10:20**

Co-Chairs: HABU, Satoshi, *Keysight, Japan*

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	<sup>1</sup> <i>STMicroelectronics Rousset, France</i> , <sup>2</sup> <i>LTM CNRS, France</i>	
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	<sup>1</sup> <i>School of Electrical Engineering, The University of Tokyo</i>	
	<sup>2</sup> <i>VLSI Design &amp; Education Center (VDEC), The University of Tokyo</i>	
	<sup>3</sup> <i>NEXTY Electronics Corporation</i>	

## **SESSION 10: TFTs**

**2019 Mar 21 10:40 – 11:20**

Co-Chairs: CAGLI, Carlo, *CEA/LETI, France*

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*Department of Materials Science and Engineering, University of Texas at Dallas, USA*

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<sup>1</sup>*Graduate School of Informatics, Kyoto University, Japan*

<sup>2</sup>*Graduate School of Science and Technology, Nara Institute of Science and Technology, Japan*

<sup>3</sup>*National Institute of Advanced Industrial Science and Technology (AIST), Japan*

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