ADVANCE PROGRAM

ICMTS 2018

31st Annual IEEE International Conference on Microelectronic Test Structures

Courtyard by Marriott
Austin Downtown/
Convention Center
Austin, Texas, USA

Tutorials – March 19, 2018
Conference – March 20 - 22, 2018

SPONSORED BY:

THE INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS
ELECTRON DEVICES SOCIETY

Conference Website: http://icmts.if.t.u-tokyo.ac.jp/

2018 ICMTS SCHEDULE AT A GLANCE	
Monday March 19 **Tutorials (Separate Registration Required)** Registration opens at 8:30 AM **All Tutorials: Guadalupe Room**	
08:50	Tutorial Introduction
09:00	Hans Tuinhout (NXP)
10:00	Coffee Break
10:20	Emanuel Tutuc (UT Austin)
11:20	James Coleman (UT Dallas)
12:20	Lunch
14:00	Fred Mancoff (Everspin)
15:00	Coffee Break
15:20	Jason Reifsnider (Samsung)
16:20	Andrew Kerber (GLOBALFOUNDRIES)
17:20	Close
17:30	**Welcome Reception**

Tuesday March 20 Registration opens at 8:00 AM - ***Foyer A (2nd Floor)*** **All Sessions: Rio Grande Ballroom** **Exhibits: Brazos I-II-II**	
09:00	**Welcome and Announcements**
09:10	**Session 1**: Process Characterization
10:30	Coffee Break with Exhibitors
11:00	**Session 2**: Modeling and Extraction
12:20	Lunch
13:40	**Keynote**: Jon Cheek (NXP)
14:10	**Session 3**: Reliability
14:50	**Exhibitor Presentations**
15:20	Coffee Break with Exhibitors
15:40	**Session 4**: Materials Characterization
17:20	Close

Wednesday March 21 Registration opens at 8:00 AM - ***Foyer A (2nd Floor)*** **All Sessions: Rio Grande Ballroom** **Exhibits: Brazos I-II-II**	
08:15	**Writing Good Papers/Getting Published**
09:00	**Session 5:** Mismatch and Variability
10:20	Coffee Break with Exhibitors
10:50	**Session 6:** On-Chip Characterization
12:10	Lunch
13:30	**Keynote**: Greg Yeric (ARM)
14:00	**Session 7**: Test Parallelism
14:40	**ICMTS 2019 Presentation**
14:50	Coffee Break with Exhibitors
15:20	**Session 8:** Device Characterization
17:00	**Close**
18:30	**Banquet "18th Over Austin"**

Thursday March 22 Registration opens at 8:30 AM - ***Foyer A (2nd Floor)*** **All Sessions: Rio Grande Ballroom**	
08:15	**Making Good Presentations**
09:00	**Session 9**: MEMS
10:20	Coffee Break
10:50	**Session 10**: Noise and RF
12:10	**Best Paper Announcement Conference Close**

Welcome to ICMTS 2018

The 31st IEEE International Conference on Microelectronic Test Structures (ICMTS) will be held in Austin, Texas, USA from Monday March 19 through Thursday March 22, 2018, at the Courtyard by Marriott Austin Downtown/Convention Center.

ICMTS is the only conference dedicated to designers and users of test structures, and encompasses developments in testing, measurement, characterization, modeling, reliability, and circuit applications as well as in test structures themselves. ICMTS 2018 is a single-track conference, and includes 10 paper presentation sessions. There will also be two keynote talks, by Greg Yeric of ARM and by Jon Cheek of NXP.

The conference proper, which runs from Tuesday through Thursday morning, will be preceded on the Monday by a series of six educational tutorials from noted experts. Ten equipment companies will be exhibiting their latest products, and these will be in the area where coffee breaks and lunch will be provided, so you can easily visit the exhibition booths, mingle with, and learn from the exhibitors. There will also be a short presentation from each exhibitor on Tuesday afternoon.

As a "bonus," aimed to help younger attendees, prior to the sessions on Wednesday and Thursday there will be talks on how to write good papers and get published, and how to prepare and make good presentations.

There is a reception on the Monday evening, where you can network, meet old friends, and make new contacts. The conference banquet is on the Wednesday evening, at "18th Over Austin," which has a spectacular view of downtown Austin from the top floor of the Hilton Garden Inn, which is a 10-minute walk from the conference hotel.

Austin is a vibrant and fast-growing city, justifiably known as the "Live Music Capital of the World." 6th street, famous for its bars and live music, is just around the corner from the conference hotel, and Lady Bird Lake, which has magnificent walking/running paths through the parks on its shores, is a few minutes away. The eclectic food trucks, restaurants, and bars of Rainey Street are also within easy walking distance, as is the famous bat bridge. The internationally renowned "South by Southwest" is being held in Austin the week before the conference.

We look forward to welcoming you to ICMTS 2018!

Colin McAndrew
NXP Semiconductors
General Chair

Brad Smith
NXP Semiconductors
Technical Program Chair

ICMTS 2018 REGISTRATION

An on-line registration link is available at the ICMTS 2018 website:
http://icmts.if.t.u-tokyo.ac.jp/

Registration Fees (US$):

	Advance*	Regular
Technical Sessions		
IEEE Member	**625**	**675**
IEEE Life Member	**300**	**325**
Non-Member	**675**	**725**
Student	**300**	**325**
Tutorials		
Non-Student	**325**	
Student	**140**	
Optional Items		
Extra Banquet Ticket	**90**	
Extra Proceedings	**50**	
Tutorial Notes	**150**	

*** before February 16, 2018**

Notes:
Technical session registration includes:
- one banquet ticket
- one bound and one electronic (USB) copy of the proceedings
- lunch Tuesday and Wednesday

Tutorial registration includes:
- printed copy of the slides
- lunch

Refund/Cancellation Policy:
All requests for refund/cancellation must be received in writing by February 26, 2018. Any requests thereafter will not be entitled to a refund. Cancellations will incur a $100 USD administration fee. Please submit cancellation requests via email to cs@cshawevents.com

HOTEL RESERVATIONS

A block of rooms has been reserved at special discounted rates for ICMTS conference participants at our host hotel, the Courtyard by Marriott Austin Downtown/Convention Center. A link for hotel registration is available on the ICMTS 2018 web-site:
http://icmts.if.t.u-tokyo.ac.jp/hotel_reg

While other hotels are available nearby, we would ask attendees to please support the conference and fully enjoy all ICMTS activities by staying at the official host hotel. We rely on attendees staying at the conference hotel. Room reservations should be made as soon as possible before February 19, as there are a limited number of rooms available at the group rate.

TRAVEL ARRANGEMENTS

Air Travel

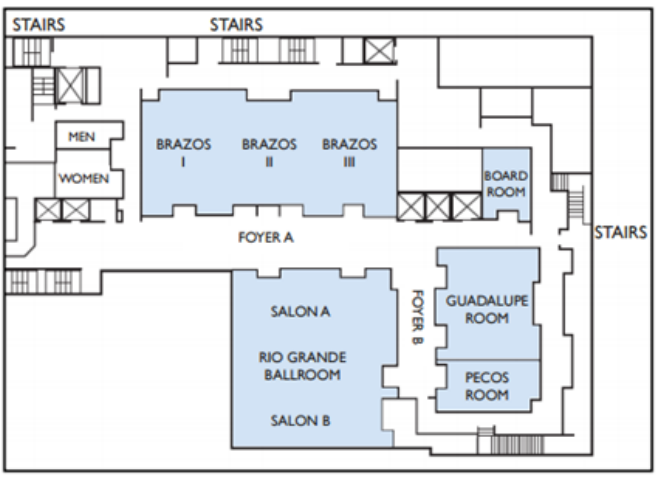
- You are responsible for booking your own air travel.
- Austin is served by the Austin-Bergstrom International airport (http://www.austintexas.gov/airport). It is served by the major airlines in the US. For international travelers there is a direct flight from London Heathrow, otherwise you will have no problem connecting via one on the major US airports.

Ground Transportation

- Car rental is available directly at the terminal, a short walk from the arrival/departure area. Getting downtown is simple, but expect traffic delays during peak travel times. Parking at the hotel is $30 per day.
- Taxi fare is about $30 one way, including tip.
- Super Shuttle is about $13 one way, a reservation is required.
- The “Airport Flyer” bus (#100) runs roughly every ½ hour, has only a few stops on the route to downtown, has a stop right on the corner where the hotel is located, and costs $1.50.

MEETING ROOM MAP

Second Floor: All conference meeting sessions will be held on the 2nd Floor.



2nd Level – Courtyard Side

EQUIPMENT EXHIBITION

Brazos I-II-III

Equipment Exhibition Chair:

Scott McDade (Keysight)

To expose ICMTS attendees to their latest and greatest products, the following companies will be exhibiting at ICMTS 2018:

- Celadon Systems
- Everbeing International
- Keithley/Tektronix
- Keysight Technologies
- MPI Corporation
- Platform Design Automation
- ProPlus Design Solutions
- SEMIPROBE

The equipment exhibits will be set up in the Brazos I-II-II rooms, and will be open on Tuesday and Wednesday. To facilitate attendees to visit and interact with the exhibitors, coffee breaks will be held in the exhibit hall, and tables at which to eat lunch are provided in the exhibit hall.

The exhibitors will also be giving short presentations on their latest offerings, from 14:50 to 15:20 on Tuesday afternoon, in the Rio Grande Ballroom.

The exhibitors are extremely important to the financial viability of the conference, so please plan to visit all the equipment exhibitors.

ADDITIONAL INFORMATION

CONFERENCE ROOMS: Meeting rooms for the conference are located on the 2nd floor of the Courtyard by Marriott Austin Downtown/Convention Center. A map of the meeting space is provided on page 5 of this booklet.

CONFERENCE BANQUET: Wednesday, March 21
The ICMTS 2018 Banquet and Casino Night will take place at "18th Over Austin" at the top of the Hilton Garden Inn Austin Downtown, which is about a 10-minute walk from the conference hotel see map at the end of the Wednesday session details). The venue offers a spectacular view of downtown Austin at night. One banquet ticket is included with every technical session registration.

ATTENDEE LOUNGE: The Pecos Room will be available throughout the duration of the conference for attendees to check e-mail, make calls, have detailed discussions, etc.

ADMISSION: All interested persons are welcome to register and attend ICMTS; you do not have to be an IEEE member. Admission to sessions requires an ICMTS badge. Please wear your badge at all times.

WELCOME RECEPTION: On Monday evening, after the tutorial sessions have finished, there will be a welcome reception. Drinks and Hors d'Oeuvres will be provided.

TUTORIALS: Tutorial talks given by noted experts from industry and academia will be held on Monday March 19. A separate registration is required to attend the tutorials.

MEMBERS OF THE PRESS: You are welcome to attend ICMTS. Admission is free. Just present your business card at the registration desk.

RECRUITING: Intensive recruiting undermines the purposes for which ICMTS was established, and is contrary to IEEE policy.

BEST PAPER AWARD: ICMTS 2018 will have a best paper award. The winner will be selected by members of the technical program committee, announced at the close of the conference on Thursday, and officially presented during the banquet of ICMTS 2019.

WEATHER: During March, the daily maximum temperature is usually between 69 and 72 ºF (21 to 24 C) and the minimum varies between about 48 and 55 º F (9 to 13 C). There is an approximately 20% chance of measurable rain on any given day in March.

EXCURSION: If there is sufficient interest, we will organize an excursion for the Thursday afternoon after the close of the conference. The excursion is optional, and may entail an additional cost.

ICMTS CONFERENCE MANAGER

Catherine Shaw, CMP
Phone: +1 732-501-3334
cs@cshawevents.com

ICMTS TUTORIAL PROGRAM

MONDAY MARCH 19

Guadalupe Room

Tutorials Chair: Chadwin Young (UT Dallas)

8:30 **Registration**

8:50 **Tutorial Introduction**

9:00 **An Introduction to Microelectronic Test Structures**
Hans Tuinhout (NXP)

This tutorial will discuss elementary requirements, boundary conditions, and examples of test structures for characterizing and modeling of semiconductor devices and technologies. They do not teach you about test structures at university, so this is a “Test Structures 101” class to fill that gap.

Dr. Tuinhout received EE M.Sc and Ph.D degrees from Delft University of Technology in the Netherlands in 1980 and 2005 respectively. Since 1980 he worked for Philips Research, now NXP Semiconductors, on electrical process and device characterization for CMOS and BiCMOS integrated circuit technologies. Over the past 25 years his work focused on characterizing and understanding parametric variability effects in contemporary mixed-signal IC technologies.

10:00 **BREAK**

10:20 **Interlayer Tunneling Field Effect Transistors**
Emanuel Tutuc (UT Austin)

Electron tunneling is receiving increased emphasis as the physical mechanism of operation in emerging devices that seek to mitigate power dissipation issues in aggressively scaled CMOS technology. Interlayer tunneling field-effect transistors (ITFETs) are a class of tunneling devices consisting of two semiconducting layers separated by a tunnel barrier. Owing to momentum conserving tunneling between the two layers, the inter-layer tunneling current-voltage characteristics possess gate-tunable negative differential resistance, a feature that can be used to implement Boolean logic functions. We describe here the fabrication, characterization, and benchmarking of ITFETs using van der Waals heterostructures of 2D materials.

Prof. Tutuc received the B.S. and M.S. degrees from Ecole Normale Superieure, The University of Paris, France in 1997 and 1998, and the Ph.D. degrees in 2004 from Princeton University, in Physics. Between 2004 and 2006, he was a post-doctoral research at I.B.M. T.J. Watson Research Center, Yorktown Heights, NY. He is currently an Associate Professor of Electrical and Computer Engineering at the University of Texas at Austin, Austin, TX. His research interests are the growth

and electronic properties of semiconductors, and their application to novel electronic devices. Prof. Tutuc is a Fellow of the American Physical Society, a recipient of a 2009 NSF CAREER Award, a 2008 DARPA Young Faculty Award, and the Charlotte Elizabeth Procter Fellowship at Princeton University.

11:20 **Silicon Photonics**
James J. Coleman (UT Dallas)

The dramatically expanding market for ever-faster data links ranging from board-to-board, chip-to-chip and eventually intra-chip has driven interest in merging the very different technologies of fiber optic links and silicon-based integrated circuits to form silicon photonics. In this tutorial, we outline the differences and similarities of IC and photonics technologies, and describe the approaches to enable future photonics-based ICs.

Prof. Coleman received his degrees in electrical engineering from the University of Illinois, Urbana. After working at Bell Laboratories and Rockwell International, he was professor of Electrical and Computer Engineering at the University of Illinois for 31 years and held the Intel Alumni Endowed Chair. In 2013, he joined the University of Texas at Dallas. Professor Coleman has published more than 600 journal publications and conference presentations on compound semiconductor laser materials and devices. He has been the recipient of the John Tyndall Award and the IEEE David Sarnoff Award, and is a member of the US National Academy of Engineering. He is a Fellow of the IEEE, OSA, SPIE, APS, AAAS, and the National Academy of Inventors.

12:20 **LUNCH**

14:00 **Characterization of Spin-Transfer Torque Magnetoresistive Random Access Memory Performance from Single Magnetic Tunnel Junction Bits up to Large Scale Arrays**
Fred Mancoff (Everspin Technologies)

Magnetoresistive Random Access Memory (MRAM) offers a nonvolatile memory solution capable of delivering high-speed and endurance with promise in areas including data storage, industrial controls, networking products, and other applications. In MRAM, the resistance state of a magnetic tunnel junction (MTJ) bit is sensed to perform a read operation while a write operation is performed by reversing the direction of magnetization of the storage layer in the MTJ. In spin-transfer torque (STT-MRAM), this write reversal is driven by an electrical current flowing through the MTJ. Here we give an overview of the development of STT-MRAM at Everspin, focusing on the progression of the characterization of MTJ performance from single bit measurements to small scale arrays included in scribe grid test structures and finally to the resulting performance of large scale product arrays. Critical aspects of MTJ array properties for successful

STT-MRAM operation are described, including write and read performance, data retention for nonvolatility, and endurance. The test structures and characterization described have enabled MRAM array development from sizes of 1 Mb up to 1 Gb.

Dr. Mancoff is a Senior Member of Technical Staff at Everspin Technologies, Inc. in Chandler, Arizona in the Technology Research and Development group. He currently works on magnetic tunnel junction device measurement and characterization for spin-transfer torque MRAM (STT-MRAM), including the development of a 1 Gb STT-MRAM product as well as future generations of MRAM technology. He received his Ph.D. in Materials Science and Engineering from Stanford University in 2000 and was a postdoctoral research associate at the National Institute of Standards and Technology (NIST) in Boulder, Colorado from 2000 to 2002. In 2002, he joined Motorola as a Senior Scientist working on STT-MRAM and spin-transfer torque oscillators and then transitioned with the Motorola MRAM program to Freescale Semiconductor in 2004 and then to the spin-off of Everspin Technologies in 2008

15:00 **BREAK**

15:20 **Foundry Characterization for Product Improvement and Yield Enhancement**
Jason Reifsnider (Samsung)

A mass production Foundry environment presents a unique perspective on test structures versus the design / development environment in which test structures flourish. This tutorial will specifically discuss the use of test structures from the Production point of view. As products are transitioned from Development to New Product Introduction (NPI), the use of test structures changes, and which structures are deemed valuable also changes. Finally, as products go from NPI to full, high volume production, test structure usage changes again. Finally, a summary will be presented of the limiting factors which drive manufacturing away from the rich test structure diversity of development.

Dr. Reifsnider is a Group Leader for Process Integration Engineering for Samsung at the Samsung Austin Semiconductor site in Austin, TX. He earned his BS EE, MS EE, and Ph.D. degrees from The University of Texas at Austin. After joining Samsung Austin in 1999, he worked on parametric test for the characterization of DRAM products for several years. This included work to both write code and analyze test data from a variety of test structures. Since moving on to Process Integration Engineering in 2002, he has worked on DRAM, NAND FLASH, and now LSI Foundry products. Since becoming the manager for PIE in 2008, he was the technical leader for transferring the 20 nm technology node and the 14nm technology node from the development fab in Seoul to the Samsung Austin production site. He now leads two integration departments, responsible for 28 nm – 65 nm production nodes at Samsung Austin, including new product introduction, production ramp, and yield improvement for dozens of products.

16:20 **Test Structure Innovation for Discrete Device and Digital Circuit Degradation in Advanced CMOS Technology Nodes**
Andreas Kerber (GLOBALFOUNDRIES)

Aggressively scaled transistor technologies with metal gate/high-k stacks bring new challenges for characterization and modeling of the standard FEOL reliability mechanism (BTI, HCI and TDDB). To address the additional challenges new test structures have been introduced in recent years to investigate the stochastic nature of BTI in SRAM devices, capture the process variability component for BTI, address self-heating concerns in bulk/SOI-FinFETs, PDSOI and FDSOI designs and link device to digital circuit degradation in RO circuits. In this tutorial, we will discuss test structures for the standard FEOL reliability characterization and recently introduced novel test structures designs together with improvements in the characterization methodologies.

Dr. Kerber received his Diploma in physics from the University of Innsbruck, Austria, in 2001, and a PhD in electrical engineering from the TU-Darmstadt, Germany, with honors in 2014. He has held positions at Bell Laboratories, Infineon Technologies, SEMATECH, IMEC, and AMD. He is now a Principal Member of Technical Staff at GLOBALFOUNDRIES in Malta, NY, working on front-end-of-line reliability focusing on metal gate/high-k CMOS process technology, advanced transistor architecture and device-to-circuit reliability correlation. Dr. Kerber has contributed to more than 110 journal and conference publications. In addition, he has presented tutorials on metal gate / high-k reliability characterization at the IIRW and IRPS. Dr. Kerber has served as a technical program committee member for the SISC, IRPS, IEDM, Infos, ESSDERC, is a Senior Member of the IEEE and a Distinguished Lecturer (DL) for the IEEE Electron Devices Society.

17:20 **Tutorial Close**

17:30 **Welcome Reception**

ICMTS CONFERENCE PROGRAM

TUESDAY MARCH 20

WELCOME AND ANNOUNCEMENTS

9:00 - 9:10 – Rio Grande Ballroom

Session 1: Process Characterization

9:10 – 10:30 – Rio Grande Ballroom

Chairs:
Tsuyoshi Sekitani (U. Osaka)
Larg Weiland (PDF Solutions)

9:10
1.1 - Test Structures for Debugging Variation of Critical Devices Caused by Layout-Dependent Effects in FinFETs
Qi Lin, Hans Pan, and Jonathan Chang

We developed a set of test structures for monitoring and debugging the variation of critical devices caused by layout-dependent effects. These test structures were verified in 16 nm FinFET technology. We also present two case studies of debugging FinFET device variation by using these test structures.

9:30
1.2 - Passive Permutation Multiplexer to Detect Hard and Soft Open Fails on Short Flow Characterization Vehicle Test Chips
Christopher Hess and Shia Yu

Short flow characterization vehicle test chips are a major contributor to fast learning cycles especially for BEOL process steps. While hard open fails can be easily detected even in large via chains, it is very difficult to detect soft open fails like a 100 times larger via resistance of just one via within a large chain of vias. A Passive Permutation Multiplexer (PPM) is presented to optimize the signal to noise ratio for detecting soft open fails. The PPM implements a balanced routing access to a local population of resistive Devices Under Test (DUT) such as via or contact chains. Thus, soft open fails are easily recognizable as outliers of all measured resistance values within such a local population of DUTs. Compared to traditional passive multiplexers, the PPM contains up to twice as many DUTs. Furthermore, significantly larger Design of Experiments (DOEs) can be implemented, since the PPM can hold more than just one DOE level within the same array.

9:50

1.3 - Novel Test Structures for Extracting Interface State Density of Advanced CMOSFETs Using Optical Charge Pumping

Hyeong-Sub Song, Dong-Jun Oh, So-Yeong Kim, Sung-Kyu Kwon, Sungju Choi, Dae Hwan Kim, Dong-Hwan Lim, Chang-Hwan Choi, Dong Myong Kim, and Hi-Deok Lee

In this paper, we proposed novel test structures to evaluate the distribution of interface state density of MOSFETs by using optical charge pumping method. Unlike other measurement methods to extract interface state density (Dit), which have a limited range of measurable energy states and influenced by gate area and gate leakage, Dit can be extracted without these problems by using the proposed test structures. Test structures were fabricated using a 0.18 um CMOS process or FD-SOI technology with high-k dielectric, respectively. Optical charge pumping was performed in proposed test structures and Dit is extracted from 109 $cm^{-2}eV^{-1}$ to 1013 $cm^{-2}eV^{-1}$.

10:10

1.4 - Test Structure to Evaluate the Impact of Parasitic Edge FET on Circuits Operating in Weak Inversion

Dale McQuirk, Chris Baker, and Brad Smith

Parasitic edge FET effects on DGO NMOS devices operating in the sub-threshold region were studied using several test structures that emulate typical functions within analog circuits. An experiment was planned to implement a processing method experiment for reducing parasitic effects within the test structures. Results from one method demonstrated a significant reduction of parasitic edge effect.

Coffee Break with Exhibitors

10:30 – 11:00 – Brazos I-II-III

Session 2: Modeling and Extraction

11:00 – 12:20 – Rio Grande Ballroom

Chairs:
Yoshio Mita (U. Tokyo)
Colin McAndrew (NXP)

11:00

2.1 - Comprehensive Investigation on Parameter Extraction Methodology for Short Channel amorphous InGaZnO Thin-Film Transistors

Chika Tanaka and Keiji Ikeda

We proposed the comprehensive parameter extraction method for short channel amorphous InGaZnO (α-InGaZnO) thin-film transistors (TFTs) on the basis of measurement data and TCAD simulations. Single parameter set were successfully extracted for channel length down to 500 nm by using RPI a-Si TFT model with channel length modulation modeling. It makes possible to

more accurate and scalable circuit performance characterization, since the extracted parameters correspond to the physical behavior of a-InGaZnO TFTs.

11:20
2.2 - Modeling Split-Gate Flash Memory Cell for Advanced Neuromorphic Computing
Mandana Tadayoni, Santosh Hariharan, Steven Lemke, Thibaut Pate-Cazal, Bernard Bertello, Vipin Tiwari, and Nhan Do

Split-gate flash memory technology had recently been used in neuromorphic computation where a non-volatile memory array is designed in such a way that enables high-precision tuning of individual memory elements. This work proposes for the first time a SPICE model of the 2-transistor, select gate and floating gate, of the split-gate flash memory cell, implemented in a 180 nm CMOS technology, that allows the users to set the individual memory cell to any precise analog state.

11:40
2.3 - Validation of the BSIM4 Irregular LOD SPICE Model by Characterization of Various Irregular LOD Test Structures
Bob Peddenpohl, Max Otrokov, and Jeremy Wells

Stress from FET Isolation regions affects the electrical behavior of transistors in modern technologies. Characterization and modeling of stress effects have primarily been done for transistor layouts that have rectangular (regular) shaped source and drains. However, circuits may include transistor layouts that have non-rectangular (irregular) shaped source and drains. This paper presents test structures to evaluate the effects caused by isolation stress on irregular source/drain transistor layouts, and shows the standard way of calculating the effective distances for modeling stress effects is also reasonable for irregular source/drain transistor layouts.

12:00
2.4 - Efficient Parameter-Extraction of SPICE Compact Model Through Automatic Differentiation
Michihiro Shintani, Masayuki Hiromoto, and Takashi Sato

A novel method for the extraction of MOSFET compact model parameters is proposed. The proposed method exploits automatic differentiation technique, utilized in back-propagation to learn the parameters of artificial neural network. In the automatic differentiation, gradient of all parameters of the MOSFET model is calculated with the reduced computational cost. Based on the calculated gradient, the model parameters are efficiently optimized. Through experiments using a SPICE model for SiC power MOSFETs, the proposed method achieved a 12.3x speedup compared to the numerical-differentiation method. In addition, it is demonstrated that the parameter extraction is accurately and effectively conducted in combination with a conventional metaheuristic algorithm based parameter extraction and proposed method.

Lunch

12:20 – 13:40 – Brazos I-II-III

Keynote Talk by Jon Cheek (NXP)

13:40 – 14:10 – Rio Grande Ballroom

Chair: Colin McAndrew (NXP)

13:40

Everything on a Wafer Better Deliver Value

Every square micron of silicon real estate on a wafer is becoming so expensive that many semiconductor companies are deciding to either not transition to the next technology node or hold off transitioning for longer and longer than ever before. Combine this with the exponential increase in mask costs and it's easy to see why everything fabricated on a wafer should maximize return on investment. Test structures are part of that equation and must also provide value relative to their cost. This talk will examine what elements bring value and what mindset changes might be needed in the era of a slowed Moore's Law.

Jon Cheek, NXP Semiconductors

Jon Cheek earned his BSEE in Microelectronics at Texas A&M University. He began his career at Advanced Micro Devices working in the area of process integration; particularly on high performance CMOS transistors. He later moved to East Fishkill as an AMD assignee for the IBM Alliance on High Performance SOI Technology. In 2004, he joined Freescale / NXP and has focused on transistor design, embedded non-volatile memory integration, and SPICE models.

Session 3: Reliability

14:10 – 14:50 – Rio Grande Ballroom

Chair:
Stewart Smith (U. Edinburgh)

14:10

3.1 - Test Structure Design for Model-Based Electromigration

Ertugrul Demircan, Mehul D. Shroff, and Hsun-Cheng Lee

As VLSI technology features are pushed to the limit with every generation and with the introduction of new materials and increased current densities to satisfy performance demands, failure risk due to Electromigraton (EM) is ever-increasing. In this paper, we present experimental results using a novel set of test structures to validate a new model-based EM risk assessment approach. In this method, EM risk can be assessed for any interconnect geometry through an exact solution of the fundamental stress equations. This approach eliminates the need for complex look-up tables for

different geometries and can be implemented in CAD tools very easily as we demonstrate on real design examples.

14:30
3.2 - Electrostatic Test Structures for Transmission Line Pulse and Human Body Model Testing at Wafer Level
Robert Ashton, Stephen Fairbanks, Adam Bergen, and Evan Grund

New two pin ESD testers can do both Transmission Line Pulse (TLP) and Human Body Model (HBM) testing at wafer level. These systems facilitate using test structures to link fundamental circuit element parameters measured with TLP and expected HBM results on final products.

Exhibitor Presentations

14:50 – 15:20 – Rio Grande Ballroom

Chair: Scott McDade (Keysight)

Coffee Break with Exhibitors

15:20 – 15:40 – Brazos I-II-III

Session 4: Materials Characterization

15:40 – 17:20 – Rio Grande Ballroom

Chairs:
Tatsuya Ohguro (Toshiba)
Chadwin Young (U. Texas at Dallas)

15:40
4.1 - Reliability Analysis of the Metal-Graphene Contact Resistance Extracted Through the Transfer Length Method
Stefano Venica, Francesco Driussi, Amit Gahoiy, Satender Katariay, Pierpaolo Palestri, Max C. Lemmeyz, and Luca Selmi

Transfer Length Method is a well-established characterization technique for contact resistance in semiconductors; however, its dependability is questioned for metal-graphene contacts. We investigate in-depth the statistical error on the extracted contact resistance values and we devise strategies to limit such error and to determine reliable results.

16:00
4.2 - Test Structures for Seed Layer Optimisation of Electroplated Ferromagnetic Films
C. M. Mackenzie Dover, A. W. S. Ross, S. Smith, J. G. Terry, A. R. Mount, and A. J. Walton

This paper presents test structures to quantify the effect of seed layer thickness and conductivity on the plating uniformity of patterned electroplated structures. The test structures enable the effect of IR drop on the electroplated

film to be extracted and provides increased understanding to help optimize the seed layer thickness.

16:20
4.3 - Test Structures Without Metal Contacts for DC Measurement of 2D-Materials Deposited on Silicon
L. K. Nanver, X. Liu, and T. Knezevic

A set of ring-shaped test structures is presented for electrical characterization of as-deposited layers on Si that electrically interact with the substrate. The test method is illustrated by investigation of 3 different nm-thin layers that are expected to form an interfacial layer of negative fixed charge. A test procedure is described that gives a low turnaround time and non-destructive way of evaluating different deposition methods for 2D-type layers in terms of diode characteristics, interface conductance, and minority carrier injection into the deposited layer.

16:40
4.4 - Test Structures for Evaluating Al_2O_3 Dielectrics for Graphene Field Effect Transistors on Flexible Substrates
Xinxin Yang, Marlene Bonmann, Andrei Vorobiev, Kjell Jeppson, and Jan Stake

Graphene is a 2-dimensional material that has emerged as a contender for future devices, especially for flexible electronics. However, no direct contact to the graphene electrode is possible as it is mounted on an insulating substrate, so it is difficult to directly evaluate the quality of gate dielectrics. This paper presents a test structure that uses coupling through a large value capacitor formed on the same substrate to investigate the quality of Al_2O_3 dielectrics formed on graphene.

17:00
4.5 - Design of Ultraflexible Organic Differential Amplifer Circuits for Wearable Sensor Technologies
Masaya Kondo, Takafumi Uemura, Mihoko Akiyama, Naoko Namba, Masahiro Sugiyama, Yuki Noda, Teppei Araki, Shusuke Yoshimoto, and Tsuyoshi Sekitani

We have designed ultraflexible organic differential amplifier circuits for wearable sensor technologies. Transistor modeling for both p- and n-type organic thin-film transistors was done for circuit simulation. Our oganic amplifier shows high gain of 60 dB and operates with 3 V, which realizes imperceptible sensor circuits for biomedical applications.

17:20 TUESDAY CLOSE

WEDNESDAY MARCH 21

How to Write Good Papers and Get Published

8:15 - 8:45 – Rio Grande Ballroom

For established academics, raised on the "publish or perish" principle, publishing papers is a core activity. For students and industry practitioners, getting started down the road to publishing can be a daunting experience. As a "value-added" extra for interested ICMTS 2018 attendees, prior to the sessions on Wednesday there will be a talk with guidance and recommendations on how to write a good paper and get it published.

Session 5: Mismatch and Variability

9:00 – 10:20 – Rio Grande Ballroom

Chairs:
Satoshi Habu (Keysight)
Hi-Deok Lee (Chungnam National U.)

9:00
5.1 - A Test Structure to Reveal Short-Range Correlation Effects of Mismatch Fluctuations in Backend Metal Fringe Capacitors
Hans Tuinhout, Adrie Zegers-van Duijnhoven, and Ihor Brunets

This paper presents a set of DUT-1-2-1-2 capacitor matching characterization test structures that revealed a thus far unknown (at least unreported) CMP-related short-range correlated mismatch fluctuation mechanism, explaining the area scaling behavior of matching of backend metal fringe capacitors.

9:20
5.2 - Monte Carlo Analysis by Direct Measurement Using Vth-shiftable SRAM Cell TEG
Shogo Yamaguchi, Daisuke Nishikata, Hitoshi Imi, and Kazuyuki Nakamura

The measurement system in which the Monte Carlo analysis of SRAM operation can be performed in actual measurement was developed. The measured results of the Monte Carlo analysis for SRAM function test and the static noise margin evaluation were agreed well with the simulated results. The proposed method can compactly cope with the recently proposed SRAM with a larger number of transistors.

9:40
5.3 - Process Variation Estimation using A Combination of Ring Oscillator Delay and FlipFlop Retention Characteristics
Takuma Konno, Shinichi Nishizawa, and Kazuhito Ito

We propose an extraction method of process variation. Extracted process variation is modeled as threshold voltage variation. Retention characteristic of a DFF circuit has different sensitivity to threshold voltage variation from a RO circuit. We propose to introduce a DFF circuit a

complement test structure for standard RO circuit for process variation extraction. Combining RO and DFF circuits enables an accurate estimation of global process variation shift. Test structures are implemented into silicon chips and result shows global variation shift is extracted from measured data.

10:00
5.4 - NPN Mismatch Dependence on Layout
Cory Compton

Mismatch structures are normally designed to look at pairs of identical devices with near ideal layouts. In this paper, we consider the effects of orientation and NPN density on the mismatch results of NPNs in a 0.18 um SiGe BiCMOS process. The mismatch structures were added to scribe-line PCM modules, which allows us to look at the results from multiple mask sets.

Coffee Break with Exhibitors

10:20 – 10:50 – Brazos I-II-III

Session 6: On-Chip Characterization

10:50 – 12:10 – Rio Grande Ballroom

Chairs:
Christopher Hess (PDF Solutions)
Greg Yeric (ARM)

10:50
6.1 - On–Chip Reconfigurable Monitor Circuit for Process Variation and Temperature Estimation
Tadashi Kishimoto, Tohru Ishihara, and Hidetoshi Onodera

This paper proposes a monitor circuit that can estimate process variation and temperature by circuit reconfiguration. The circuit topology of the temperature monitoring is crafted such that the oscillation frequency is determined by the amount of leakage current which has an exponential dependency to temperature. The voltage dependence of this circuit is small in the configuration for temperature measurement, and the temperature dependence is small in the configuration for process variation estimation. A test chip structure fabricated in a 65 nm CMOS process demonstrates the temperature estimation capability with accuracy within -0.3 C to 0.4 C over a temperature range of 10 C to 100 C, as well as the ability for estimating threshold voltage variations.

11:10
6.2 - DFT-Enabled Within-Die AC Uniformity and Performance Monitor Structure for Advanced Process
Nui Chong, I-Ru Chen, Da Cheng, Amitava Majumdar, Ping-Chin Yeh, and Jonathan Chang

An on-chip ring oscillator based monitoring vehicle embedded within host blocks and accessed through DFT

circuit is introduced and characterized. Within-wafer AC uniformity, performance and power are analyzed in a 7 nm testchip. The design and analysis techniques described are suitable to monitor process variation, real-time power fluctuation and product performance.

11:30
6.3 - Versatile Chip-Level Integrated Test Vehicle for Dynamic Thermal Evaluation
Suresh Parameswaran, Saravanan Balakrishnan, and Boon Ang

Thermal management of semiconductor chips is becoming critical as the demand for chip performance increases. It is necessary to evaluate/manage the thermal aspects of a chip throughout the development cycle – starting from initial planning stage to deployment on customer board and beyond. In this paper, we present a versatile thermal evaluation vehicle that addresses the above requirements. This paper describes the architecture, implementation, details of operation, programming aspects, usage model and various applications of a silicon chip that is successfully used as a thermal evaluation tool.

11:50
6.4 - All-Digital On-Chip Heterogeneous Sensors for Tracking the Minimum Energy Point of Processors
Shu Hokimoto, Jun Shiomi, Tohru Ishihara, and Hidetoshi Onodera

Dynamically scaling the supply voltage (VDD) and the threshold voltage (VTH) is one of the most effective approaches for reducing the energy consumption of processors. With all-digital within-die heterogeneous sensors, we propose a simple runtime method to accurately identify the best pair of VDD and VTH, which minimizes the energy consumption of a processor under a specific operating condition which is determined by a process variation, an activity factor, and a performance requirement for the processor. Measured results for a 32-bit RISC processor integrating the heterogeneous sensors show that the proposed method successfully tracks the minimum energy operating point (i.e. the best pair of VDD and VTH) of the processor even in a case that the operating condition widely varies.

Lunch

12:10 – 13:30 – Brazos I-II-III

Keynote Talk by Greg Yeric (ARM)

13:30 – 14:00 – Rio Grande Ballroom

Chair: Brad Smith (NXP)

13:30

Test Structures Beyond Moore's Law

The field of test structures has enabled the long and impressive progression of Moore's Law, driving the parametric and random yield understanding to allow feature sizes to push from microns to nanometers. However, several different types of change are on the horizon. Standard Moore (and as importantly, Dennard) scaling advances are waning, which will require innovative solutions in semiconductor hardware. At the same time, the applications that will be consuming future semiconductor content will be expanding beyond computing and communications to new areas, such as the Internet of Things (IoT), Artificial Intelligence (AI), and healthcare. This talk will explore these changes, and explore what might be needed from the field of test structures.

Greg Yeric, ARM

Greg Yeric earned his BSEE, MSEE, and PhD in Microelectronics at The University of Texas at Austin. He began his career at Motorola's Advanced Products Research and Development Laboratories in the area of process integration, subsequently working at TestChip Technologies, HPL Technologies, and Synopsys, in the areas of test structures and yield analysis. For the last 9 years, he has been at ARM Holdings. He is an ARM Fellow, focusing on future technology and its interaction with design.

Session 7: Test Parallelism

14:00 – 14:40 – Rio Grande Ballroom

Chair:
Bill Verzi (Keysight)

14:00

7.1 - Addressable Test Structure Design Enabling Parallel Testing of Reliability Devices

Lee DeBruler, Dennis Pretti, Mike Violette, Dave Peterson, Salil Mujumdar, Xia Li, and Ken Marr

With this paper, we are showing a pad efficient design for testing reliability structures using a multiplex controlled pass gate methodology. This design enables the ability for parallel stressing of all devices and ability to identify precise failing locations. With further engineering of the pass gate this methodology should apply to all semiconductor technologies.

14:20

7.2 - Algorithm Based Adaptive Parametric Testing for Outlier Detection and Test Time Reduction

Veenadhar Katragadda, Martin Muthee, Arthur Gasasira, Frank Seelmann, and Jiun-Hsin Liao

Parallel test capability, enabled by numerous independent measurement channels has significantly increased throughput in parametric testing. It involves testing of numerous devices simultaneously synchronously or asynchronously. The number of devices tested for a given pad layout is increased by using higher dimensional arrays, the hallmark of which is pad sharing. Parallel testing of multiple devices with shared pads is vulnerable to device fails, where a failing device adversely affects measurement of all other devices.

ICMTS 2019 Presentation

14:40 – 14:50 – Rio Grande Ballroom

Coffee Break with Exhibitors

14:50 – 15:20 – Brazos I-II-III

Session 8: Device Characterization

15:20 – 17:00 – Rio Grande Ballroom

Chairs:
Kjell Jeppson (Chalmers U.)
Mark Poulter (TI)

15:20
8.1 - Evaluation of Qss on SOI Back Si/SiO_2 Interface by Newly Designed Charge Pumping Method-TEG
Kazuma Takeda, Jiro Ida, Takayuki Mori, and Yasuo Arai

The Qss of SOI back Si/SiO_2 interface was evaluated by newly designed CP-TEG. The CP method was also re-examined to apply to the thick oxide MOS. It was learned that the Qss of SOI back interface (bonded wafer interface) is comparable to that of the thermal oxidation interface.

15:40
8.2 - Quantitative Model of CMOS Inverter Chain Ring Oscillator's Effective Capacitance and Its Improvements in 14 nm FinFET Technology
Seong Yeol Mun, J. Cho, B. Zhu, P. Agnihotri, C. Y. Wong, T. J. Lee, V. Mahajan, B. W. Liu, Y. J. Shi, W. Hong, J. Ciavatti, J. G. Lee, S. B. Samavedam, and D. K. Sohn

The quantitative model of effective total capacitance, Ceff, of a CMOS ring oscillator (R/O) inverter chain in a 14 nm node FinFET 3D structure using advanced Replacement Metal Gate (RMG) is successfully extracted using all the unit capacitance components comprising the R/O, such as inverter, fan-out (F/O) MOSCAP, and metal routing. The extracted Ceff model is well validated by perfect matching to the measured Si Ceff in the R/O.

16:00
8.3 - Measurement of IGBT Trench MOS-Gated Region Characteristics Using Short Turn-Around-Time MOSFET Test Structures

Kiyoshi Takeuchi, Munetoshi Fukui, Takuya Saraya, Kazuo Itou, Shinichi Suzuki, Toshihiko Takakura, and Toshiro Hiramoto

Trench MOSFET test structures were fabricated for evaluating IGBT MOS-gated region performance. It was found that the test structures can be used for measuring saturation and sub-threshold current, though accurate estimation of linear resistance is difficult. Charge pumping measurement can be used to evaluate the oxide/substrate interface quality, for possible application to process optimization.

16:20
8.4 - Sensitivity of High-k Encapsulated MoS_2 Transistors to I-V Measurement Execution Time
Pavel Bolshakov, Ava Khosravi, Peng Zhao, Paul K. Hurley, Robert M. Wallace, and Chadwin D. Young

MoS_2 FETs encapsulated in a high-k environment were fabricated and electrically characterized. Changes in gate voltage step and measurement speed were introduced and compared to study the effects on the I-V response. This study demonstrated significant changes in subthreshold slope and threshold voltage in part due to charge trapping at the high-k/MoS_2 interface, which can alter device performance.

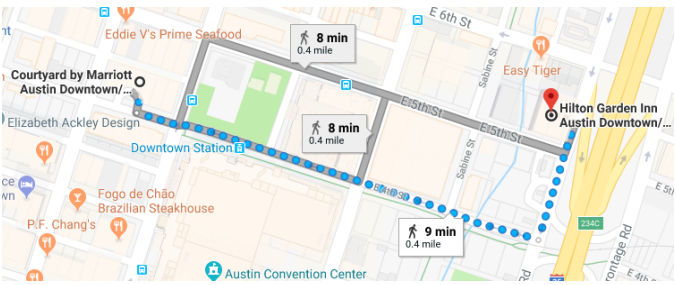
16:40
8.5 - Total Ionizing Dose Effects on Analog Performance of 65 nm Bulk CMOS with Enclosed-Gate and Standard Layout
Matthias Bucher, Aristeidis Nikolaou, Alexia Papadopoulou, Nikolaos Makris, Loukas Chevas, Giulio Borghello, Henri D. Koch, and Federico Faccio

High irradiation doses cause significant shifts in design parameters of standard bulk silicon CMOS. Analog performance of a commercial 65 nm CMOS technology is examined for standard and enclosed gate layouts, with Total Ionizing Dose (TID) up to 500 Mrad. The paper provides insight in geometrical and bias dependence of key design parameters such as threshold voltage, DIBL, transconductance efficiency, slope factor, and intrinsic gain.

17:00 WEDNESDAY CLOSE

18:30 Banquet and Casino Night

HILTON GARDEN INN AUSTIN DOWNTOWN



THURSDAY MARCH 22

How to Prepare and Make Good Presentations

8:15 - 8:45 – Rio Grande Ballroom

Once your conference paper is accepted, or when you want to communicate your developments within your company, you will have to prepare and present slides. Besides being nervous of public speaking, many people make elementary mistakes in slides that diminish the impact of a presentation. As a “value-added” extra for interested ICMTS 2018 attendees, prior to the sessions on Wednesday there will be a talk with guidance and recommendations on how to prepare for and make a good presentation.

Session 9: MEMS

9:00 – 10:20 – Rio Grande Ballroom

Chairs:
Richard Allen (NIST)
Kiyoshi Takeuchi (U. Tokyo)

9:00
9.1 - An On-Chip Test Structure for Studying the Frictional Behavior of Deep-RIE MEMS Sidewall Surfaces
R. Ranga Reddy, Yuki Okamoto, and Yoshio Mita

An on-chip micro-mechanical test structure has been developed to investigate the friction behavior of Deep-RIE sidewall contacting surfaces of single crystal silicon which is most widely used in micromechanical systems (MEMS). Two orthogonally placed electrostatic comb-drive actuators were adopted to apply the normal load and generate the tangential motion on sidewall surfaces. Through experiments, it was found that with the increment of normal forces, the static friction coefficient is no longer a constant value and it has less effect on dynamic friction coefficient. DRIE process parameters greatly influence the frictional properties on both static and dynamic friction coefficients.

9:20
9.2 - Wafer Level Characterisation of Microelectrodes for Electrochemical Sensing Applications
E. O. Blair, L. Parga Basanta, I. Schmueser, J. R. K. Marland, A. Buchoux, A. Tsiamis, C. Dunare, M. Normand, A. A. Stokes, A. J. Walton, and S. Smith

This work presents a system for making measurements of electrochemical sensor test structures at wafer-level. Normally such sensors need to be diced and packaged, but by integrating the characterization step into the fabrication process, developing electrochemical sensors becomes faster and less expensive. This abstract presents initial measurements demonstrating the capability of making electrochemical measurements on test structures on a probe station.

9:40
9.3 - Test Structure for Electrical Assessment of UV Laser Direct Fine Patterned Material
Naoto Usami, Akio Higo, Ayako Mizushima, Yuki Okamoto, and Yoshio Mita

We propose a test structure to electrically assess direct laser fine patterning, which is entering a microelectronic era (below 10 mm). Indium-Tin-Oxide (ITO) was used as a material example. High speed ITO patterning with laser ablation contributes short turn-around-time development of opto-electrical devices, such as organic light emitting diode. However, not only machine-induced line-edge fluctuation but also the process (e.g. heat) induced material degradation may affect electrical linewidth. The aim of our test structure is to assess such critical dimension change through measurement of electrical property (i.e. conductivity). It consists of Kelvin connection straight lines and Greek crosses with various widths. Ultraviolet (UV) laser process as well as lithography and plasma etching were applied with the same test structure. The measurement revealed that the applied direct patterning condition induced small damage, showing applicability of direct patterning in microelectronics R&D.

10:00
9.4 - Open Model for External Mechanical Stress of Semiconductors and MEMS
R. T. Buhler and R. C. Giacomini

This paper defines the details of the bending equipment solution and the calibration required for characterization of external mechanical stress in semiconductors or MEMS. The equipment is suited for use in probe station for electrical characterization of devices under controlled external mechanical stress.

Coffee Break

10:20 – 10:50 – Brazos I-II-III

Session 10: Noise and RF

10:50 – 12:10 – Rio Grande Ballroom

Chairs:
Hans Tuinhout (NXP)
Anthony Walton (U. Edinburgh)

10:50
10.1 - Importance of Complete Characterization Setup on On-Wafer TRL Calibration in Sub-THz Range
Chandan Yadav, Marina Deng, Magali De Matos, Sebastien Fregonese, and Thomas Zimmer

In this paper, we present the effect of different sub-mm and mm-wave probe geometry and topology on the measurement results of dedicated test structures combined with on-wafer TRL calibration along with simulation results of intrinsic test structures carried out in HFSS. The limitation of on-wafer TRL calibration is pointed out for some sub-mm and mm-wave probes.

11:10
10.2 - Measurement Time Reduction Technique for Input Referred Noise of Dynamic Comparator
Yuki Ishijima, Shuya Nakagawa, and Hiroki Ishikuro

A measurement technique to reduce the measurement time of input referred noise in dynamic comparator is presented. By using binary search method to detect the standard deviation of input referred noise and offset, proposed technique can reduce the measurement time by a factor of n/log2(n).

11:30
10.3 - System Aware DUT Design for Optimum On-Wafer Noise Measurement
Chih-Hung Chen, Benson Yang, Pei-Hsien Chua, Graham Brown, and Saswati Das

This paper presents a system-aware design of device-under-tests (DUT) for optimum on-wafer noise measurement. It overcomes the challenge due to the voltage drop in the interconnections of a large DUT. It also prevents the inaccuracy from a small DUT. Experimental data and suggested device sizes for different technologies are presented.

11:50
10.4 - Measurement of Temperature Effect on Random Telegraph Noise Induced Delay Fluctuation
A. K. M. Mahfuzul Islam, Masashi Okay, and Hidetoshi Onodera

We present detailed measurement results of temperature effect on Random Telegraph Noise (RTN) induced delay fluctuation using a test chip fabricated in a 65-nm Silicon-On-Thin-Buried-Oxide process. Skewed ring oscillators (ROs) are used to evaluate pMOSFET and nMOSFET specific RTN effects. Furthermore, threshold voltage distributions have been extracted such that the simulated delay distribution matches with the measured delay distributions. Measurement results reveal that with the increase of temperature RTN effect decreases. However, low correlation coefficients of 0:3 to 0:4 have been found between 0 C and 80 C for different ROs. Low correlation poses challenges in realizing robust runtime performance compensation techniques such as replica critical path based delay compensation.

Best Paper Announcement, Conference Close

12:10 – Rio Grande Ballroom

EXECUTIVE COMMITTEE

General Chair	Colin McAndrew (NXP)
Technical Program Chair	Brad Smith (NXP)
Tutorial Chair	Chadwin Young (UT Dallas)
Equipment Chair	Scott McDade (Keysight)
Conf. Manager	Catherine Shaw (C. Shaw LLC)
US Steering Committee	Bill Verzi (Keysight)
US Steering Committee	Larg Weiland (PDF Solutions)
Website	Yoshio Mita (U. Tokyo)

TECHNICAL PROGRAM COMMITTEE

Richard Allen	NIST
Yuzo Fukuzaki	Sony Corp.
Satoshi Habu	Keysight Technologies
Christopher Hess	PDF Solutions
Kjell Jeppson	Chalmers U. Technology
Chang Yong Kang	Nvidia
Mark Ketchen	Octevue
Johan Klootwijk	Philips Research
Alexey Kovalgin	U. Twente
Hi-Deok Lee	Chungnam National U.
Emilio Lora-Tamayo	Menéndez Pelayo Int'l. U.
Alan Mathewson	Tyndall National Institute
Hiroaki Matsui	U. Tokyo
Colin McAndrew	NXP Semiconductors
Kevin McCarthy	U. College Cork
Yoshio Mita	U. Tokyo
Jerome Mitard	IMEC
Tatsuya Ohguro	Toshiba Corp.
Mark Poulter	Texas Instruments
Tsuyoshi Sekitani	U. Osaka
Luca Selmi	U. Modena and Reggio Emilia
Brad Smith	NXP Semiconductors
Stewart Smith	U. Edinburgh
Kiyoshi Takeuchi	U. Tokyo
Bing-Yu Tsui	National Chiao Tung U.
Hans Tuinhout	NXP Semiconductors
Bill Verzi	Keysight Technologies
Anthony Walton	U. Edinburgh
Larg Weiland	PDF Solutions
Greg Yeric	ARM
Chadwin Young	UT Dallas

STEERING COMMITTEE

Bill Verzi (USA)	Keysight Technologies
Larg Weiland (USA)	PDF Solutions
Satoshi Habu (Japan)	Keysight Technologies
Yoshio Mita (Japan)	U. Tokyo
Anthony Walton (Europe)	U. Edinburgh
Luca Selmi (Europe)	U. Modena and Reggio Emilia

ICMTS 2018 Exhibitors

CELADON™

EVERBEING
EVERBEING INT'L CORP.

KEITHLEY
A Tektronix Company

KEYSIGHT
TECHNOLOGIES

MPI

PDA
PLATFORM DESIGN AUTOMATION, INC.

PROPLUS
The DFY Technology Provider

SEMIPROBE™