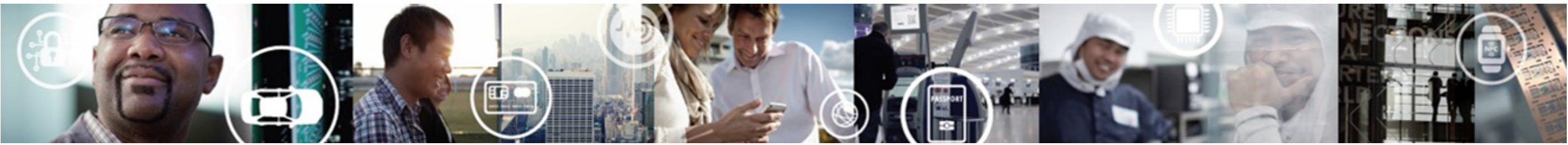
HOW TO WRITE A GOOD PAPER AND GET IT PUBLISHED

COLIN MCANDREW



NXP

SECURE CONNECTIONS FOR A SMARTER WORLD

Warning

- this is a **very** boring presentation!
  - lots of words
  - few pictures

- do **not** use as an example for your conference presentation!
  - see Brad Smith’s “bonus” talk: How to Prepare and Make Good Presentations

Why Listen to Me?

- published 1 book, 11 book chapters, 77 conference papers, 62 journal papers
  - I am from industry, not academia, these are usually “after hours” activities
- 4 best paper awards
  - IEEE ICMTS 1993 and 2012, IEEE CICC 2002, IEEE BCTM 2015
- have reviewed / handled many 1000’s of papers
  - editor IEEE Trans. Electron Devices (TED) 2001-2010
  - editor IEEE Journal of the Electron Devices Society (JEDS) 2013-2022
  - IEEE BCTM committee 1994-2004
  - IEEE ICMTS committee 2000-2020
  - IEEE CICC committee 2000-2020
  - IEEE BMAS committee 2004-2010

Why Should You Publish?

- in academia, it is an expected part of the job
  - for students and Professors
- in industry
  - some companies pay you for publishing
  - mainly for personal satisfaction, peer recognition, career development/advancement
  - it looks good for your company
    - sends a message to customers/competitors about innovation and R&D investment
    - helps attract and retain top technical talent
    - projects that there is a rewarding and valued technical career path

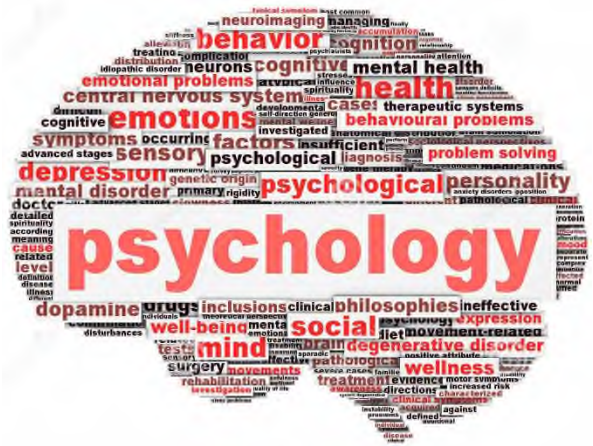
What Should You Publish?

- don’t assume your daily work is **not** worth publishing
- don’t assume your daily work **is** worth publishing
  - get to know what conferences and journals are interested in
    - to find appropriate targets for submission
  - become aware of existing state-of-the-art

- for research
  - should significantly advance the technical state-of-the-art
  - target archival journals and IEEE IEDM, VLSI, IEEE CICC, IEEE ISSCC
- for engineering application
  - should be practically useful
  - IEEE ICMTS is a terrific venue

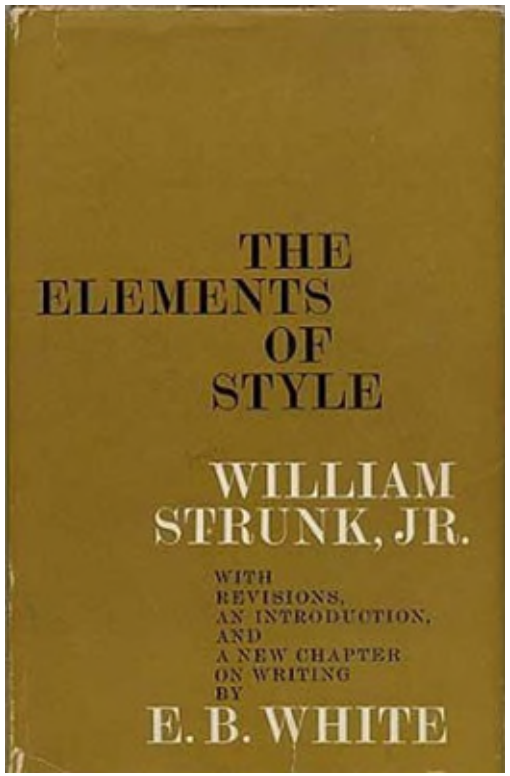
Do’s

- keep abreast of conferences in your work area and what you can contribute
  - attend and participate even if you aren’t presenting a paper
  - get to know people at, and get involved with, a conference
    - best way is to publish papers at the conference
- keep abreast of the present state-of-the-art
  - that way you can better evaluate the degree of advance of your contributions
  - reviewing conference and journal submissions forces you to do this
- reference original sources (not just your previous papers!)
- submit an abstract to a conference
  - not too much effort to write
  - forces you to write a full paper when accepted!



Do’s (Continued)

- keep a list of potential topics you can write a paper on
  - I have done this, for over 30 years
  - work on these as time permits
    - yes, this involves time outside of work
- practice and hone writing and presentation skills
  - read “Strunk and White”
  - use the Oxford comma
  - good presentations make a significant positive impact
    - for you
    - for your company / institute
  - use internal company / institute forums to improve these skills



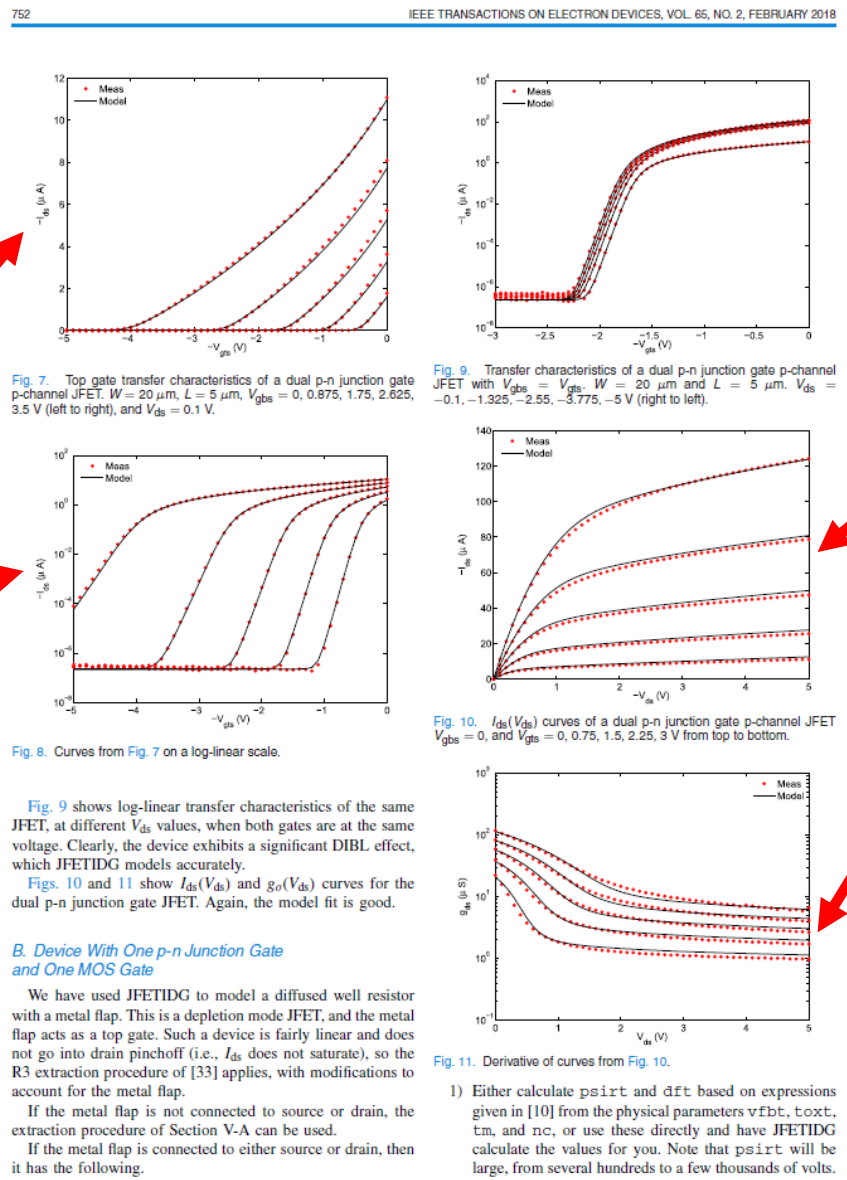
Do’s (Continued)

- take pride in, and be very picky about, being perfect in **every** single detail
  - define all symbols and acronyms when used first
  - use the same font and style for symbols **everywhere**
    - in equations, text, figures, tables, captions
    - tricky if plotting / typesetting package fonts are different – make as close as possible
  - place imported pictures in the same alignment in documents and presentations
    - it is distracting to have them shift around
  - when constructing drawings, schematics, etc. make sure all lines are aligned, snapped to grid, consistent lengths, ...
    - I use 1/10-inch grid, try to keep major lines on integer inches or 1/5 inches, it helps scaling
  - these small details make a difference, imperfections detract from technical impact

Examples

linear-linear and log-linear plots of the same data aligned vertically

$I_D(V_D)$ and $g_o(V_D)$ plots aligned vertically



752 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 65, NO. 2, FEBRUARY 2018

Fig. 7. Top gate transfer characteristics of a dual p-n junction gate p-channel JFET. $W = 20\ \mu m$, $L = 5\ \mu m$, $V_{gbs} = 0, 0.875, 1.75, 2.625, 3.5$ V (left to right), and $V_{ds} = 0.1$ V.

Fig. 8. Curves from Fig. 7 on a log-linear scale.

Fig. 9 shows log-linear transfer characteristics of the same JFET, at different V_{ds} values, when both gates are at the same voltage. Clearly, the device exhibits a significant DIBL effect, which JFETIDG models accurately.

Figs. 10 and 11 show $I_{ds}(V_{ds})$ and $g_o(V_{ds})$ curves for the dual p-n junction gate JFET. Again, the model fit is good.

B. Device With One p-n Junction Gate and One MOS Gate

We have used JFETIDG to model a diffused well resistor with a metal flap. This is a depletion mode JFET, and the metal flap acts as a top gate. Such a device is fairly linear and does not go into drain pinchoff (i.e., I_{ds} does not saturate), so the R3 extraction procedure of [33] applies, with modifications to account for the metal flap.

If the metal flap is not connected to source or drain, the extraction procedure of Section V-A can be used.

If the metal flap is connected to either source or drain, then it has the following.

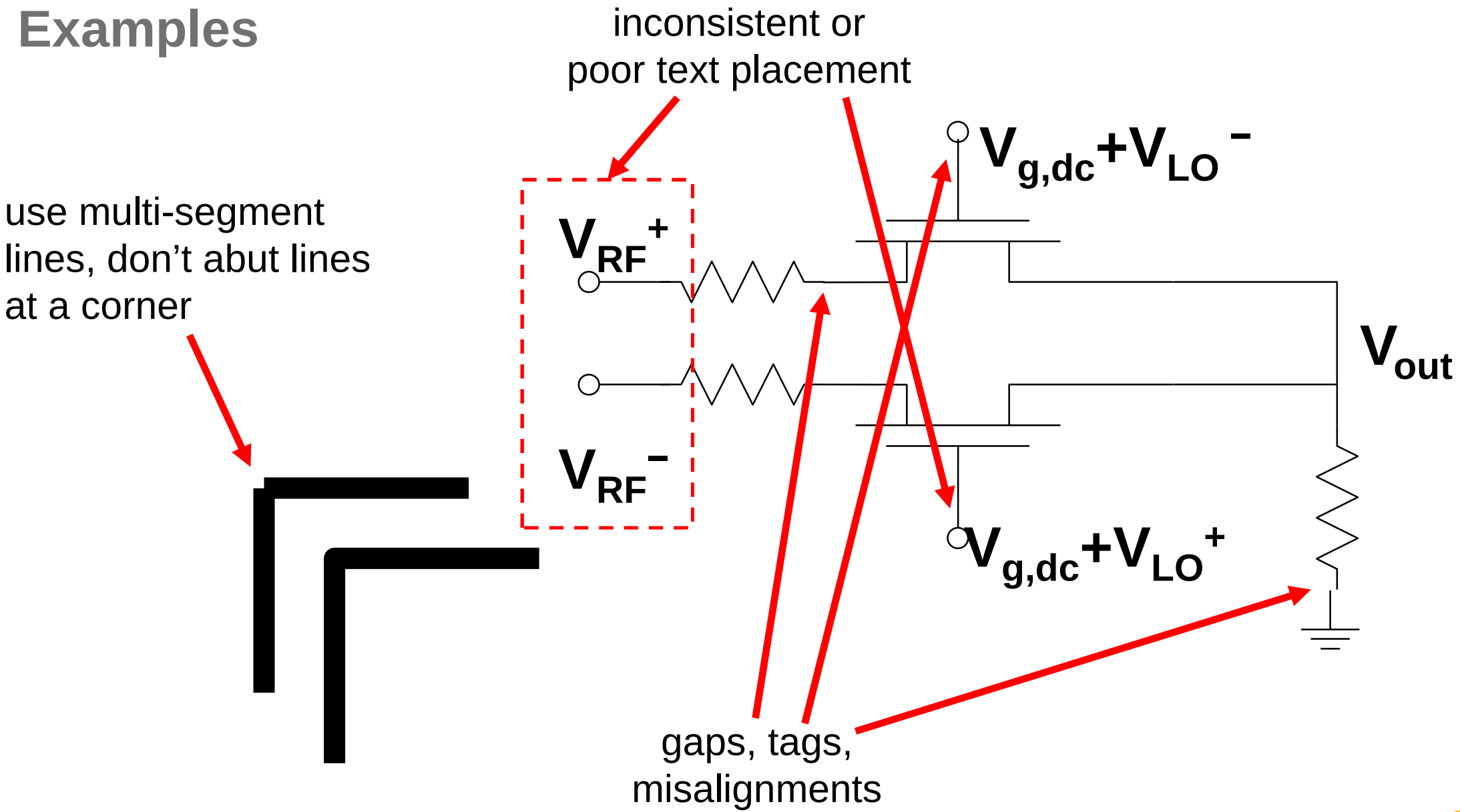
Fig. 9. Transfer characteristics of a dual p-n junction gate p-channel JFET with $V_{gbs} = V_{gts}$. $W = 20\ \mu m$ and $L = 5\ \mu m$. $V_{ds} = -0.1, -1.325, -2.55, -3.775, -5$ V (right to left).

Fig. 10. $I_{ds}(V_{ds})$ curves of a dual p-n junction gate p-channel JFET $V_{gbs} = 0$, and $V_{gts} = 0, 0.75, 1.5, 2.25, 3$ V from top to bottom.

Fig. 11. Derivative of curves from Fig. 10.

1) Either calculate `psirt` and `dft` based on expressions given in [10] from the physical parameters `vfbt`, `toxt`, `tm`, and `nc`, or use these directly and have JFETIDG calculate the values for you. Note that `psirt` will be large, from several hundreds to a few thousands of volts.

Examples


inconsistent or
poor text placement
use multi-segment
lines, don't abut lines
at a corner
V_{RF}^+
V_{RF}^-
$V_{g,dc}+V_{LO}^-$
$V_{g,dc}+V_{LO}^+$
V_{out}
gaps, tags,
misalignments

Recommendations

- use LaTeX for typesetting rather than MS-Word
  - looks **much** better and more professional
  - has no issues with figures moving around and destroying your document
  - many Windows versions freely available (I use MiKTeX)
  - with BibTeX it is easy to set up, and re-use, references
- for figures use matplotlib in python, and use this color palette
  - #648FFF, #DC267F, #FFB000, #FE6100, #785EF0
  - it is designed to be distinguishable for people who are color-blind
- make your paper “look” like a paper
  - balance text, equations, and figures so it “looks” nice

Example

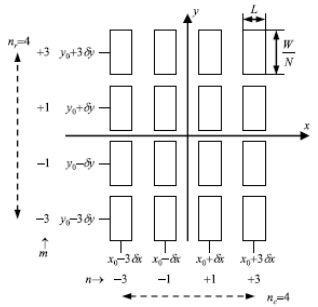


Fig. 1. 2-D Manhattan grid layout.

There has been a difference of opinion in [12] and [26], as to whether the effects of linear process gradients do or do not inherently cancel in CC layouts. We explain why, and under what conditions, both points of view are correct.

The basic layout is assumed to be of identical rectangular sections placed in an equally spaced Manhattan grid. Such layout restrictions are typical of those in modern CMOS processes. Matching routing is also important [19], [23]; we do not address that here, but have verified that our layouts are indeed routable. Our goal is to provide an analytical formulation that assists transparent and intuitive understanding of what CC layout entails.

The nomenclature used is as follows. The two devices, and sections thereof, are denoted by A and B. The number of columns and rows of the Manhattan grid are n_r and n_c, respectively, and the indices of a section of the grid in the x- and y-directions are n and m, respectively. i and j are generic non-negative integers, o are odd positive integers, and e are even non-negative integers.

II. Single Section Analysis

Consider device sections placed as in Fig. 1, comprising n_r rows and n_c columns. The device could be of any type (MOS transistor, bipolar transistor, capacitor, resistor, etc.), but we will consider the total device length and width to be L and W, respectively, being broken into N sections each of length L and width $w = W/N$ (this is appropriate for MOS transistors; resistors would normally be broken along the length direction, which is just a geometry label swap). The half-pitches between the sections are δx and δy in the x- and y-directions, respectively, and the reference point (x_0, y_0) is taken as the CC point of all of the sections (it could be arbitrary; the reason for this selection will become apparent). Each section can be represented by a pair of integer indices (n, m) where the center of the section is $(x_0 + n\delta x, y_0 + m\delta y)$.

If there are even numbers of rows and columns of device sections in the layout then (n, m) are odd. For the layout of Fig. 1, $n, m \in \{-3, -1, 1, 3\}$.

If there is an odd number of rows then y_0 is located at the y-direction middle of the middle row, and m takes on even values. If there is an odd number of columns then x_0 is located at the x-direction center of the center column, and n takes on even values.[1]

Assume a quadratic spatial dependence for each process parameter p of interest, so

$$p(x, y) = p_0 + s_x(x - x_0) + s_y(y - y_0) + \frac{1}{2}s_{xx}(x - x_0)^2 + \frac{1}{2}s_{yy}(y - y_0)^2 + s_{xy}(x - x_0)(y - y_0) \quad (1)$$

where $p_0 = p(x_0, y_0)$, $s_x = \partial p/\partial x$ and $s_y = \partial p/\partial y$ are the linear gradient components in the x- and y-directions, respectively, and $s_{xx} = \partial^2 p/\partial x^2$, $s_{yy} = \partial^2 p/\partial y^2$, and $s_{xy} = \partial^2 p/\partial x \partial y$ are the quadratic gradient components. For a process gradient that is radial the coefficients in (1) depend upon position within a wafer.

For section (n, m) the effective (i.e., average) value of p over that section is

$$\bar{p}(n, m) = \frac{1}{wL}\int_{x_0+n\delta x-L/2}^{x_0+n\delta x+L/2}\int_{y_0+m\delta y-w/2}^{y_0+m\delta y+w/2} p(x, y)dy\,dx = p_0 + ns_x\delta x + ms_y\delta y + s_{xx}\frac{L^2 + 12n^2\delta x^2}{24} + s_{yy}\frac{w^2 + 12m^2\delta y^2}{24} + nms_{xy}\delta x\delta y. \quad (2)$$

Note that the L^2 and w^2 terms in (2) mean that computing $\bar{p}$ as $p(x_0 + n\delta x, y_0 + m\delta y)$, as done in some previous analyses, is correct only if the process gradient is linear.

It is straightforward to extend (2) to higher order process gradients; if p is modeled by a kth order Taylor expansion then (2) generalizes to

$$\bar{p}(n, m) = p_0 + c_0 + \sum_{i=1}^{k}\sum_{j=0}^{i} c_{i,j}n^{i-j}m^j \quad (3)$$

where the c are constant coefficients.

III. Analysis of Multiple Section Device

For a device A, averaging (3) over all N sections gives an effective value of p for the device of

$$\bar{p}_A = p_0 + c_0 + \frac{1}{N}\sum_{A}\sum_{i=1}^{k}\sum_{j=0}^{i} c_{i,j}n^{i-j}m^j. \quad (4)$$

A similar form holds for $\bar{p}_B$, the effective value of p for a second device B, with the summations changed to be over the (n, m) indices of the sections of that device. Note that the form (4) is independent of the choice of (x_0, y_0) because an origin shift maps a polynomial into a polynomial of the same

[1] There cannot be an odd number of both rows and columns as this gives an odd number of total sections, but we are considering two devices so the total number of sections must be even.

order with different coefficients. The two devices A and B match, i.e., cancel process gradients up to the kth order, when $\bar{p}_A = \bar{p}_B$.

The p_0, c_0, and $c_{i,j}$ coefficients in (4) and its equivalent for $\bar{p}_B$ are the same for both devices, so the first two terms on the right-hand side of (4) are automatically the same for device A and device B. Therefore, the criteria for an interdigitated layout to balance nonlinear process gradients up to order k are that the rest of the terms on the right-hand side of (4) match. Each $c_{i,j}$ can be an arbitrary value, so the summations of the products of the powers of the section indices must be the same for each separate possible combination of powers, so we must have

$$\sum_A n^i m^j = \sum_B n^i m^j,\ i, j = 0, 1, 2, \ldots,\ i + j \le k. \quad (5)$$

These criteria reduce evaluation of whether a layout cancels the effect of process gradients to simple integer arithmetic and comparison; you do not have to explicitly evaluate the integrals in (2).

If n_c is even then our indexing scheme gives $n \in \{-(n_c - 1), \ldots, -3, -1, 1, 3, \ldots, n_c - 1\}$ or if n_c is odd then $n \in \{-(n_c - 1), \ldots, -2, 0, 2, \ldots, n_c - 1\}$, and similarly for m. In each row, for every section with a negative value for n there is a corresponding section with a positive value of the same magnitude. Therefore

$$\sum_{row} n^o = 0, o = 1, 3, 5, \ldots \quad (6)$$

holds for every row, i.e., the sum of all odd order powers of n must be zero in each row. Now m is constant in each row, so

$$m^i \sum_{row} n^o = \sum_{row} n^o m^i = m^i \times 0 = 0. \quad (7)$$

Summing (7) over all rows, for the total sum for all sections of devices A and B gives

$$\sum_{A+B} n^o m^i = \sum_{A+B} n^i m^o = 0 \quad (8)$$

where we include the equivalent result from summing any odd power of m in each column, which must be zero, and then summing over all columns. Separating the sums over the different devices A and B gives

$$\sum_A n^o m^i = -\sum_B n^o m^i,\ \sum_A n^i m^o = -\sum_B n^i m^o. \quad (9)$$

But we see from (5) that the summation terms on either side of each equality sign in (9) must also be equal, and zero is the only number whose negative is the same as its value. Therefore, for sums involving odd order powers we have the stronger conditions

$$\sum_A n^o m^i = \sum_B n^o m^i = 0 \quad i + o \le k.$$
$$\sum_A n^i m^o = \sum_B n^i m^o = 0. \quad (10)$$

For first order gradients ($o = 1$, $i = 0$) this is just a statement that the sections for each device must be laid out in a CC configuration.

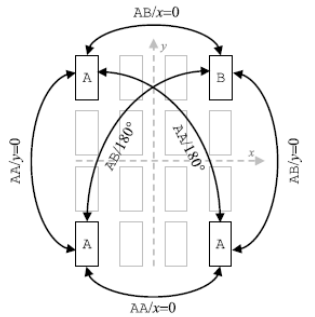


Fig. 2. Rotational and reflectional symmetries.

For first and second order process gradient cancellation the criteria (5) and (10) are

$$\sum_A n = \sum_B n = 0$$
$$\sum_A m = \sum_B m = 0$$
$$\sum_A n^2 = \sum_B n^2$$
$$\sum_A nm = \sum_B nm = 0$$
$$\sum_A m^2 = \sum_B m^2. \quad (11)$$

IV. Quantification of Layout Symmetries and Their Consequences

Because of our choice of indexing scheme, it becomes possible to explicitly quantify what "symmetry" means for a layout and very simply evaluate how each symmetry contributes to the criteria (5) and (10).

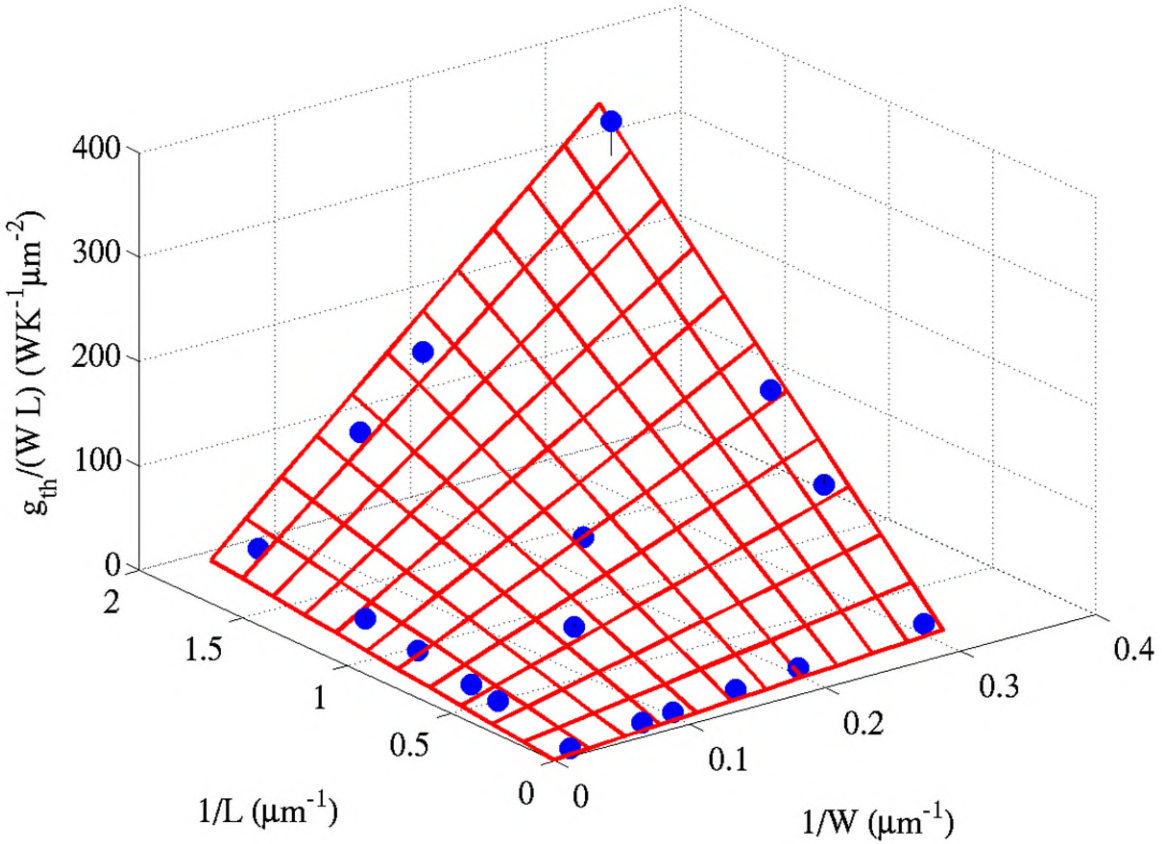
In the discussion below: "AA symmetry" means that, under the operation specified, sections of device A map into sections of device A and sections of device B map into sections of device B; "AB symmetry" means that, under the operation specified, sections of device A map into sections of device B, and *vice versa*; "/$x = 0$" means reflection about $x = 0$ (i.e., about the y-axis); "/$y = 0$" means reflection about $y = 0$ (i.e., about the x-axis); "/180°" means rotation by 180° (i.e., reflections about both the y- and x-axis).[2] Fig. 2 can help visualize these operations and symmetries (mentally perform the rotation and reflection operations in your head).

If a layout has AA/$x = 0$ symmetry then, for even n_c, for every section of each device there is a corresponding section

[2] Here "rotation" always means about the origin (x_0, y_0), which is also the CC point.

Use Plots/Charts Rather Than Tables to Show Data

L	W	g_{TH}
60	0.65	5.733e-5
10.8	0.65	1.419e-4
7.2	0.65	2.026e-4
3.6	0.65	3.753e-4
60	0.98	3.789e-4
60	1.3	2.963e-5
3.6	1.3	1.883e-4



if you do use tables, format numbers to align vertically and look nice

note: this plot is from an older paper of mine, done with Matlab; today I would use matplotlib in python, which gives visually much nicer plots

Do Not’s

- do not submit junk
  - you look bad, your company / institute looks bad, wastes reviewers’ time
- do not separate your developments into MPUs (Minimum Publishable Units)
  - you look bad, your company / institute looks bad
- do not publish the same material multiple times in multiple places
  - exception is review / invited paper to summarize a body of work
  - subsequent journal publication of conference paper is OK
    - requires “enhanced” and “more complete” version (“at least a third ... enhanced ... material”)
  - previously archival journals were more widely available than conference proceedings
    - so, publication of a good conference paper in a journal was OK
  - not so now with IEEEXplore, content must be differentiated

Predatory Journals

- never, ever publish in predatory journals
  - if you have not received solicitations yet, you will
  - you will be asked to pay $$$, there is no peer review, it is a money-making scam
  - you may even receive an offer to become an editor
- Beall's used to be the go-to source, but has been silenced
  - https://cabells.com/about-blacklist is the new best place to check
- some academics at "lesser" US colleges have flooded the scam system
  - they got swept up in "publish or perish" tsunami
- if your institute / company counts publications, not outlet / content, GET OUT!
- publish in reputable places, for example the IEEE
- never, ever publish in predatory journals

Tone of a Submission

- always be technically correct
  - if root cause is unknown, present all possibilities, not just one
  - speculate only when you must, and be clear you are doing so
- always be politically correct

- by submitting a technical paper, you are often implicitly saying that previous work is wrong, inaccurate, or in some other way has problems
  - do **not** use statements like “the previous work [X] is wrong because ...”
  - **do** use statements like “we improve on the previous work of [X] because ...”

- remember: the person reviewing your submission may be a person whose work you are building on, so be diplomatic ...

Content of a Submission

- follow guidelines for submission (format, length, ...)
  - many conferences ask for abstracts, full papers after acceptance
- don’t re-iterate all the history of the field
  - reviewers and future readers should know it
  - graduate students tend to do this (the information is, for them, relatively new)
- be very clear about what the advance is
  - passive descriptions may not make clear what is already known and what you have done
  - say “this submission advances the state-of-the-art because ...”
    - stands out to a reviewer going through 70 conference submissions
  - balance modesty / bragging and clarity

What Reviewers will Do and will Say

- most conferences / journals try **really** hard to objectively evaluate submissions
- but not every reviewer will be an expert in the subject area of your submission
  - especially for conference submissions
- there may be misunderstanding of content and contribution
  - less likely with “this submission advances the state-of-the-art because ...”
- adopt “feedback is a gift” mindset
  - constructive criticism is always beneficial
  - if you act on it, you will get published

Negative Reviews of Conference Submissions

- many have a “closed door” policy
  - no feedback on why a submission was accepted or rejected
- there are some complaints from authors about decisions
  - whackos and psychos
    - web-based submission is increasing the number of these
    - of the many 1000’s of submissions I have been involved with I have only had a few of these
  - disgruntled authors
    - some are legitimate, based on reviewers not understanding submission
    - some are just “sour grapes”
  - legitimate inquiries
    - really want constructive feedback

Negative Reviews of Journal Submissions

- easy decisions are clear cut reject and clear accept
  - there is a large gray area in the middle
- when pressed to make a decision it may be to reject
- if the reviews are weak and miss the mark, **push back**!
- be polite and diplomatic in your rebuttal
  - revise the manuscript as recommended if the comment / criticism is correct
    - thank the reviewer in your cover letter
  - clearly explain why other reviewers' comments are wrong
- if you are correct there is a **very** good chance your submission will be accepted
  - persistence can pay off
- do not "shop around" to lesser journals, this is detected and makes you look bad

Misunderstandings in Reviews

- reviewers / editors may not understand, or misunderstand, what you have written
- do **not** respond with detailed analysis of how everything negative pointed out is, pedantically, already covered in places X, Y, and Z in the manuscript
  - reviewers have limited time for evaluations, as will eventual readers
- if reviewers had trouble understanding your submission others will too
  - even if it is technically correct
- the impact of your submission will be greatly diminished if published as-is
  - people will not easily understand your work
- “feedback is a gift”
  - improve the clarity of your manuscript, don’t argue with the reviewers or editor

Final Recommendations

- you will learn better what to do by doing it, so do it, and practice doing it
  - writing
  - presentations
- think like a reader / listener who is not as familiar with your work as you are
  - what have you assumed they know but likely do not?

1. make and continually update your list of possible paper topics
2. write and submit your papers as time permits
3. go back to step 1