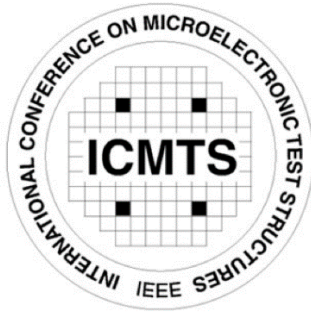


30th ICMTS

2017 IEEE International Conference on
Microelectronic Test Structures



March 27-30, 2017
Maison Minatec
3 Parvis Louis Néel,
38054 Grenoble (France)



Technically Sponsored by:
The IEEE Electron Device Society

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WELCOME LETTER

Dear Colleagues,

the 30th International Conference on Microelectronic Test Structures will be held in Grenoble (France) at The Maison Minatec 3 Parvis Louis Néel, 38054 Grenoble. This year it is organized by the LETI CEATech in collaboration with IMEP/INPG, and it is technically co-sponsored by the IEEE Electron Devices Society.

The conference will be held on March 28 to 30, 2017, and will be preceded by a one day Tutorial Short Course on microelectronic test structures on March 27.

This event will bring together designers and users of test structures to discuss recent developments and future directions, in a one track program, with convivial breaks allowing attendees to discuss and exchange viewpoints and challenges.

Since the first one was held in Long Beach in 1988, this is the 30th session, the 10th in Europe and the 1st in France.

The technical program will include 9 sessions relevant to ICMTS criteria and containing large area topics, with test structures measurements and results. As in previous editions, one session will be dedicated to equipment exhibition by companies focusing their business on test structures characterization.

For the 1st time, this session will also present a European project: ASCENT which provides access to Research infrastructures and programs for advanced CMOS and other test structures for experimentation and testing.

The Conference will be hosted within the "Maison Minatec", located at walking distance to the Main Train Station ("Gare de Grenoble") and the Airport Shuttle Station ("Gare Routière") close to many restaurants and hotels. Grenoble downtown with many tourist attractions is close by. The Tourist Office would be very pleased to give you a kind welcome and plenty of information. <http://www.grenoble-tourisme.com/fr/>

The Minatec innovation campus is an international hub for micro and nanotechnology research; it achieves strong connections between research, education and industry; it is home to some 3000 researchers, 1200 students, and 600 business and technology transfer experts, on a 20-hectare state-of-the-art campus with 13000 m² of clean room space.

An attractive social program is offered to the conference registered and accompanying persons. This includes a Welcome Reception on Monday evening at the Maison Minatec; The Conference Banquet on Wednesday evening at "La Bastille" with cable car run for a gorgeous view on the city and the alpes; and, on Thursday afternoon, a guided tour of the ancient city heart of Grenoble.

We hope to welcome you in Grenoble in March!

Sincerely,

Alain Toffoli and Gérard Ghibaudo, General Chairmen

Hans Tuinhout, Technical Program Chair

Gilles Reimbold, Tutorial Chair

Amal Chabli and Antoine Cros, Exhibition Chairs

Florian Vuong, Carlo Cagli and Jean Coignus, Local Arrangements Chairs

GENERAL INFORMATION

Conference Information

The 2016 International Conference on Microelectronic Test Structures is organized by the Leti – CEA of Grenoble in collaboration with IMEP/INPG and it is technically co-sponsored by the IEEE Electron Devices Society. The purpose of this conference is to bring together designers and test structures users to discuss recent developments and future directions of research on test structures or enabled by test structures. A rich one-day Tutorial Short Course is proposed the day before the conference start. Tutorials cover a large variety of technical areas related to Microelectronic Test Structures.

Both the Tutorials and the Technical Sessions will all be held at the “Maison Minatec”, Salle Titane. The full address is 3, Parvis Louis Néel, Grenoble.

Web Site and Email Contacts

The ICMTS 2017 Website has the following address:

<http://icmts2017.insight-outside.fr/>

Email Contact for general information:

ICMTS2017@insight-outside.fr

Presentations

The official language of the conference is English. This year all presentations will be oral, and the allowed time for each speaker is 15 minutes, followed by 5 minutes for questions and answers.

We encourage all authors to send a copy of their presentations to ICMTS2017-Abstract@insight-outside.fr at latest on March the 17th. The official format for presentation is PowerPoint file .pptx; the format .ppt although accepted is discouraged for compatibility issues. Adobe PDF files are also accepted.

The conference room accommodates about 120 seats and is fully equipped for hosting presentations. Audio equipment, PC, projector and remote controls will be provided.

We suggest all authors to present themselves to their session chairperson at least 10 minutes in advance, in order to be instructed about the control panel, microphone and pointer. Furthermore the author will verify that the presentation files are correctly loaded on the computer system, so that the slides will show smoothly.

Best Paper Award

The program committee will select one of the regular conference contributions for the Best Paper Award. The Best Paper will be announced at the end of the conference. The award will be handed out at ICMTS 2018. Furthermore, the last year's Best Paper Award will be handed out to the recipients. The Award was won last year with the paper entitled *Test*

Conference Proceedings

The conference proceedings will be published in paper and on a USB-stick. One copy of the paper proceedings and one USB stick are included in the registration fee. Additional copies will be available at the conference for 50 per copy.

Conference Registration

Registration Fees

Prices are excluding VAT

	Advance*	Regular
Technical Session		
IEEE Member	400	450
Non-Member	450	500
Student	250	275
Short Courses (Advance Registration Only)		
Member/Non-Member	250	250
Student	120	120
Extra Banquet Ticket		
	60	60

*Before February 17th, 2017

On-site Registration (Registration at the conference)

Registration on the conference day is possible at the main desk. Fees will be the same as Regular Registration.

Registration fees include admission to the technical sessions, equipment exhibits, morning and afternoon coffee breaks, the welcome reception, lunch (Monday - tutorial, Tuesday, Wednesday and Thursday - conference), the conference banquet and excursion to Grenoble historical downtown. It also includes one paper copy of the proceedings and one copy on USB-stick.

Payment of Registration Fees

For payment please refer to the "registration information" session on the conference website (<http://icmts2017.insight-outside.fr/>). Onsite, the registration payment can be in cash, by credit card (VISA, MASTERCARD), or non-transferrable check. The confirmation of your IEEE Membership or Student status will be conducted during Registration at the Conference.

Cancellation Policy

Cancellation can only be accepted if a written notice is sent by e-mail or fax to the ICMTS 2017 main office (Fax: +33 438381819, email: ICMTS2017@insight-outside.fr). No fees will be withheld for cancellation prior February 26th. If the cancellation is notified between February 26th and March 13th, a charge of 50% of the total registration fees will be withheld in

order to cover administration and banking costs. After March 13th 2017, no refund will be possible, but a copy of the Proceedings will be delivered after the Conference. All refunds will be processed after the Conference.

Equipment Exhibition

During the conference an equipment exhibition will be held in the main hall of “Maison Minatec”. The exhibition will display equipment and systems closely associated with the design, fabrication, analysis and characterization of test structures. Companies working in related fields present themselves and their products. This exhibition will allow one-to-one discussions between exhibitors and conference attendees on the latest practices and test equipment. For more details see the ICMTS website. The exhibition opening times are given below along with a preliminary list of exhibitors. The full list will be distributed at the conference.

March 27,	8:30-16:50	Tutorials
March 28,	8:30-18:00	Technical Sessions
March 29,	8:30-16:30	Technical Sessions
March 30,	8:30-12:20	Technical Sessions and Close-down

Exhibitors List

- Ascent European Nanoelectronic Access
- Everbeing Int'l Corp.
- Hprobe
- Imina Technologies
- JEM Europe
- Keysight Technologies Inc.
- MB Electronique
- MPICorporation
- Platform Design Automation
- Synergie Concept
- Tektronix

Internet Access

The “Maison Minatec” is covered by a Wi-Fi signal that provides internet access. To connect to the internet, instructions will be provided on site along with network ID and WPA key.

Lunch Service

Lunches and coffee breaks will be served in the main “Maison Minatec” Hall. If you have any particular request concerning food, please specify it during online registration in the “Special Dietary” menu (first page after clicking “Register Now”).

Conference Banquet

Conference banquet will be held on Wednesday the 29th at the restaurant “[Le Téléferique](#)” on top of the “Bastille” that watches over the city of Grenoble. To reach it a cableway ticket will be provided within the registration package.

The [cableway station](#) is on the Quai Stéphane Jay, on the left side of the river Isère. Please consider that the weather on the “Bastille” can be colder than at city level.



A down-up view of the “Bastille” and the cableway



An up-down view from the “Bastille” on the city

Excursion

After the conference a guided tour in the ancient Grenoble will be proposed to all the attendees and accompanying people. The walking tour will start at about 14:00 and will be concluded at around 16:30. The details will be described during the conference. We encourage all the attendees to participate to the tour and to reserve their tickets in advance, in order to allow a better organization.

About Grenoble

How to come here

- **Airports**

Grenoble is served by two airports. The main one is [Lyon Saint-Exupéry \(LYS\)](#). It is connected to Grenoble by bus shuttles. Shuttles leave every hour and the trip takes about one hour (Get off at the final destination: Grenoble Gare Routière). Tickets can be bought on Internet (35€ round-trip) or directly onboard. We encourage you to buy your ticket in advance. For flight connections to and from UK, [Grenoble Isère Airport \(GNB\)](#) is also a possible choice.

- **Highways**

Grenoble can be reached by car using the highways A48, travelling south-bound and the A41, travelling west-bound. Driving in Grenoble however is discouraged since traffic jams are very frequently experienced by car drivers.

- **Train station**

The main train station of Grenoble is only 10 minutes' walk far from the conference site. To buy a train ticket, please surf on the [SNCF website](#). In France trains are classified as high speed

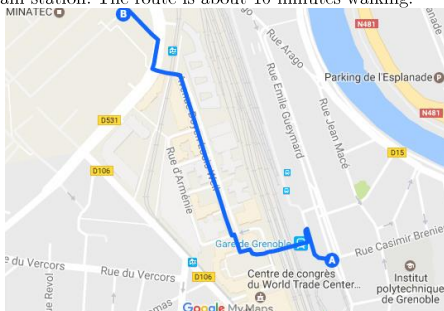
train (TGV) and normal speed trains (TER, for small distances, and InterCity for longer distances). A TGV links Grenoble to Paris in about 3,5 hours.

Climate and temperatures

The weather in March is generally dry but still a bit cold. Maximum temperatures are around 15°C (59°F or 288K) in the average, while the minimum temperatures can still be as low as 4°C (39°F or 277K). Moreover consider that Grenoble can be relatively windy in spring time.

Map

A small city map can be found on the conference website. Here a smaller map is proposed showing how to reach the conference site from the main train station. The route is about 10 minutes walking.



Currency

The official currency in France is the Euro (€). Banks are open from Monday to Friday from 8:30 to 17:00. The actual change rates are 1,04USD and 122,77JPY. ATM can be easily found all over the city.

Electricity and telephone

In France the electricity grid provides 220V at 50Hz frequency. Pugs are E/F and C types. For Italian L type, please note that French plugs don't accept the ground pin between phase and neutral pins.

Accommodation

Grenoble offers a large choice of hotels and hotel residents. A quite rich list of hotels is provided on the conference website under the page "accommodation". For ICMTS a special agreement was set with Accorhotels to provide better offers. Please check them out on the conference website.

In Case of Emergency

The official emergency service in the whole European Community is 112, dialed without prefix.

Safety and Crime

Although Grenoble is a relatively safe city, pickpocketing affects the most crowded places. We thus encourage you to pay attention to your belongings.

Walking at night poses no particular risks, but as in any other city, good sense is always required.

Embassies and consulates

A list of embassies and consulate on the French territory can be found on www.diplomatie.gouv.fr. Please refer to this website to ensure if you need a Visa for your stay.

In Grenoble can be found the consulates of Greece, Algeria and Tunisia.

Sight-seeing in Grenoble

The first references to the city of Grenoble are as old as 43BC. At that time the city was called *Cularo* and was a small gallic village. The Emperor Gratian was so impressed and touched by the people's warm welcome as he was received in the village that he gave it the status of roman city. In honor of this, *Cularo* was renamed *Gratianopolis*. After the French Revolution, the name was changed to Grenoble.

Grenoble has much to offer to tourists both within its small downtown streets and in the gorgeous surrounding mountains. The city is nested within three mountain chains. On the north the Chartreuse looks over Grenoble with the "Bastille" and its hidden monastery. The west side is covered by the Vercors, almost entirely protected as a regional park. The east side is dominated by the Belledonne, particularly appreciated by skiers and hikers.

Biking, hiking, climbing, rafting, canyoning but also gliding, parachuting are all common words in the vocabulary *grenoblois*.

But the city in itself has also a lot to offer. The cable car will provide you a wonderful view of the city before you start losing yourself in the small *rues* of the city center. Several museums (most of them free) will provide hours of cultural pleasure. The Grenoble Museum of Art, the Dauphinois Museum, and the Old Bishop's Palace Museum are just some examples.

If you are interested in seeing where the French Revolution started, you might visit the Vizille Castle and spend some time in the vast garden, where it is not uncommon to encounter wildlife.

Many useful information can be found on the [tourism website](#) (14, rue de la République). A Grenoble Pass can be bought there to visit up to four cultural places with interesting discounts (2 visits 12.50€; 3 visits 16.50€).

Bus tickets can be bought at the bus stops or on board, with a small overprice. For tram tickets, it is necessary to buy them at the tram stops (1 ticket 1.50€, 10 tickets 13.40€).



A view of Place Saint André,
also called *Place du Trib* by the students



A view of Place Grenette



A view of Mont Aiguille, a few km south from Grenoble

TUTORIALS

Tutorials Lecturer Biographies

Jean-Pierre Raskin

Jean-Pierre RASKIN received the Industrial Engineer degree from the Institut Supérieur Industriel d'Arlon, Belgium, in 1993, and the M.S. and Ph.D. degrees in Applied Sciences from the Université catholique de Louvain (UCL), Louvain-la-Neuve, Belgium, in 1994 and 1997, respectively. In 1998, he joined the EECS Department of the University of Michigan, Ann Arbor, USA. In 2000, he joined the Microwave Laboratory of UCL, Louvain-la-Neuve, Belgium, as Associate Professor, and he has been a Full Professor since 2007. Since 2014, he has been the head of the Electrical Engineering department of UCL. His research interests are the modeling, wideband characterization and fabrication of advanced SOI MOSFETs as well as micro and nanofabrication of MEMS / NEMS sensors and actuators, including the extraction of intrinsic material properties at nanometer scale. He is IEEE Fellow, EuMA Associate Member, Société de l'électricité, de l'électronique et des technologies de l'information et de la communication (SEE) Member, and Material Research Society (MRS) Member.

Stewart Smith

Stewart Smith received the B.Eng.(hons) degree in electronics and electrical engineering in 1997 and the Ph.D. degree in 2003 from the University of Edinburgh, Scotland, UK. He is currently a lecturer in the School of Engineering at the University of Edinburgh and a member of the Research Institute for Bioengineering. Stewart is a member of the RSE Young Academy of Scotland and an officer of the Scottish Chapter of the IEEE Electron Devices Society. His current research interests include the design and fabrication of bioelectronic and biomedical microsystems, microfluidics and biosensors, and development of test structures for MEMS and microsystems processes.

Tomasz Brozek

Dr Brozek is a Technical Fellow and Engagement Director at PDF Solutions, San Jose, California.

He earned his M.S. EE degree from Lvov Technical University and Ph.D. degree in Physics from Institute Semiconductors, Ukrainian Academy of Sciences. He worked as Assistant Professor and lead research projects in physics and technology of MOS devices at Warsaw University of Technology, Poland and at University of California, Los Angeles.

Tomasz has been with PDF since 2000 and focused on process characterization, technology integration, yield improvement, and reliability.

He has served as Engagement Manager for several successful PDF yield ramp projects in the past. He has been working on projects with advanced CMOS (down to 20nm node), NVM FLASH, DRAM, MOS Image Sensors.

Before joining PDF Tomasz was with Motorola, working on device characterization, charging damage, process assessment, and reliability support for technology development and transfer of Logic, BiCMOS, and embedded FLASH technologies.

Jean-François Carpentier

Jean-François Carpentier received the Ph.D. degree in electrical engineering in 1994 from the University of Lille (IEMN Laboratory), France, for his thesis on electromagnetic solvers to study interconnections in MMIC. From 1995 to 1997, he was an Assistant Professor, engaged in frequency domain numerical techniques for 3-D electromagnetic simulations. In 1997, he joined STMicroelectronics, Central R&D, Crolles, France. He developed electromagnetic simulations activity for passive components and interconnections for RF, analog, and digital applications on silicon. He became an expert in simulation, modeling and characterization of Si-passive components and interconnections. In 2002, he moved to RF design with MEMS, especially with bulk acoustic wave resonators. He was engaged in research and development on RF circuits and BAW devices for mobile communications. In 2005, he has been with the Passive and RF-MEMS above IC group, and he managed a group on filtering with BAW resonators, including modeling, RF characterization, and filter designs. In 2010, he joined R&D process development group as team manager to develop integration of heterogeneous systems on silicon interposers, with special interest on 60GHz module with beam-forming in WiGiG context to provide Gbit/s data transfer. Since 2012, he was engaged in a new More than Moore activity inside STMicroelectronics relative to photonics. He was in charge of testchips specification, design and characterization to qualify the technology. In 2012, he was graduated of "Habilitation à Diriger des Recherches" at Grenoble INP.

Carlo Cagli

Carlo Cagli received his B.S. and M.S. degrees in Physics in 2005 and 2007 from the University of Milan, Italy. He received the PhD degree in 2011 from the Polytechnic of Milan, Italy. During this period he spent several months at the Lawrence Berkeley National Laboratory (LBNL) in Berkeley to work at the Molecular Foundry Facility. He focused on RRAM electrical characterization. Since 2011 he is with CEA-Leti in Grenoble focusing on the advanced characterization of emerging non-volatile memories.

Sorin Cristoloveanu

Sorin Cristoloveanu received the PhD (1976) in Electronics and the French Doctorat ès-Sciences in Physics (1981) from Grenoble Polytechnic Institute, France. He is currently Director of Research CNRS. He also worked at JPL (Pasadena), Motorola (Phoenix), and the Universities of Maryland, Florida, Vanderbilt, Western Australia, and Kyungpook (World Class University project). He served as the director of the LPCS Laboratory and the Center for Advanced Projects in Microelectronics, initial seed of Minatoc center. He authored more than 1,100 technical journal papers and communications at international conferences (including 160 invited contributions). He is the author or the editor of 28 books, and he has organized 25 international conferences. His expertise is in the area of the electrical characterization and modeling of semiconductor materials and devices, with special interest for silicon-on-insulator structures. He has supervised more than 80 PhD completions. He has received the IEEE Grove Award (2017) and the Electronics Division Award of the Electrochemical Society (2002). He is a Fellow of IEEE, a Fellow of the Electrochemical Society, and Editor of Solid-State Electronics.

Tutorial Program

Monday 27th March

Where: Maison Minatec, salle Titane

08:30 Registration

08:50 Tutorials Opening

Gilles Reimbold, Tutorial Chair

09:00 Characterization of analog performances (RF, noise...) of advanced CMOS technologies

Jean-Pierre Raskin, Université Catholique de Louvain, Belgium

Performance of RF integrated circuit (IC) is directly linked to the analog and high frequency characteristics of the transistors, the quality of the back-end of line process as well as the electromagnetic properties of the substrate. This last decade Silicon-on-Insulator (SOI) MOSFET technology has demonstrated its potentialities for high frequency commercial applications pushing the limits of CMOS technology. Thanks to the introduction of the trap-rich high-resistivity SOI substrate on the market, the ICs requirements in term of linearity for RF switches, for instance, are fulfilled. Today partially depleted SOI MOSFET is the mainstream technology for RF SOI systems. Future generations of mobile communication systems will require transistors with better high frequency performance at lower power consumption. The advanced MOS transistors in competition are FinFET and Ultra Thin Body and Buried oxide (UTBB) SOI MOSFETs. The use of specific RF test structures at the early stage of a technological node development is of first importance to analyze the transistor parasitic resistances and capacitances, the transistor cutoff frequencies, the self-heating, and the substrate coupling and non-linear behavior. The relative impact of the transistor and the passive elements and interconnections on the small- and large-signal RF performance of SOI RF switches and power amplifier will be presented.

10:00 Coffee Break

10:20 MEMS Test

Stewart Smith, University of Edinburgh, Scotland, UK

Micro Electro Mechanical Systems (MEMS) technology provides new functionality to CMOS electronics, extending the technology roadmap in a "More than Moore" direction. Key examples are the common mechanical force sensors (MEMS accelerometers or gyroscopes) found in many mobile technologies. Other microsystems technologies include electro-chemical sensors and electro-optical systems. For the successful integration of MEMS technologies with CMOS, process engineers must be capable of extracting key parameters such as sacrificial layer etching speed and mechanical properties to reliably produce the devices. This tutorial will review reported test structures and test methods for MEMS process and systems.

11:20 Device and Process Variability

Tomasz Brozek, PDF Solutions, USA

Keeping Moore's Law alive requires continuous scaling of both geometrical dimensions and operating voltage.

Device and process variability are usually main limiters of scaling, and serious challenge in advanced technology generations. They impact the yield of Integrated circuits, both Parametric and Functional components. The Tutorial will discuss the sources of variability, their decomposition, and characterization. In addition to transistor variability, the impact of process variability on FEOL, MOL, and BEOL modules will be covered. Finally, characterization approaches, and examples will be provided.

12:20 Lunch

14:00 Test for silicon photonics

Jean-François Carpentier, STMicroelectronics, France

The topic of Optical Wafer Sorting and Platform Qualification from foundry point of view represents a new era since wafer-scale optical testers are not as mature as electrical testers and the optimum testing strategy for silicon photonics has still to be written, especially in the 3D approach developed by STMicroelectronics at data rate of 25Gb/s. The tutorial will cover various aspects as device, function and complex circuits from static (ex.: loss) and dynamic (ex.: eye diagram) point of views.

15:00 Coffee Break

15:20 Test & Characterization of RRAM memories

Carlo Cagli, CEA-LETI, France

Resistive memories, generally called RRAM, are emerging non-volatile memory devices that are attracting much attention as potential next generation memory devices. RRAM stock the logic information in the resistive level of the active material. The characterization of this kind of device poses several challenges. The memory stack is indeed very sensitive to the applied potentials (within a few tens of mV) and the device performances varies greatly with them. The control of the current discharge, during the writing stage is a key point to prevent premature device failure. In addition, most emerging memories have a bipolar nature which calls for dedicated setup. Endurance assessment can also be challenging due to the large number of required cycles ($>10^{11}$).

In this tutorial a description of the main aspects of RRAM characterization will be discussed from single cell test to large array.

16:20 Test structures and methods for FDSOI characterization

Sorin Cristoloveanu, CNRS-IMEP, France

From now on, the MOS transistor will operate in fully-depleted (FD) mode. Electrostatic considerations request sub-10 nm thick body in at least one direction, vertical or lateral. A second gate and an oxide underneath the body are clear assets for back-biasing schemes and dielectric isolation. A straightforward solution is the planar FDSOI technology that cumulates ultrathin body, thin buried oxide (BOX) and short high-K/metal gates. Nanosize SOI materials and devices feature two oxides, three interfaces and two possible channels, more or less overlapped. This complexity cannot be addressed with conventional characterization methods developed for bulk-Si devices. We review test structures and pragmatic techniques appropriate for ultrathin FDSOI technology. The pseudo-MOSFET

method is unrivalled for the evaluation of SOI-like materials. Selected examples will illustrate the properties of recent SOI materials (UTBB, GeOI, sSOI, etc). We argue that the gated PIN diode is a powerful tool to access the properties of electron and hole channels simultaneously without suffering from parasitic floating-body and transient effects. Typical MOSFETs can be used not only for conventional extraction of carrier mobility and lifetime, oxide and interface defects but also for sophisticated characterization (current transients, noise, geometrical magnetoresistance revealing size-quantization effects, etc.). Finally, we present customized MOS structures especially conceived for the evaluation of less usual scaling-related mechanisms (supercoupling effect, parasitic bipolar transistor, floating-body effects).

WELCOME RECEPTION

Monday, March 27th

Location: Salle Titane

18:00-19:30 Welcome Reception

We would like to invite you to a welcome reception at the Maison Minatec to introduce you at the conference and to let you enjoy with all attendees some good wine and tasty food.

TECHNICAL PROGRAM

Tuesday 28th March

Where: Maison Minatec, salle Titane

08:00—17:00 Registration

08:50 Conference Opening

Alain Toffoli and Gérard Ghibaudo, General Chairmen

Hans Tuinhout, Technical Program Chairman

SESSION 1: Novel Test Structures

09:10—10:30

Co-Chairs: Gerard Ghibaudo *IMEP-LAHC MINATEC, Grenoble, France*
Stewart Smith, *University of Edinburgh, Scotland, UK*

9:10

1.1 — Characterization and monitoring structures for robustness against cyclic thermomechanical stress: design and influence of Ti-Al(Cu) layer scheme

A. Mann, H. Lohmeyer and Y. Joseph

Robert Bosch GmbH, Automotive Electronics, Reutlingen, Germany

For the qualification of different backend stack options in an early phase of technology development and for process control purposes, we developed a wafer-level test approach based on dedicated test structures sensitive to repetitive-powerpulsing stress. End-of-life trials indicate a strong dependence of the mean lifetime on the lower metal finger configuration and the used Ti-Al(Cu) layer scheme.

9:30

1.2 — Test structures for studying flexible interconnect supported by carbon nanotube scaffolds

D. Jiang, S. Sun, M. Edwards, J. Liu, and K. Jeppson

Department of Microelectronics and Nanoscience Electronic Materials and Systems Laboratory Gothenburg, Sweden

Due to their flexibility and compatibility with silicon devices, the use carbon nanotubes as scaffolds for metal interconnect in flexible and

wearable electronics has been proposed. This paper examines the performance of dual-height carbon nanotubes as flexible scaffolds for horizontal and vertical interconnect. For this purpose a number of test structures has been designed and fabricated and their electrical and mechanical performance is investigated.

9:50

1.3 — Dealing with Leakage Current in TLM and CTLM Structures with Vertical Junction Isolation

S. Bystrova¹, S.M. Smits¹, J. Klootwijk², R. A. M. Wolters¹, A.Y. Kovalgin¹, L. K. Nanver¹ and J. Schmitz¹

¹MESA+ Institute for Nanotechnology, University of Twente, Enschede, Netherlands; ²Philips Research, Eindhoven, Netherlands

Circular Transfer Length Method (CTLM) structures are often employed to extract contact resistivity towards a doped semiconductor region. In this article we treat the situation where the doped region is junction-isolated from the substrate. The junction isolation may be leaky resulting in erroneous parameter extraction. This paper demonstrates by exemplary measurement results on industrial solar cell samples that using a proper methodology reliable contact resistivity values can be obtained on junction isolated CTLM structures.

10:10

1.4 — Electrical test structures for verifying continuity of ultra-thin insulating and conducting films

S. Banerjee, R. van der Velde, M. Yang, J. Schmitz and A. Y. Kovalgin
MESA+ Institute for Nanotechnology, University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands

In this work, electrical characterization on insulating aluminum nitride (AlN) and conducting tungsten (W) films was performed using dedicated test structures, to determine the thickness at which the films reached continuity. A discontinuous-to-continuous transformation of AlN layer (occurring below 11 nm) caused a transition from Ohmic to non-Ohmic conduction. For similar transformation of the W layer (occurring at approximately 2 nm), the reverse transition was observed.

10:30-11:00 Coffee Break

SESSION 2: Novel Materials Characterization

11:00—12:20

Co-Chairs: Alexey Kovalgin, *University of Twente, The Netherlands*
Anthony Walton, *University of Edinburgh, Scotland, UK*

11:00

2.1 — Detailed characterization and critical discussion of series resistance in graphene-metal contacts

S. Venica, F. Driussi, P. Palestri, L. Selmi, A. Gahoi* , V. Passi* , M. C. Lemme*

DPIA, Università degli Studi di Udine, Via delle Scienze 208, Udine, Italy; *University of Siegen, Siegen, Germany

The contact-end resistance method is applied to TLM measurements to characterize the graphene-metal contact resistance. The experiments show that the commonly used transmission line model fails to describe the graphene-metal contact under specific biasing. This is due to the additional resistance of the junction induced in graphene near the contact.

11:20

2.2 — The outstanding properties of Graphene-Insulator-Semiconductor (GIS) test structures for photoelectric determination of semiconductor devices band diagram

K. Piskorski¹, V. Passi², J. Ruhkopf², M. C. Lemme², H. M. Przewlocki¹

¹Institute of Electron Technology, Warsaw; ²University of Siegen, Germany

This paper shows results of the photoelectric measurements of the band alignment at the Si-SiO₂ interface of the graphene gated capacitors. Graphene-insulator-semiconductor (GIS) structures, due to low absorption of the graphene layer, are excellent tools for characterization of barrier heights at the semiconductor-insulator interface. Very sensitive and accurate measurements were carried out allowing to determine the barrier heights for photoemission of electrons ($E_b = 4.34 \pm 0.01$ eV) and holes ($E_b = 4.70 \pm 0.03$ eV) from the semiconductor substrate into the insulator.

11:40

2.3 — Electromechanical testing of ZnO thin films under high uniaxial strain

R. Tuyaerts^{1,2}, J.-P. Raskin¹, J. Proost²

¹Institute of Information and Communication Technologies, Electronics and Applied Mathematics, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium; ²Institute of Mechanics, Materials and Civil Engineering Université catholique de Louvain, 1348, Louvain-la-Neuve, Belgium

Thanks to an innovative design, stress-strain curves of released thin films can be obtained, up to the fracture of the material, using internal stress present in a second material. This technique has also been used to make electrical resistivity measurement under deformation and will be extended to perform Hall measurements.

12:00

2.4 — Test Structures for Understanding the Impact of Ultra-High Vacuum Metal Deposition on Top-Gate MoS₂ Field-Effect-Transistors

P. Bolshacov¹, P. Zhao, C. Smyth¹, A. Azcatl¹, P. Hurley², R. Wallace¹, and C. Young¹

¹The University of Texas at Dallas, Richardson, TX 75080, USA; ²Tyndall Micronano Electronics, University of College Cork, Cork, Ireland

Greek crosses and TLM test structures were fabricated and characterized along with top-gate field effect transistors. We also show the usefulness

and adaptation of a single TLM structure into multiple bottom-gate FETs that allow for extraction of contact resistance and typical device parameters for direct correlation on the same TMD flake enabling very little variability that can occur “flak to flake”. Sheet resistance and contact resistance were successfully extracted and improvement in device performance was demonstrated with C-V and I-V measurements.

12:20—13:30 Lunch

SESSION 3: Variability Characterization

13:30—14:30

Co-Chairs: Christopher Hess, *PDF Solutions Inc, USA*
Brad Smith, *NXP Semiconductors, USA*

13:30

3.1 — Statistical Characterization and Modeling of Drain Current Local and Global Variability in 14nm bulk FinFETs

T.A. Karatsori^{1,2}, C.G. Theodorou¹, R. Lavieville¹, T. Chiarella³, J. Mitard³, N. Horiguchi³, C. A. Dimitriadis², G. Ghibaudo¹

¹IMEP-LAHC, Univ. Grenoble Alpes, Minatec, 38016 Grenoble, France;

²Department of Physics, Aristotle University of Thessaloniki, Greece;

³IMEC, Kapeldreef 75, 3001 Leuven, Belgium.

A detailed statistical characterization and modeling of drain current local and global variability in 14nm Si bulk FinFET devices is performed. To this end, an analytical mismatch model covering weak to strong inversion region is used to extract the main matching parameters. Our results show that, despite their very aggressive dimensions in terms of Fin width and height, such devices exhibit excellent local and global variability performance.

13:50

3.2 — Measurement of mismatch factor and noise of SRAM PUF using small bias voltage

Z. Cui, B. Zheng, Y. Piao, S. Liu, R. Xie and H. Shinohara

Graduate School of Information, Production and Systems, Waseda University.

Distributions of mismatch factor and noise factor of PUF are measured using 256 bit SRAM PUF test structure with bias voltage inputs. By combining shifted bias voltages and repeat evaluation, it is confirmed with measurement data that both noise and whole 256 bit mismatch factor follow Gaussian distribution.

14:10

3.3 — V_{th}-shiftable SRAM Cell TEGs for Direct Measurement for the Immunity of the Threshold Voltage Variability

S. Yamaguchi, H. Imi, S. Tokumaru, T. Kondo, H. Yamamoto, K. Nakamura

Center for Microelectronic Systems, Kyushu Institute of Technology

In order to demonstrate the immunity of the 12-transistor ratio-less SRAM operation for the variability of the threshold voltage (V_{th}) of MOSFETs by the measurement, we developed the V_{th} -shiftable SRAM cell TEGs (VTSTs). The measured results are discussed by the fail condition maps (FCMs) and the maximum limit of V_{th} -shift for stable SRAM operation.

14:30

3.4 — Ring-oscillator test-structures for sub-0.1% accuracy wafer-level characterization of active- and standby current consumption, variability, and fast aging of oscillation frequencies

M. Vertregt, H. Tuinhout, N. Wils, A. Zegers, and J. Croon
NXP Semiconductors

This paper presents the layout and characterization results of a set of 44 wafer-level probed ring oscillator test structures each using a 6-probe pad module. This approach allows extremely accurate wafer level characterization, which proves valuable for model verification and silicon-based performance/leakage trade-offs of multiple inverter dimensions under varying supply, back-bias, and temperature conditions.

14:50-15:05 Coffee Break

SESSION Exhibitions

15:05—18:00

Chairs: Antoine Cros & Hans Tuinhout

15:05-15:55 Exhibitors presentations

15:55

Invited Paper — Challenges of contemporary and future parametric testing, *Part 1*

B. Verzi

Keysight Technologies

16:20 Coffee Break and Exhibitions

16:40

Invited Paper — Challenges of contemporary and future parametric testing, *Part 2*

B. Verzi

Keysight Technologies

17:05 Exhibitions

18:00 End of Day 1

Wednesday 29th March

Where: Maison Minatec, salle Titane

09:00—17:00 Registration

SESSION 4: Device Modeling

09:00—10:20

Co-Chairs: Kjell Jeppson, *Chalmers University of Technology, Sweden*
Yoshio Mita, *The University of Tokyo, Japan*

9:00

4.1 — Systematic evaluation of the split-CV based parameter extraction methodologies for 28nm FDSOI

K. Pradeep^{1,3}, G. Gouget¹, T. Poiroux², P. Scheer¹, A. Juge¹, G. Ghibaudo³

¹STMicroelectronics, Crolles Site, 850 rue Jean Monnet, 38926 Crolles, France; ²CEA-Leti, MINATEC Campus, 38054 Grenoble Cedex 9, France; ³IMEP-LAHC, MINATEC Campus, 3 Parvis Louis Néel, 38016 Grenoble, Cedex 1, France

In this work, robust methodologies for parameter extraction using split-CV measurements in FDSOI structures are developed. These methods enable an automated and robust extraction procedure which is very important from an industrial perspective. The accuracy and robustness of the improved methods are verified using statistical measurements carried out on 28nm FDSOI devices and comparison with physical characterization.

9:20

4.2 — True Kelvin Test Structure to achieve Accurate and Repeatable DC Wafer-Level Measurements for Device Modelling Applications

C. B. Sia

Cascade Microtech Inc. (A FormFactor Company)

6-pad True Kelvin Test Structure for advanced CMOS devices is proposed in this work. It allows test engineers to make very accurate and repeatable wafer-level measurements required for SPICE modelling applications. This design helps to overcome parasitic resistances of the probe holder and probe which change with temperatures, mitigates the oxidation of exposed underlying copper on the pads due to repeated probing on the same test pads at elevated temperatures and more importantly, minimizes the frequency of probe tip cleaning required to get accurate and repeatable measurements.

9:40

4.3 — Impact of access resistance on New Y function methodology for MOSFET parameter extraction in advanced FD-SOI technology

J.-B. Henry^{1,2}, A. Cros², Q. Raffhay¹, G. Ghibaudo¹, J. Rosa²

¹STMicroelectronics, Crolles Site, TR&D/STD/TPS/SiRel 850 rue Jean Monnet, 38926 Crolles, France; ²IMEP-LAHC, MINATEC Campus, 3 Parvis Louis Néel, 38016 Grenoble, Cedex 1, France.

In this work, an upgraded version of the so called New Y function MOSFET parameter extraction methodology is proposed [1], taking the impact of access resistance into account. This new approach is applied on STMicroelectronics 28 nm FD-SOI MOS technology to show the consequences of neglecting access resistance on the value of extracted parameters.

10:00

4.4 — Input Capacitance Determination of Power MOSFETs from Switching Trajectories

K. Oishi, M. Shintani, M. Hiramoto, and T. Sato

Graduate School of Informatics, Kyoto University, Japan

A novel method for determining input capacitance of power MOSFETs is proposed. Through the measurements of gate charge transfer trajectories during switching, gate-source capacitance and drain-gate capacitance are determined. The capacitances obtained by the proposed method simulate switching behaviors of the MOSFET much more accurately than the conventional ones obtained by the small signal measurement

10:20—11:00 Coffee Break

SESSION 5: RF and HV Device Characterization

11:00—12:20

Co-Chairs: Luca Selmi, *University of Udine, Italy*

Christopher Hess, *PDF Solutions Inc, USA*

11:00

5.1 — A 130 to 170 GHz Integrated Noise Source based on Avalanche Silicon Schottky Diode in BiCMOS 55 nm for In-Situ noise characterization

J. C. A. Goncalves^{1,2}, T. Quemerais³, D. Gloria², G. Avenier², S. Lepilliet¹, G. Ducournau¹, C. Gaquière¹ and F. Danneville¹

¹IEMN, UMR CNRS 8520, Avenue Poincaré – CS 60069, 59652 Villeneuve-d'Ascq, France; ²STMicroelectronics, 850 rue Jean Monnet, 38920 Crolles, France ³STMicroelectronics, 12 rue Jules Horowitz, 38000 Grenoble, France

In this paper, dedicated silicon (Si) Schottky diodes, designed to be used as noise source are presented. To this aim, test structures have been designed and characterized, leading to Schottky diodes featuring an avalanche breakdown voltage close to (-6) V. Biased around the breakdown voltage while its anode grounded, the diode shows an adjustable Excess Noise Ratio (ENR) which ranges between 4 dB to 20 dB in D-band. Hence, because of its ability to be integrated within Si process, this noise source allows high frequency in-situ noise characterization in advanced Si CMOS or BiCMOS technologies dedicated to millimeter-wave applications.

11:20

5.2 — Design of a Broadband CMOS RF Power Amplifier to establish device-circuit aging correlations

E. Barajas¹, D. Mateo¹, X. Aragones¹, A. Crespo-Yepes², R. Rodriguez², J. Martin-Martinez², M. Nafria²

¹Dept. Enginyeria Electrònica, Universitat Politècnica de Catalunya (UPC), Edifici C4, 08034, Barcelona, Spain; ²Dept. Enginyeria Electrònica, Universitat Autònoma de Barcelona (UAB), Edifici Q, 08193 Bellaterra, Barcelona, Spain

This paper presents the design of a Broadband CMOS RF Power Amplifier in order to be stressed at circuit level but with the possibility to be measured both at circuit and at device level. It allows establishing a relation between the degradation of circuit's RF performances and those of its individual devices parameters. The test structure, measurement set-up and procedure are described in detail.

11:40

5.3 — DC and RF characterization of RF MOSFET embedding structure

A. Takeshige, K. Katayama, S. Amakawa, K. Takano, T. Yoshida, and M. Fujishima

Graduate School of Advanced Sciences of Matter, Hiroshima University

It is not so easy to correlate DC Kelvin measurement data of an RF transistor and its non-Kelvin RF measurement data, because the actual bias voltages in the latter are not known precisely. Knowing the bias voltages requires accurate characterization of its embedding structure. This paper reports on an attempt at correlating DC and RF measurements of parasitic resistances associated with a MOSFET test structure, including a transmission line, on a CMOS chip.

12:00

5.4 — High voltage MOSFETs integration on advanced CMOS technology: characterization of thick gate oxides incorporating High K Metal Gate stack from logic core process

D. Morillon^{1,3}, F. Julien¹, J. Coignus², A. Toffol², L. Welter¹, C. Jahan², J.-P. Reynard¹, E. Richard¹, P. Masson³

¹STMicroelectronics, France; ²CEA LETI, Minatec Campus, Grenoble, France; ³EpOC / Nice Sophia-Antipolis University, Biot, France

This paper presents the performance evaluation of high voltage MOS gate stacks integrated in an aggressive digital core platform, thus including High K Metal Gate (HKMG) stack. Physical, electrical, and reliability characterizations are performed on capacitors in order to evaluate the impact of HKMG integration on the MOS structures.

12:20—13:30 Lunch

SESSION 6: Array Testing and Mapping

13:30—14:50

Co-Chairs: Satoshi Habu, *Keysight Technologies, Japan*

13:30 Introduction and invitation to ICMTS 2018

13:50

6.1 — An arrayed test structure for transistor damage assessment induced by circuit analysis and repairing processes with back-side-accessing Focused Ion Beam

N. Usami¹, J. Kinoshita², R. Ikeno³, Y. Okamoto¹, M. Tanno², K. Asada³ and Y. Mita¹

¹Department of Electrical Engineering and Information Systems (EEIS), the University of Tokyo; ²Van Partners, Toyota Tsusho Electronics Corporation; ³VLSI Design and Education Center (VDEC), the University of Tokyo

We propose an arrayed test structure to assess the damages of metal-oxide-semiconductor field-effect transistors (MOSFETs) exposed under back-side LSI processes, such as by Focused Ion Beam (FIB). Back-side process with FIB is becoming essential to analyze and repair modern LSI chips, to avoid processing through many metal layers with dense wiring and dummy patterns. To access transistors from back-side, however, FET active region must be cropped out and that may cause damage to transistor characteristics. Our test structure consists of 2-D-arrayed MOSFETs. The impact by the back-side process on various conditions can be visualized as I-V characteristics change. Several FIB back-side processes were applied to the proposed test structure and corresponding change of MOSFET characteristics were measured.

14:10

6.2 — A new test vehicle for RRAM array characterization

C. Nguyen, C. Cagli, L. Kadura, J-F. Nodin, S. Bernasconi, G. Reimbold
CEA-Leti, MINATEC Campus, 38054 Grenoble Cedex 9, France

This paper presents a test vehicle to characterize Resistive memories (RRAM) arrays. The structure of the array, the decoders, and the selectors are explained as well as the electrical setup that drives the arrays decoders and performs the electrical characterization. Eventually some electrical results are presented and discussed.

14:30

6.3 — Development of an Advanced System for Automated 200mm Wafer Mapping of Stress Using Test Structures

S. Lokhandwala, J. Murray, S. Smith, A.R. Mount[†], J.G. Terry, A.J. Walton

Institute for Integrated Micro and Nano Systems (part of the Joint Research Institute for Integrated Systems), School of Engineering, Scottish Microelectronics Centre, The University of Edinburgh, Edinburgh, EH9 3FF, UK; [†]School of Chemistry, Joseph Black Building, The University of Edinburgh, EH9 3JJ, UK

Controlling and understanding the stress in materials is of major importance in the successful fabrication of MEMS devices. Failure to properly account for the effects of stress can lead to substrate warping

and layer delamination, both of which are detrimental to the performance and reliability of components. Hence, it is desirable to have reliable and automated technology to spatially monitor both stress and strain on silicon wafers. This paper reports in detail an integrated measurement system that has been specifically designed to semi-automatically wafer map stress, strain and Young's modulus. The measurement system is designed to automatically determine the rotation of a test structure from which strain can be extracted. This is then combined with a customized nanoindenter extracting Young's modulus and these two measurements from the same location are used to calculate the spatial stress in the film.

14:50—15:10 Coffee Break

SESSION 7: Sensor Test Structures

15:10—16:30

Co-Chairs: Johan Klootwijk, *Philips Research, The Netherlands*
Bill Verzi, *Keysight Technologies, USA*

15:10

7.1 — A Test Structure to Characterize Transparent Electrode Array Platform with TFTs for Bio-Chemical Applications

A. Tixier-Mita^{1,2}, S. Ihida², G. Cathcart¹, F. A. Shaik¹, H. Fujita, Y. Mita³, H. Toshiyoshi^{1,2}

¹RCAST, The University of Tokyo; ²IIS, The University of Tokyo, Japan;
³Dept. of Elec. Eng. and Info. Sys., The University of Tokyo, Japan

A test structure to characterize impedance of Transparent Electrode Array Platform with Transparent Thin-Film-Transistors for Bio-Chemical Applications is proposed. The structure is a post-processed electrode that connects source terminals of multiple TFTs. This characterization is essential to determine the limits, in terms of sensitivity and operation frequency, of impedance measurements with these devices for biological cells applications.

15:30

7.2 — Test Structures for the Characterization of Sensor Packaging Technology

E. O. Blair, A. Buchoux, A. Tsiamis, C. Dunare, J. R. K. Marland, J. G. Terry, S. Smith, and A. J. Walton.

The University of Edinburgh The Kings Buildings, Alexander Crum Brown Road Edinburgh, EH9 3FF Scotland, UK

This paper reports test structures for characterizing sensor packaging materials for liquid environments. These enable the evaluation of: 1) successful removal of packaging material on the sensing areas, 2) the permeability of the material to its operating environment, 3) electrical connection of the bond wires, and 4) the ingress of the liquid environment between the packaging material and the chip surface. The use of these structures is then demonstrated in the evaluation of a UV curable resin as an example.

15:50

7.3 — Test structures for optimizing polymer electrolyte performance in a microfabricated electrochemical oxygen sensor

J. R. K. Marland*, C. Dunare*, A. Tsiamis†, E. González-Fernández#, E. O. Blair*, S. Smith†, J. G. Terry*, A. F. Murray†, A. J. Walton*

*Institute for Integrated Micro and Nano Systems; †Institute for Bioengineering School of Engineering, The University of Edinburgh, UK;

#School of Chemistry, The University of Edinburgh, Scotland, UK

Test structures were fabricated for optimizing the design and fabrication of a solid polymer electrolyte in an electrochemical oxygen sensor. Measurements showed that the adhesion and durability of the polymer structure were affected by its geometry as well as the underlying material. Test electrodes covered by the polymer were effective at supporting electrochemical oxygen detection.

16:10

7.4 — Test Structures for Stepwise Deformation Sensing on Super-flexible Strain Sensors

C. Wang^a, B. B. Xu^a, J.G. Terry^b, S. Smith^b, A.J. Walton^b, Y. Li^{a*}

^aSmart Materials and Surfaces Lab, Faculty of Engineering and Environment, Northumbria University, Newcastle upon Tyne, NE1 8ST, UK; ^bSMC, Institute for Integrated Micro and Nano Systems School of Engineering, The University of Edinburgh, Edinburgh, EH9 3FF, UK

Super-flexible sensors functioning with a strain changing range of up to 0.6 can be enabled by surface creasing. In this paper test structures are developed to exploit the sensing mechanism of structural electrodes. The growth and co-existence of wrinkles and creases on electrodes are characterized with a lateral strain range of 0.3 to 0.543. Further investigation will focus on characterizing the mechano-responsive electrical switching mechanism of the test structures.

18:30—23:00 Gala Dinner at «Le Téléférique»

Thursday 30th March

Where: Maison Minatec, salle Titane

SESSION 8: Low Frequency Noise Characterization

9:00—10:20

Co-Chairs: Antoine Cros, *STMicroelectronics, France*

Colin McAndrew, *NXP Semiconductors*

9:00

8.1 — A Statistical Modeling Methodology of RTN Gate Size Dependency Based on Skewed Ring Oscillators

A. K. M. Mahfuzul Islam¹, T. Nakai², and H. Onodera^{1,2}

¹Department of Informatics and Electronics Institute of Industrial Science, The University of Tokyo 4-6-1 Meguro-ku, Tokyo, Japan;

²Department of Communications and Computer Engineering Graduate School of Informatics, Kyoto University Sakyo-ku, Kyoto, Japan

With technology scaling, RTN induced delay variation has become a concern. Therefore, optimization of gate sizing considering RTN is required especially at low voltage operation, where the delay becomes highly sensitive to transistor noise. In this paper, we focus on RTN modeling of gate size dependency. We propose a test structure of ring oscillator (RO) array with different skewed inverters to characterize gate size dependency. We propose a statistical analysis flow to decouple the RTN effects of downsized and upsized transistors from skewed inverter based delay distribution. The proposed methodology successfully models RTN gate size dependency for nMOSFET and pMOSFET simultaneously. The estimated delay distributions based on the constructed RTN model matches well with the measured distributions for ROs with different gate sizes.

9:20

8.2 — A variability-based analysis technique revealing physical mechanisms of MOSFET low-frequency noise

T. H. Both^{1,2}, J. A. Croon¹, M. Banaszkeski da Silva², H. P. Tuinhout¹, A. Zegers-van Duijnhoven¹, A. J. Scholten¹, G. I. Wirth²

¹NXP Semiconductors, ²Universidade Federal do Rio Grande do Sul

This paper presents a technique for statistical analysis of MOSFET low-frequency noise (LFN) based on the autocorrelation of numerous LFN power spectral density (PSD) spectra. This correlation analysis reveals information about physical mechanisms behind 1/f noise that is difficult to obtain otherwise. The methodology also enables quantification and validation of old and new statistical LFN models.

9:40

8.3 — Statistical Low-Frequency Noise Characterization in sub-15nm Si/SiGe Nanowire Trigate pMOSFETs

C. G. Theodorou¹, R. Lavieville¹, T.A. Karatsori^{1,2}, S. Barraud³, C.A. Dimitriadis², G. Ghibaudo¹

¹IMEP-LAHC, Univ. Grenoble Alpes, Minatec, 38016 Grenoble, France;

²Department of Physics, Aristotle University of Thessaloniki, Greece;

³CEA-LETI, Univ. Grenoble Alpes, Minatec, 38054 Grenoble, France.

A detailed statistical characterization of the drain current low-frequency noise (LFN) in sub 15nm Si/SiGe Trigate NW pMOSFETs is presented. The slow oxide trap density and distribution, as well as the correlated mobility fluctuations effect are probed for several channel geometries. The LFN variability scaling is also presented and compared to established nano-scale planar CMOS technologies. Our results indicate that such devices demonstrate relatively good noise variability levels, despite their very aggressive dimensions and not yet optimized fabrication process.

10:00

8.4 — Variability of Low Frequency Noise and Mismatch in Enclosed-Gate and Standard nMOSFETs

M. Bucher¹, A. Nikolaou¹, N. Mavredakis¹, N. Makris¹, M. Coustans², J. Lolivier³, P. Habas³, A. Acovic³, R. Meyer³

¹Technical University of Crete, 73100 Chania, Greece; ²Ecole Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland; ³EM Microelectronic-Marin SA, 2074 Marin, Switzerland

Variability of Low Frequency Noise (LFN) and Random Telegraph Noise (RTN) is an important concern for many analog CMOS integrated circuits. In this paper, transistors with enclosed gate layout are examined and compared with standard layout transistors, with particular emphasis on weak inversion region. Enclosed gate transistors show an improved gate voltage mismatch in weak inversion. A compact MOSFET model for LFN and its variability, based on number fluctuation theory, is shown to cover well the behavior of either type of transistors. Lower levels of noise as well as lower variability of noise are observed in enclosed gate transistors.

SESSION 9: Novel Device Architecture Characterization

11:00—12:20

Co-Chairs: Chadwin Young, *The University of Texas, USA*
Carlo Cagli, *CEA-Leti, France*

11:00

9.1 — A microsecond time resolved current collapse test setup dedicated to GaN based Schottky diode characterization

T. Lorin^a, W. Van Den Daele^a, C. Gillot^a, M. Charles^a, J.Biscarrat^a, M. Plissonnier^a, G. Ghibaudo^b, G. Reimbold^a

^aCEA, LETI, MINATEC Campus, F-38054 Grenoble, France; ^bIMEP-LAHC, Université Grenoble Alpes, Minattec/INPG, 38016 Grenoble, France

This paper presents a test set up to characterize current collapse effects in power diodes such as GaN-based Schottky junctions. The set up principle and its main components are described. Recording of current transients very shortly (2 μ s on wafer prober) after reverse to forward switching are shown and the related trapping effect are analyzed through temperature dependent measurements.

11:20

9.2 — Novel C-V measurements based method for the extraction of GaN buffer layer residual doping level in HEMT

I. Nifa¹, C. Leroux¹, A. Torres¹, M. Charles¹, and G. Reimbold¹, G. Ghibaudo² and E. Bano²

¹CEA, LETI, Minattec Campus, 17 rue des Martyrs, F-38054 Grenoble cedex, France ; ²IMEP-LAHC, MINATEC/INPG, 3 Parvis Louis Néel, 38016 Grenoble, France.

This paper presents a new methodology to characterize the GaN buffer doping level which is a critical parameter for epitaxial fabrication of GaN wafers. As demonstrated in this study, its characterization is challenging due to parasitic effects. New configuration Capacitance-Voltage (C-V)

measurements are carried out on a Metal Insulator Semiconductor (MIS) structure with a gate on Al₂O₃ dielectric. The experimental study is validated with a self-consistent Poisson-Schrodinger (PS) simulation.

11:40

9.3 — Test structure configurations for analysis of Field Effect influenced self-heating and thermal coupling in High Voltage SiGe HBTs

B. Ó hAinle, E. Coyne and B. Lane
Analog Devices

This paper presents several test structure configurations that facilitate a comprehensive assessment of self-heating and thermal coupling effects in High Voltage SiGe HBTs in a DTI on SOI process. Several layout test structures are investigated including variations in device separations, multi-device arrays and the influence of the substrate contact in the regions outside the trench isolation, and indeed the potential for trench field effects themselves, the latter two both due to the high voltages involved. The findings are reported with a view to focus on a Compact Modelling solution implementable in a commercial CAD tool.

12:00

9.4 — Test structures for nano-gap fabrication process development for nano-electromechanical systems

S. Smith^{1,3}, Y. Takeshiro⁴, Y. Okamoto⁴, J.G. Terry², A.J. Walton², R. Ikeno³, K. Asada³, and Y. Mita⁴

¹Institute for Bioengineering; ²Institute for Integrated Micro and Nano Systems School of Engineering, The University of Edinburgh, UK ³VLSI Design and Education Centre, the University of Tokyo, Japan ⁴Department of Electrical Engineering and Information Systems, the University of Tokyo, Japan

Nanometre scale pores, gaps or trenches are of significant interest for a number of applications in nano and microsystems. This paper presents the design of test structure chips for the development of a process for the fabrication of controllable nanoscale trenches or gaps using standard microfabrication processes. Initial results from the test structures show the capability of the process.

12:20 **Best Paper Announcement**
12:40 **Lunch and conference closure**
14:00 **Excursion**

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Anthony J. Walton	University of Edinburgh	UK
Larg Weiland	PDF Solutions Inc.	USA
Greg Yeric	ARM	USA
Chadwin Young	University of Texas	USA

ICMTS 2017 CONDENSED PROGRAM

Monday, March 27 th	
08:30	Registration
08:50	Tutorials opening
09:00	Characterization of analog performances of advanced CMOS
10:00	Coffee Break
10:20	MEMS Test
11:20	Variability – Static and dynamic aspects
12:20	Lunch
13:30	Tests for Silicon Photonics
14:30	Coffee Break
14:50	Characterization of RRAM devices
15:50	FDSOI Characterization
16:50	End of Tutorials
18:00	Welcome Reception

Tuesday, March 28 th	
08:30	Registration
09:00	Conference Opening
09:10	Session 1: Novel Test Structures
10:30	Coffee Break
11:00	Session 2: Novel Materials Char.
12:20	Lunch
13:30	Session 3: Variability Char.
14:50	Coffee Break
15:05	Session Exhibitions
18:00	End of Day 1

Wednesday, March 29 th	
08:30	Registration
09:00	Session 4: Device Modeling
10:20	Coffee Break
11:00	Session 5: RF and HV Device Char.
12:20	Lunch
13:30	Session 6: Array Testing and mapp.
14:50	Coffee Break
15:10	Session 7: Sensor test Structures
16:30	End of Sessions
18:30	Dinner Gala

Thursday, March 30 th	
08:30	Registration
09:00	Session 8: LF Noise Characterization
10:20	Coffee Break
11:00	Session 9: Novel Device Arch. Char.
12:20	Best Paper, Lunch and conference closure
14:00	Excursion