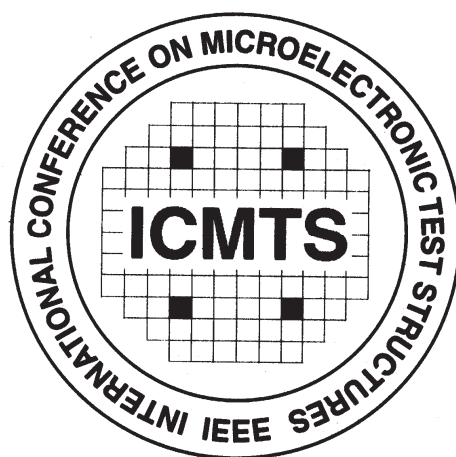


2016 International Conference on Microelectronic Test Structures



29th IEEE ICMTS Conference Proceedings

March 28-31

Mielparque Yokohama, Japan

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CHAIRMAN'S LETTER

Dear Colleagues,

The 29th IEEE International Conference on Microelectronic Test Structures (ICMTS 2016) will be held in Yokohama, Japan, on March 28-31. Test structures are indispensable for the development, design and production of any microelectronic circuits, devices and processes. Since 1988, ICMTS has provided a forum for designers and users of test structures in all areas of microelectronics, to discuss recent developments and future directions. This year, the conference consists of about 40 oral presentations in ten sessions. As usual, it will be preceded by a one-day tutorial short course. There will also be an equipment exhibition related to test structure measurements. The conference is technically co-sponsored by the IEEE Electron Devices Society.

This is the first time the conference is held in the port city Yokohama. The conference venue, Mielparque Yokohama, is comfortably located just in front of a seaside park within an old town area. It is also very close (only two minutes walk) to a subway station, from which convenient access to the airports, as well as nearby locations including central Tokyo is provided. Since Yokohama is a major tourist destination, you can find abundant shops, restaurants and other tourist attractions around.

I look forward to your participation in ICMTS 2016!

Sincerely,

Kiyoshi Takeuchi
General Chairman

SESSION 1: MEMS and Sensors

2016 March 29, 9:00 – 10: 20

Co-Chairs: Stewart Smith, *The University of Edinburgh, UK*

- 9:00 An Efficient Method to Evaluate 4 million Micro-bump Interconnection Resistances for**
1.1 3D Stacked 16-Mpixel Image Sensor 2
Yoshiaki Takemoto, Hideki Kato, Toru Kondo, Naohiro Takazawa, Mitsuhiro Tsukimura, Haruhisa Saito, Kenji Kobayashi, Jun Aoki, Shunsuke Suzuki, Yuichi Gomi, Seisuke Matsuda, and Yoshitaka Tadaki, *Olympus Corporation, Japan*
- 9:20 An End-point Visualization Test Structure for All Plasma Dry Release of Deep-RIE**
1.2 MEMS 6
Yuki Okamoto, Eric Lebrasseur, Isao Mori, and Yoshio Mita,
The University of Tokyo, Japan
- 9:40 Spring-constant measurement methods for RF-MEMS capacitive switches** 10
1.3 Jiahui Wang, Jeroen Bielen, Cora Salm, and Jurriaan Schmitz,
University of Twente, The Netherlands
- 10:00 Microfabricated test structures for thermal resonant gas sensor** 16
1.4 Matthieu Denoual¹, M. Pouliquen¹, Julien Grand¹, Hussein Awala¹, Sveltana Mintova¹, O. de Sagazan², Shu Inoue³, Agnes Tixier-Mita³, Yoshio Mita³, and D. Robbes¹
¹*ENSICAEN, University of Caen, France*, ²*The University of Rennes, France*,
³*The University of Tokyo, Japan*

SESSION 2: Thermal Issues

2016 Mar 29, 11:00 – 12:20

Co-Chairs: Anthony J. Walton, *University of Edinburgh, UK*

Hi-Deok Lee, *Chungnam National University, Korea*

- 11:00 A Test Structure for Analysis of Metal Wire Effect on Temperature Distribution in**
2.1 Stacked IC 22
Toshihiro Matsuda¹, Haruka Demachi¹, Hideyuki Iwata¹, Tomoyuki Hatakeyama¹, and Takashi Ohzone²,
¹*Toyama Prefectural University, Japan*, ²*Dawn Enterprise, Japan*
- 11:20 Dedicated test-structures for investigation of the thermal impact of the BEOL in**
2.2 advanced SiGe HBTs in time and frequency domain 28
Rosario D'Esposito¹, Sebastien Fregonese¹, Anjan Chakravorty², and Thomas Zimmer¹,
¹*University of Bordeaux, France*, ²*IIT Madras, India*
- 11:40 Hotspot test structures for evaluating carbon nanotube microfin coolers and**
2.3 graphene-like heat spreaders..... 32
Kjell Jeppson¹, Jie Bao², Shirong Huang², Yong Zhang², Shuangxi Sun², Yifeng Fu², and Johan Liu², ¹*Chalmers University, Sweden*, ²*Shanghai University, China*

12:00	Transistor Self-Heating Correction and Thermal Conductance Extraction using Only DC Data	38
	Colin C. McAndrew ¹ , Alexandra Lorenzo-Cassagnes ¹ , and Olin L. Hartin ² , ¹ <i>NXP Semiconductors, AZ, USA</i> , ² <i>Arizona State University, AZ, USA</i>	

SESSION 3: Arrayed Test Structures

2016 Mar 29, 14:10 – 15:40

Co-Chairs: Tatsuya Ohguro, *Toshiba, Japan*
 Christopher Hess, *PDF Solutions, USA*

14:10	[Invited] Random Telegraph Noise Measurement and Analysis based on Arrayed Test Circuit toward High S/N CMOS Image Sensors	46
3.1	Rihito Kuroda, Akinobu Teramoto, and Shigetoshi Sugawa, <i>Tohoku University, Japan</i>	
14:40	Proposal of a New Array Structure to Enable the Detection of Soft Failure and the Aging Test with Overcurrent of Resistive Element	52
3.2	Shingo Sato and Yasuhisa Omura, <i>Kansai University, Japan</i> ,	
15:00	Advanced Ioff Measureable MOSFET Array with Eliminating Leakage Current of Peripheral Circuits	58
3.3	Tsuyoshi Suzuki, Shigetaka Mori, Hidetoshi Oishi, Masaaki Bairo, Manabu Tomita, Kazuhisa Ogawa, Yuzo Fukuzaki, and Hidetoshi Ohnuma, <i>Sony Corporation, Japan</i>	
15:20	Design and use of an array-based test structure to characterize mechanical stress effects caused by WLCSP solder bumps	62
3.4	Hans Tuinhout and Rob van Dalen, <i>NXP Semiconductors, The Netherlands</i>	

SESSION 4: Parameter Extraction

2016 Mar 29 16:10 – 17:10

Co-Chairs: Kjell Jeppson, *Chalmers University, Sweden*

16:10	New access resistance extraction methodology for 14nm FD-SOI technology	70
4.1	Jean-Baptiste Henry ¹ , Antoine Cros ¹ , Quentin Rafhay ² , Gerard Ghibaudo ² , and Julien Rosa ¹ , ¹ <i>STMicroelectronics, France</i> , ² <i>IMEP-LAHC, France</i> ,	
16:30	Test Structures for CMOS RF Reliability Assessment	76
4.2	Leonhard HeiB ^{1,2} , Andreas Lachmann ² , Reiner Schwab ² , Georgos Panagopoulos ² , Peter Baumgartner ² , Mamatha Yakkegondi Virupakshappa ² , and Doris Schmitt-Landsiedel ^{1,2} , ¹ <i>Technical University of Munich, Germany</i> , ² <i>Intel Deutschland GmbH, Germany</i> ,	
16:50	Statistical Analysis and Modeling of Random Telegraph Noise Based on Gate Delay Variation Measurement	82
4.3	A.K.M. Mahfuzul Islam, Tatsuya Nakai, and Hidetoshi Onodera, <i>Kyoto University, Japan</i>	

SESSION 5: RF and Power Devices

2016 Mar 30 9:20 – 10:20

Co-Chairs: Colin McAndrew, *NXP Semiconductors, USA*

9:20	A High Power Curve Tracer for Characterizing Full Operational Range of SiC Power	
5.1	Transistors	90
	Yohei Nakamura, Michihiro Shintani, Takashi Sato, and Takashi Hikihara, <i>Kyoto University, Japan</i>	
9:40	A Test Structure Set for on-wafer 3D-TRL calibration	96
5.2	Manuel Potéreau, Arnaud Curutchet, Rosario D’Esposito, Magali De Matos, Sebastien Fregonese, and Thomas Zimmer, <i>University of Bordeaux, France</i>	
10:00	Test Structures of LASCOR Device for RF ESD Protection in Nanoscale CMOS Process	
5.3	100
	Chun-Yu Lin and Rong-Kun Chang, <i>National Taiwan Normal University, Taiwan</i>	

SESSION 6: Capacitances

2016 Mar 30 10:50 – 11:50

Co-Chairs: Hans P. Tuinhout, *NXP Semiconductor, The Netherlands*
Chadwin Young, *University of Texas at Dallas, USA*

10:50	Highly Effective and Versatile Test Structure for Evaluating Dielectric Properties using	
6.1	Flexible Pulse Generator on Chip	106
	Shigetaka Mori, Ken Sawada, Manabu Tomita, Kazuhisa Ogawa, Tsuyoshi Suzuki, Hidetoshi Oishi, Masaaki Bairo, Yuzo Fukuzaki, and Hidetoshi Ohnuma, <i>Sony Corporation, Japan</i>	
11:10	Extraction of Floating-Gate Capacitive Parameters in Split-Gate Flash Memory Cells	
6.2	110
	Yuri Tkachev, <i>Silicon Storage Technology, Inc., CA, USA</i>	
11:30	Demonstration of MOS Capacitor Measurement for Wafer Manufacturing using a	
6.3	Direct Charge Measurement	116
	Kenichi Takano ¹ , Masaharu Goto ¹ , Ernesto Shiling ² , Arthur Gasasira ³ , and Jiun-Hsin Liao ³ , <i>Keysight Technologies, ¹Japan, ²CA, USA, ³GLOBALFOUNDRIES, NY, USA</i>	

SESSION 7: Memories

2016 Mar 30 13:40 – 14:40

Co-Chairs: Yuzo Fukuzaki, *Sony Corporation, Japan*
Carlo Cagli, *CEA/LETI, France*

- 13:40 Test circuits to characterize setup/hold/access times, minimum voltage and maximum frequency of operation for memory compilers** 122
7.1 Nitin Dhamija, Gaurav Lalani, Mike Nelson, Joe Brown, Henning Spruth, and Puneet Sharma, *Freescale Semiconductor, India*
- 14:00 A New Write Stability Metric Using Extended Write Butterfly Curve for Yield Estimation in SRAM Cells at Low Supply Voltage** 126
7.2 Hao Qiu, Kiyoshi Takeuchi, Tomoko Mizutani, Takuya Saraya, Masaharu Kobayashi, and Toshiro Hiramoto, *The University of Tokyo, Japan*
- 14:20 Measurement of SRAM Power-On State for PUF Applications Using an Addressable SRAM Cell Array Test Structure** 130
7.3 Kiyoshi Takeuchi, Tomoko Mizutani, Hirofumi Shinohara, Takuya Saraya, Masaharu Kobayashi, and Toshiro Hiramoto, *The University of Tokyo, Japan*

SESSION 8: Non-Volatile Memories

2016 Mar 30 15:30 – 17:00

Co-Chairs: Jurriaan Schmitz, *University of Twente, The Netherlands*
Satoshi Habu, *Keysight Technologies, Japan*

- 15:30 [Invited] New power-gating architectures using nonvolatile retention: Comparative study of nonvolatile power-gating (NVPG) and normally-off architectures for SRAM** 136
8.1 Yusuke Shuto, Shuu'ichirou Yamamoto, and Satoshi Sugahara, *Tokyo Institute of Technology, Japan*
- 16:00 Challenges of Modeling the Split-Gate SuperFlash® Memory Cell with 1.1V Select Transistor** 142
8.2 M. Tadayoni¹, S. Martinie², O. Rozeau², S. Hariharan¹, C. Raynaud², and N. Do¹,
¹*Silicon Storage Technology, Inc., CA, USA*, ²*CEA-LETI, France*
- 16:20 Ultra-small and Ultra-reliable Innovative Fuses Scalable from 0.35µm to 28nm** 148
8.3 Shine Chung, Wen-Kuan Fang, YC Hsu, JY Hsiao, Lupin Lin, and Wen-Hua Yu, *Attopsemi Technology Corporation, Taiwan*
- 16:40 Impact of a Laser Pulse On HfO₂-based RRAM Cells Reliability and Integrity** 152
8.4 A. Krakovinsky^{1,2}, M. Bocquet², R. Wacquez¹, J. Coignus¹, D. Deleruyelle², C. Djaou², G. Reimbold¹, and J-M. Portal², ¹*CEA-LETI, France*, ²*Aix-Marseille University, France*

SESSION 9: Process and Device Characterization

2016 Mar 31 9:00 – 10:20

Co-Chairs: Larg Weiland, *PDF Solutions, USA*

Bing-Yue Tsui, *National Chiao Tung University, Taiwan*

- 9:00 Test Structures to support the Development and Process Verification of Microelectrodes
9.1 for High Temperature Operation in Molten Salts** 158
E.O. Blair, D.K. Corrigan, I. Schmueser, J.G. Terry, S. Smith, A.R. Mount, and A.J. Walton,
The University of Edinburgh, UK
- 9:20 Interface Trap Density Estimation in FinFETs from the Subthreshold Current** 164
9.2 J. Schmitz, B. Kaleli, P. Kuipers, N. van den Berg, S.M. Smits, and R.J.E. Hueting,
University of Twente, The Netherlands
- 9:40 Novel Test Structure for Evaluating Dynamic Dopant Activation after Ion Implantation
9.3** 168
Jung-Ruey Tsai¹, Ruey-Dar Chang², Cheng-Hui Chou², Hsueh-Chun Liao², Sz-Kai Huang^{1,2},
Sung-Hung Lin^{1,2}, and Jui-Chang Lin^{1,2},
¹*Asia University, Taiwan*, ²*Chang Gung University, Taiwan*
- 10:00 Top-Gated MoS₂ Capacitors and Transistors with High-k Dielectrics for Interface Study
9.4** 172
Peng Zhao¹, A. Azcatl¹, P. Bolshakov-Barrett¹, P.K. Hurley², R.M. Wallace¹, and C.D. Young¹,
¹*The University of Texas at Dallas*, ²*University of College Cork, Ireland*

SESSION 10: Materials Characterization

2016 Mar 31 10:50 – 12:10

Co-Chairs: Bill Verzi, *Agilent Technologies, USA*

- 10:50 Chip level characterisation studies of Ni and NiFe electrochemical deposition using test
10.1 structures** 178
J. Murray, R. Perry, J.G. Terry, S. Smith, A.R. Mount, and A.J. Walton,
The University of Edinburgh, UK
- 11:10 Test Structures for the Characterisation of Conductive Carbon Produced from
10.2 Photoresist** 184
S. Scarfi, S. Smith, A. Tabasnikov, I. Schmueser, E. Blair, A.S. Bunting, A.J. Walton,
A.F. Murray and J.G. Terry, *The University of Edinburgh, UK*
- 11:30 Comparing Current Flows in Ultrashallow pn- / Schottky-like Diodes with 2-Diode Test
10.3 Method** 190
X. Liu and L.K. Nanver, *University of Twente, The Netherlands*
- 11:50 A Reliable Schottky Barrier Height Extraction Procedure** 196
10.4 Bing-Yue Tsui and Fu-Tze Yu, *National Chiao-Tung University*

AUTHORS INDEX

Aoki, J.	2	Gogo, M.	116	Liu, J.	32
Awala, H.	16	Gomi, Y.	2	Liu, X.	192
Azcat, A.	176	Grand, J.	16	Lorenzo-Cassagnes, A.	38
Bairo, M.	58, 106	Hariharan, S.	142	Mahfuzul Islam, A.K.M.	83
Bao, J.	32	Hartin, O. L.	38	Martinie, S.	142
Baumgartner, P.	76	Hatakeyama, T.	22	de Matos, M.	96
van den Berg, N.	164	Heiß, L.	76	Matsuda, S.	2
Bielen, J.	10	Henry, J.-B.	70	Matsuda, T.	22
Blair, E. O.	158, 186	Hikihara, T.	90	McAndrew, C. C.	38
Bocquet, M.	152	Hiramoto, T.	126, 130	Mintova, S.	16
Bolshakov-Barrett, P.	176	Hsiao, J.-Y.	148	Mita, Y.	6, 16
Brown, J.	122	Hsu, Y.-C.	148	Mizutani, T.	126, 130
Bunting, A. S.	186	Huang, S.	32	Mori, I.	6
Chakravorty, A.	28	Huang, S.-K.	170	Mori, S.	58, 106
Chang, R.-D.	170	Huetting, R. J. E.	164	Mount, A. R.	158, 180
Chang, R.-K.	100	Hurley, P. K.	176	Murray, A. F.	186
Chou, C.-H.	170	Inoue, S.	16	Murray, J.	180
Chung, S.	148	Iwata, H.	22	Nakai, T.	83
Coignus, J.	152	Jeppson, K.	32	Nakamura, Y.	90
Corrigan, D. K.	158	Kaleli, B.	164	Nanver, L. K.	192
Cros, A.	70	Kato, H.	2	Nelson, M.	122
Curutchet, A.	96	Kobayashi, K.	2	Ogawa, K.	58, 106
van Dalen, R.	62	Kobayashi, M.	126, 130	Ohnuma, H.	58, 106
Deleruyelle, D.	152	Kondo, T.	2	Ohzone, T.	22
Demachi, H.	22	Krakovinsky, A.	152	Oishi, H.	58, 106
Denoual, M.	16	Kuipers, P.	164	Okamoto, Y.	6
D'Esposito, R.	28, 96	Kuroda, R.	46	Omura, Y.	52
Dhamija, N.	122	Lachmann, A.	76	Onodera, H.	83
Djaou, C.	152	Lalani, G.	122	Panagopoulos, G.	76
Do, N.	142	Lebrasseur, E.	6	Perry, R.	180
Fang, W.-K.	148	Liao, H.-C.	170	Poliquen, M.	16
Fregonese, S.	28, 96	Liao, J.-H.	116	Portal, J.-M.	152
Fu, Y.	32	Lin, C.-Y.	100	Potéreau, M.	96
Fukuzaki, Y.	58, 106	Lin, J.-C.	170	Qiu, H.	126
Gasasira, A.	116	Lin, L.	148	Rafhay, Q.	70
Ghibaudo, G.	70	Lin, S.-H.	170	Raynaud, C.	142

Reibold, G.	152	Teramoto, A.	46
Robbes, D.	16	Terry, J. G.	158, 180, 186
Rosa, J.	70	Tixier-Mita, A.	16
Rozeau, O.	142	Tkachev, Y.	110
de Sagazan, O.	16	Tomita, M.	58, 106
Saito, H.	2	Tsai, J.-R.	170
Salm, C.	10	Tsui, B.-Y.	198
Saraya, T.	126, 130	Tsukimura, M.	2
Sato, S.	52	Tuinhout, H. P.	62
Sato, T.	90	Virupakshappa, M. Y.	76
Sawada, K.	106	Wacquez, R.	152
Scarfì, S.	186	Wallace, R. M.	176
Schmitt-Landsiedel, D.	76	Walton, A. J.	158, 180, 186
Schmitz, J.	10, 164	Wang, J.	10
Schmueser, I.	158, 186	Yamamoto, S.	136
Schwab, R.	76	Young, C. D.	176
Sharma, P.	122	Yu, F.-T.	198
Shiling, E.	116	Yu, W.-H.	148
Shinohara, H.	130	Zhang, Y.	32
Shintani, M.	90	Zhao, P.	176
Shuto, Y.	136	Zimmer, T.	28, 96
Smith, S.	158, 180, 186		
Smits, S. M.	164		
Spruth, H.	122		
Sugahara, S.	136		
Sugawa, S.	46		
Sun, S.	32		
Suzuki, S.	2		
Suzuki, T.	58, 106		
Tabasnikov, A.	186		
Tadaki, Y.	2		
Tadayoni, M.	142		
Takano, K.	116		
Takazawa, N.	2		
Takemoto, Y.	2		
Takeuchi, K.	126, 130		

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† Loren Linholm passed away on 18 January 2016.

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