27th ICMTS

2014 IEEE International Conference on Microelectronic Test Structures

March 24–27, 2014
Palazzo Antonini Cernazai
Via Prospero Antonini
Udine, Italy

Technically sponsored by:
The IEEE Electron Devices Society

Contents

WELCOME LETTER

Dear Colleagues,

the 27th International Conference on Microelectronic Test Structures will be held in Udine (Italy) at Palazzo Antonini Cernazai, via Prospero Antonini, Udine. This year it is organized by the Università degli Studi di Udine. It is technically co–sponsored by the IEEE Electron Devices Society. The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The conference will be held on March 25–27, 2011, and will be preceded by a one–day Tutorial Short Course on microelectronic test structures on March 24.

The first ICMTS was held in Long Beach in 1988, and since then the conference has cycled between Europe, North America, and Asia. It will be the second time that ICMTS is held in Italy and for the first time in Udine. As in previous editions there will also be a related equipment exhibition focused on test structure measurements and related companies.

Venue of the Conference is the Sala Gusmani of Palazzo Antonini Cernazai, conveniently situated within walking distance of the Train Station, in the heart of the Udine historical center. Hotels, restaurants and tourist attractions are abundantly found in the near vicinity. Palazzo Antonini Cernazai itself is one of the historical buildings owned by the Università degli Studi di Udine and it is the seat of the humanistic pole of the University. It was built by the noble family of Antonini and it has been erected in the year 1595.

An attractive social programme is offered to the conference delegates and accompanying persons. This includes a Welcome Reception on Monday, a short excursion at the Tiepolo Galleries in Palazzo Arcivescovile and the Conference Banquet on Wednesday, and, on Thursday, an excursion to Villa Manin, one of the most important artistic monuments in Friuli Venezia Giulia.

We hope to welcome you in Udine in March!

Sincerely

Luca Selmi, General Chairman
Johan Klootwijk, Technical Program Chair
Gaudenzio Meneghesso, Tutorial Chair
Alain Toffoli, Exhibition Chair
Francesco Driussi, Local Arrangements Chair

GENERAL INFORMATION

Conference Information

The 2014 International Conference on Microelectronic Test Structures is organized by the Università degli Studi di Udine and it is technically co–sponsored by the IEEE Electron Devices Society. The purpose is to bring together designers and users of test structures to discuss recent developments and future directions of research on test structures or enabled by test structures. The Conference will be preceded by a one–day Tutorial Short Course covering a variety of technical areas related to Microelectronic Test Structures.

The Tutorials and the Technical sessions will all be held at the Sala Gusmani in Palazzo Antonini Cernazai. The address is: via Prospero Antonini, Udine.

Website and Email Contacts

ICMTS Website:
http://icmts2014.uniud.it
General Contact:
icmts2014@gmail.com

Presentations

The official language of the conference is English. The ICMTS considers both oral and poster presentations to be of equal value and importance to the conference. The time allowed for oral presentations is 15 minutes plus 5 minutes for discussion. All those authors who have been selected for poster presentation should be prepared to make a 3 minute oral presentation describing their research. There will be no questions after the presentation as these will be followed by an opportunity to discuss the work with the author at their poster. It is suggested these talks should be limited to three slides. We welcome three Invited Speakers to the conference this year: Prof. Kazuo Terada (Hiroshima State University), Dr. Greg Yeric (ARM) and Prof. Mark A. Reed (Yale University). The Invited Speakers are allocated 35 minutes plus 5 minutes for questions.

Sala Gusmani,
venue of the Tutorial and Technical Program

The conference hall offers up to 130 seats and all required facilities including PC, beamer, and audio equipment. All presentations will be uploaded on the Conference PC before the start of the conference, to allow a smooth transition between consecutive presentations. Hence, all presentation materials should be sent to icmts2014@gmail.com before March the 17th 2014. Adobe PDF and PowerPoint (.ppt and .pptx) formats are accepted. In addition, all presenters are requested to bring the original files as backup. All speakers are requested to report to their session chairperson 10 minutes before the session begins. They can then familiarize themselves with the control panel, and ensure that their presentation files are correctly loaded on the computer system well before the session starts.

Best Paper Award

The program committee will select one of the regular conference contributions for the Best Paper Award. The Best Paper will be announced at the end of the conference. The award will be handed out at ICMTS 2015. Furthermore, the last year's Best Paper Award will be handed out to the recipients. The Award was won last year with the paper entitled "Tr Variance Evaluation induced by Probing Pressure and its Stress Extraction Methodology in 28nm High-K and Metal Gate Process" authored by T. Okagaki and coworkers.

Conference Proceedings

The conference proceedings will be published in paper and on a USB–stick. One copy of the paper proceedings and one USB stick are included in the registration fee. Additional copies will be available at the conference for 50€ per copy.

Conference Registration

Registration Fees

Early Registration (Before Febrary 15st, 2014)

	Member*	Non Member	Student**
Tutorial	120€	140€	80€/100€
Technical Sessions	320€	350€	180€/210€

Late Registration (After Febrary 15st, 2014)

	Member*	Non Member	Student**
Tutorial	140€	160€	100€/120€
Technical Sessions	350€	400€	210€/260€

On-site Registration (Registration at the conference)
On–site registration goes at the Late Registration.

* Must be a member of the IEEE

** Lower prices for student members of IEEE

Registration fees include admission to the technical sessions, equipment exhibits, morning and afternoon coffee breaks, the welcome reception, lunch (Monday – tutorial, Tuesday, Wednesday and Thursday – conference), the conference banquet and excursion to Villa Manin. It also includes one paper copy of the proceedings and a USB stick.

Payment of Registration Fees

For payment, please follow the information reported in the Conference Website: http://icmts2014.uniud.it/2014/index.html . Onsite, the registration payment can be in cash, by credit card (VISA, MASTERCARD), or non–transferrable check to "Dip. di Ing. Elettrica Gestionale e Meccanica (DIEGM), Univ. di Udine". The confirmation of your IEEE Membership or Student status will be conducted during Registration at the Conference.

Cancellation

Cancellation can only be accepted if a written notice is sent by e-mail or fax to the ICMTS 2014 Secretariat (Fax: +39 0432 558251, email: patrik.osgnach@uniud.it). A charge of 20% of the total registration fees will be withheld in order to cover administration and banking costs. After March 10th 2014, no refund will be possible, but a copy of the Proceedings will be delivered after the Conference. All refunds will be processed after the Conference.

Equipment Exhibition

During the conference an equipment exhibition will be held in Sala del Pianoforte, Palazzo Caiselli. The exhibition will display equipment and systems closely associated with the design, fabrication, analysis and characterisation of test structures. Companies working in related fields present themselves and their products. This exhibition will permit one–to–one discussions between exhibitors and conference attendees on the latest practices and test equipment. For more details see the ICMTS website. The exhibition opening times are given below along with a preliminary list of exhibitors. The full list will be distributed at the conference.

March 24	8:50–17:20	Set up – Tutorial
March 25, 26	8:50–17:20	Conference
March 27	9:00–12:40	Conference and Close-down

Exhibitors List (at time of press)

- Agilent Technologies
- Accretech
- JEM Europe
- Keithley
- Tokyo Electron Limited

Messages

If you need to be contacted during the Conference Sessions, a message can be left at the registration desk between the hours of 9:00am and 5:00pm, March 24-26, and from 9:00am to 12 noon on March 27. Messages will be placed on a Message Board beside the registration desk.

Messages can be posted for attendees by emailing Ms. Chiara Macuz (chiara.macuz@uniud.it).

Internet access

The conference area is equipped with WiFi internet. The WiFi access will be guaranteed to all academic delegates through the eduroam net. If requested, credentials to access the WiFi will be provided to non academic delegates. Instructions for WiFi connection can be found at http://ainf.uniud.it/fileadmin/istruzioni/wi-fi/Istruzioni_WindowsXPeVista/convegni/WiFi-Cisco-EN.pdf.

Lunch Venue

During ICMTS the tutorial and conference lunches will be served at the Sala del Pianoforte of Palazzo Caiselli, just two minutes walk from Palazzo Antonini Cernazai. Palazzo Caiselli is situated in Vicolo Florio (2 in blue in the ICMTS Google map).

Conference Banquet

The conference banquet will be held in the Casa della Contadinanza, on the top of the Udine Castle hill.

Casa della Contadinanza, outside

Night view of the Udine Castle square

The conference registration fees include one banquet ticket. Guest tickets are available in the accompanying person package.

Excursion

The excursion to Villa Manin will take place Thursday afternoon after lunch, between 14:30 and 18:00 approximately. It is recommended to reserve for the excursion in order to allow the organization to arrange all details. Transfer to Villa Manin in Passariano will be by bus.

Details of the excursion will be announced at the conference, where registration will take place.

Udine Information

Getting there

- **Travelling by plane**
  Udine is served mainly by three international airports, Venezia, Treviso and Trieste. Connections to/from Udine are served by bus (Trieste and Venezia airports) and by train (Venezia and Treviso airports).
- **Travelling by car**
  Udine is located along Highway A23 which connects Austria with major highway A4 travelling est to west of Italy. More informations on Autostrade per l'Italia SpA. To plan a travel to Udine by car, you might refer to ViaMichelin website www.viamichelin.it.
- **Travelling by train**
  Udine Train Station is located 200 meters from the city center. City busses stop in front of the station. Taxis are available at the station too. Udine is connected by train with all major Italian cities. Schedules and prices available at Italian Railway website http://www.trenitalia.com. When browsing the website make sure to select the "tutti i treni" - "all trains" option . Then, insert the stations and dates, click the search button and then click the "all solutions" option at the center bottom of the page. Otherwise only a very limited set of high speed trains will be displayed.

The venue is within 15 minutes walking from Udine's Train Station. All conference hotels are within walking distance. For more information on traveling to Udine and on public transport in Udine, check http://icmts2014.uniud.it/2014/logistics.html.

Map

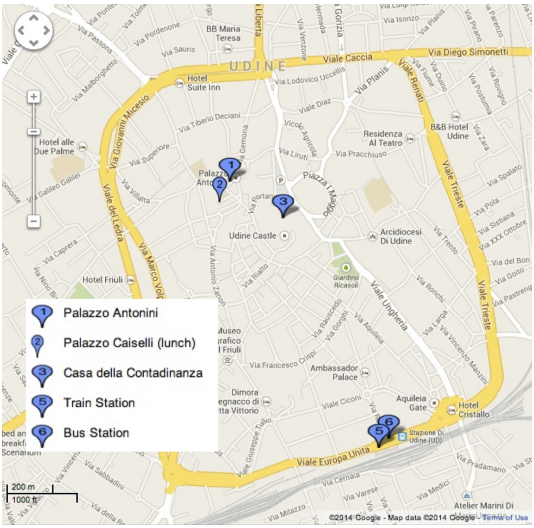
A city map with the important locations for ICMTS 2014 (including a large list of hotel and restaurants) can be found at http://icmts2014.uniud.it/2014/logistics.html

Climate

The Udine weather in late March may be quite variable. In this period, the daily maximum temperature is around 15 °C.

Accommodation

Udine offers a large number of hotels and guest houses covering a wide range of prices and standards. A list of hotels in Udine with special agreements for discounted rates with the University of Udine can be found at http://icmts2014.uniud.it/2014/hotel_bb.pdf. A



limited amount of rooms at reduced price are available for students at the Residenza Universitaria Delle Grazie and at the CISM (www.cism.it). For more details please check http://icmts2014.uniud.it/2014/logistics.html

Currency

The official currency in Italy is the Euro (€). Banks normally open on weekdays between 9:00am until 1:00 pm and between 2:30 pm until 4:30 pm. ATMs are available throughout the city.

Electricity and telephone

The Italian electricity net is 230 V/50 Hz and uses the L type plug. The cellular phone network is GSM 900/1800. All mobile operators support GPRS and UMTS service.

National Emergency numbers

For emergencies, Police, fire brigade, ambulance: tel.: 112.

Safety and crime

Udine is considered as a safe city. Violent crimes are very rare. Also pickpocketing is not usual.

Embassies and consulates

Italian embassies and consulates abroad and foreign embassies and consulates in Italy can be found at www.esteri.it.

Whether a prospective visitor requires a visa depends on his nationality and how long he intends to stay in Italy.

Sight-seeing Udine

Udine, the Regional capital of Friuli, and its surroundings, have a lot to offer to visitors: its friendly squares, Tiepolo masterpieces and traditional osterias, the Roman cities of Aquileia and Cividale del Friuli, the lagoon of Grado, the Alps and the Collio vineyards. Because of its mixed geography, Region Friuli Venezia Giulia has both popular coastal destinations in the summer and mountain ski resorts in the winter, as well as year-round opportunities to enjoy this impressive scenery.

According to the legend, the hill where the Castle of Udine stands was built with the ground transported by Attila's soldiers in their helmets, in order to create a rise from which their chief could see the city of Aquileia burning after his devastating pass. Highlights to visit in the city are: Torre dell'Orologio, The Cathedral, The medieval Castle and Santa Maria in Castello, Oratorio della Puritá, Loggia del Lionello, the Tiepolo Galleries in the Archbishop Palace, San Francesco Church and Piazza delle Erbe. All are within walking distance in the town center.

You can explore Udine and its surroundings on foot, by bike, car, coach and train. Information is available at Udine Infopoint, Piazza I Maggio, 7, Tel. +39 0432 295972, info.udine@turismo.fvg.it, www.facebook.com/udine.turismo. For more information about the city's history and current activities, check the following websites: http://www.turismofvg.it/Home (in English, German and Italian) and http://www.udine20.it (in Italian).

The FVG Card is a chip card displaying the owner's name. You can buy it on–line (www.turismofvg.it/Special-offers/FVG-Card). From the date of first use, it is valid for 48 hours (15 euros), 72 hours (20 euros) or 7 days (29 euros), and it gives you free entry to any attraction or transportation it covers, as well as special discounts in theatres, theme parks, cultural events and spas.

Piazza Libertà, Udine historical centre.

TUTORIALS

Tutorial Lecturer Biographies

Stewart Smith

Stewart Smith received the B. Eng. (hons) degree in Electronics and Electrical Engineering in 1997 and the Ph.D. degree in 2003 from the University of Edinburgh, Scotland, UK. He has published papers at every ICMTS conference from 1999 onwards and received the best paper award at ICMTS 2004 (Awaji, Japan). Stewart is a Lecturer in Electronics with the School of Engineering at the University of Edinburgh. His research interests include the design and fabrication of biological and medical microsystems, integration of novel technologies with CMOS and test structures for microsystem fabrication processes. He was recently appointed to the Royal Society of Edinburgh, Young Academy of Scotland and is an irregular contributor to the YAS blog http://researchtheheadlines.org.

Benno Ankele

Benno Ankele received the M. SC degree in applied physics from the University of Technology in Graz (Austria) in 1986. He started his professional career as a university researcher on organic semiconductors at the IFP in Graz before he joined AMS in Unterpremstätten (Austria) as an IC design engineer. In 1994 he became process characterization manager of AMS. In 1998 he joined the circuit design center of Infineon Technologies in Villach (Austria). As a principal engineer and head of the design - technology interface, Benno Ankele is involved in the design for manufacturing (DfM) of mixed analog/digital circuits.

Andrea Lacaita

Andrea Lacaita is professor of Electron Devices and Analog IC design in the School of Engineering at the Politecnico di Milano. He has been actively involved in the development of Single Photon Avalanche Diodes, nowadays adopted as high sensitivity sensors in various applications. In the fields of mainstream microelectronics he has contributed to characterization and modeling of non–volatile memories, both Flash and emerging. Over the past 20 years he has served in technical committees of IEDM, VLSI Symposium, ESSDERC. He has been Department Chair, Member of the Academic Senate and is nowadays member of the Board of the Politecnico Foundation. He is now setting up PoliFAB, a facility for R&D and service, consisting of 450 m^2 cleanrooms.

Andreas Martin

Andreas Martin received his M.Eng.Sc. in Electrical and Electronic Engineering from the Technical University of Darmstadt, Germany, in 1992. After seven years in the silicon technology characterization group of the Tyndall Institute (former NMRC), Cork, Ireland he started working for the central Reliability Methodology department

of Infineon Technologies AG in Munich, Germany in the field of fWLR Monitoring. He is involved in advanced and novel test structure design, development of new stress methods and data analysis techniques on the topics: dielectrics, plasma induced damage, metallization and device degradation topics. He has published and co-authored numerous papers, given tutorials and invited talks at conferences and served in committees of the IEEE IRW, IEEE IRPS and of the "Workshop on Dielectrics in Microelectronics" (WoDiM) for many years. He is a senior member of the IEEE, Infineon's alternate of the JEDEC-subcommittee 14.2, member of the IEC WLR-workgroup TC 47 and co-chair of the German ITG-group 8.5.6 on "WLR and reliability simulations".

Amal Chabli

Amal Chabli joined the CEA in 1983. Mainly involved in physical and chemical characterization of materials for the micro and nanotechnology programmes, she has been the leader of the MINATEC nanocharacterization project. Since 2009, she is CEA director of research in the field of material characterization and she has managed several research programs in that field including the "Recherche Technologique de Base" French programme that supports the investment and R&D projects on the MINATEC nanocharacterization centre. She is actively contributing to the nanocharacterization road map of the Technology Division of the CEA promoting in particular the 3D nanocharacterization techniques. She has recently extended his research activity to the characterization of materials for photovoltaic applications. She has more than 80 publications with peer review selection.

Andrew Marshall

Andrew Marshall is an analog and digital IC design expert, working on benchmarking of leading edge and future technologies. He is a research professor at the University of Texas in Dallas. Dr. Marshall has authored/co-authored approximately 80 patents and 80 papers. He is co-author of the book 'SOI Design: Analog, Memory and Digital Techniques' and sole author of "Mismatch and Noise in Modern IC Processes". Dr. Marshall is a Fellow of both the IEEE and Institute of Physics, and Fellow Emeritus of Texas Instruments Incorporated.

Tutorial Programme

Monday, March 24th

Location: Palazzo Antonini Cernazai

08:00 Registration

08:50 Tutorials Opening – Gaudenzio Meneghesso, *Tutorials Chair, University of Padova, Italy*

09:00 Introduction to Microelectronic Test Structures
Stewart Smith, University of Edinburgh, UK
This presentation will begin with a review of test structures detailing their history and hot topics over the past 20+ years. The presentation will include the development of test structures for measuring sheet resistance, line width and contact resistance. Measurement and equipment developments will also be addressed focusing on procedures for obtaining accurate and repeatable measurements.

10.00 Coffee break

10.20 Process Control Monitoring and Tolerance Modeling for Analog/Mixed Signal CMOS Design
Benno Ankele, Infineon Technologies Villach, Austria
Test structures are used for process control monitoring (PCM) in IC fabrication as well as for tolerance modeling in IC design. In this tutorial we compare PCM requirements from factories and design perspectives. We address questions such as: which design parameters can / cannot be measured on PCM structures? How to prioritize PCM parameters? Do we need six-sigma in fabrication / in design? How to deal with design parameter tolerances in concurrent engineering? Can PCM techniques support parametric design for manufacturability? We strive towards a PCM concept which is lean but does not miss the link to statistical parameter tolerances and correlations used in analog/mixed signal IC design. Finally, our methodology shall also support high-volume products which are fabricated in a multi-factory scenario.

11:20 Advanced Non–Volatile Memories Characterization
Andrea Lacaita, Politecnico di Milano, Italy
10-years data retention is a key reliability target for non-volatile memories that should be guaranteed to all industrial products. To this aim, accelerated qualification tests are usually performed on new technologies and, to speed up data loss, Arrhenius-like time-to-temperature conversions are adopted. However, to derive reliable results a comprehensive understanding of the physical mechanisms responsible for data loss is needed together with a careful assessment of their activation energy. Moreover, a careful design of the accelerated qualification test is also essential, to account for real on-field operation and to address the impact of novel unexpected effects. The tutorial will address these referring to two case studies, i.e., floating-gate Flash and Phase Change memories. Focus will be on the physical mechanisms limiting data retention on the typical cell, showing data from 41-nm NAND, 45-nm NOR

and 45-nm PCM technologies and providing quantitative models able to explain experimental observations and supporting accelerated testing.

12.20 Lunch

14:00 Reliability Characterization in CMOS

Andreas Martin, Infineon, Neubiberg, Germany

This tutorial will present a brief overview of standard CMOS reliability characterization and some new and interesting developments. Two main characterization areas can be distinguished, process qualification and fWLR (fast Wafer Level Reliability) Monitoring. Test structure design is closely connected to the reliability stress and measurement sequence in use. Three fWLR examples are discussed in detail for: electromigration, NBTI (negative bias temperature instability) and PID (plasma induced damage). For any reliability data assessment and data comparison to reliability targets, properly incorporated data analysis methods are of great importance. The tutorial is aimed towards reliability engineers with some basic experience in the field.

15.00 Coffee break

15:20 Characterization of Nanoscale Materials and Devices

Amal Chabli, CEA Leti, France

In the field of micro- and nano-technologies, physical and chemical characterization is a powerful tool to support and improve the material choice, the analysis and correction of scaling effects, the design and validation of integration processes. Impressive capabilities are demonstrated in terms of sensitivity, selectivity, depth resolution, and spatial resolution. They may be based on instrumental effort including synchrotron radiation use or advanced configurations of probe-sample interaction such as scanning probe microscopy, nano-beam electron diffraction, transmission electron holography, electron tomography, and atom probe tomography. Numerous characterization techniques are available either on full-wafer layers or at the device level, providing complementary information. As an example, transmission electron microscopy allows the characterization of devices with nanometer-scale resolution, leading to 2D maps of electrical properties or strain distributions on nano-devices. The tutorial wills to overview how these capabilities allow to support the development of advanced technologies and devices and to understand the electrical tests results.

16:20 Benchmarking and Test Methodologies for Beyond CMOS Technologies

Andrew Marshall, University of Texas

Conventional silicon CMOS is approaching the point that scaling further will be a monumental task. It is generally assumed that for electronics is to continue scaling nanoelectronics must develop in a different direction. Some beyond CMOS devices are charge based, so minor adaptations to test methods are adequate. However, others are not charge based, and need new techniques to verify performance. Test and verification methods for beyond CMOS charge-based and non-charge based devices are discussed.

WELCOME RECEPTION

Monday, March 24th

Location: Sala del Pianoforte, Palazzo Caiselli

18:00-19:30 Welcome Reception

In order to welcome you to ICMTS 2014, a welcome reception will be held in Sala del Pianoforte of Palazzo Caiselli. The address is Vicolo Florio, Udine (2 in blue in the map).

TECHNICAL PROGRAMME

Tuesday 25th March

Location: Palazzo Antonini Cernazai

08:00–17.00 Registration

08:50 Conference Opening

Luca Selmi, General Chairman
Johan Klootwijk, Technical Program Chairman

SESSION 1: Parameter Extraction

09:00–10:40

Co-Chairs: Steward Smith, *University of Edinburgh, UK*
Loren W. Linholm, *Consultant, USA*

09:00

1.1 – Reconsideration of Effective MOSFET Channel Length Extracted from Channel Resistance (Invited)

Kazuo Terada

Hiroshima City University, Japan

"Channel Resistance Method" (CRM) to extract effective MOSFET channel length (L_{EFF}) is briefly surveyed and the L_{EFF} data for the MOSFET having both "halo" and "extension" in its channel are presented. It is found that LEFF is strongly affected by the halo dose and gate voltage. As the halo dose is decreased to zero, L_{EFF} converge to reasonable value and that for the MOSFET having uniform channel is uniquely determined, even if various sample MOSFET sets are used. Taking this property into consideration we propose new channel length definition, which is constant and obeys the classical current equation for the MOSFET with uniform channel, in order to provide the common channel length interpretation for both design and technology engineers.

09:40

1.2 – Effective Field and Universal Mobility in High-k Metal Gate UTBB- FDSOI Devices

O. Nier[1,2,3,4], D. Rideau[1], A. Cros[1], F. Monsieur[1], G. Ghibaudo[2], R. Clerc[5], J. C. Barbé[3], C. Tavernier[1] and H. Jaouen[1]

[1]*ST Microelectronics, Crolles, France;* [2]*IMEP-LAHC, MINATEC, France;* [3]*CEA-LETI, MINATEC, France;*

[4] *University of Udine, Italy;* [5] *Laboratoire Hubert Curien & Institut d'Optique, Saint-Etienne, France*

This paper aims to review important theoretical aspects of the effective field (E_{eff}) and parameter characterizing the "universal" behavior of the mobility $\mu_{eff}(E_{eff})$ curves. Experimental values for η are extracted for various front and back gate biases conditions, temperatures and for devices with various Equivalent Oxide Thicknesses. We demonstrated that a "nearly universal" trend for the mobility with respect to E_{eff} can be obtained only in a limited range of back biases. Indeed, we showed that in reverse back bias conditions, a single value of η does not make possible a "universal" plot of the μ_{eff} versus E_{eff}.

10:00

1.3 – Split-CV for pseudo-MOSFET characterization: experimental setups and associated parameter extraction methods

Luca Pirro, Irina Ionica, Gerard Ghibaudo and Sorin Cristoloveanu

IMEP-LAHC, Grenoble, France

In this paper, we present recent advances in the split-CV measurement applied for direct characterization of bare SOI wafers with the pseudo-MOSFET test method. We discuss the procedure and precautions needed for correct measurement of capacitance and conductance versus frequency. The experimental results are used to illustrate the extraction of carrier mobility and interface trap density.

10:20

1.4 – Extraction Procedure for Emitter Series Resistance Contributions in SiGeC BiCMOS Technologies

F. Stein[1,2], Z. Huszka[3], N. Derrier[1], C. Maneux[2] and D. Celi[1]

[1] *ST Microelectronics, Crolles, France;* [2] *IMS, Universitè Bordeaux, France;* [3] *ams AG, Austria*

The accurate determination of the emitter series resistance RE has been topic for numerous investigations throughout the development of modern bipolar device technologies. A good knowledge of the parasitic resistances of the device under test is important due to the apparent voltage drops over these resistors in high current operation. Opposed to the base and collector resistance today there are no appropriate individual test structures that allow for a precise determination of the emitter resistance. In this work we present the application of a new extraction method to a recent SiGeC HBT device technology for mmW applications. The new method allows a precise parameter determination of the desired resistance values without adding additional cost for a dedicated test structure.

10:40–11:00 Break

SESSION 2: Memory

11:00–12:20

Co-Chairs: Alan Mathewson, *Tyndall National Institute, IRL*
Kevin McCarthy, *UC Cork, IRL*

11:00

2.1 – Statistical Analysis of Resistive Switching Characteristics in ReRAM Test Arrays

Cristian Zambelli, Alessandro Grossi, Piero Olivo, Damian Walckzyk[1], Thomas Bertaud[1], Bernard Tillack[1,2], Thomas Schroeder[1,3], Valeriy Stikanov[4], Christian Walckzyk[1]
Università degli Studi di Ferrara, Italy; [1] *IHP, Germany;* [2] *Technische Universitat Berlin, Germany;* [3] *Brandenburgische Technische Universitat, Germany;* [4] *IASA, Kiev, Ukraine*

The design and the manufacturing of ReRAM test structures allow deeper insight in the performance of the FORMING, RESET, and SET operations at array level, providing details on the process induced variability of the technology, and on the potential sources of failures. Test structures allow also demonstrating the integration capability of the ReRAM technology using a CMOS-compatible process ramping up such non-volatile memory to a maturity level.

11:20

2.2 – Understanding the Switching Mechanism of Charge-Injection GeTe/Sb_2Te_3 Phase Change Memory through Electrical Measurement and Analysis of 1R Test Structure

N. Takaura, T. Ohyanagi, M. Tai, M. Kitamura, M. Kinoshita, K. Akita, T. Morikawa, [1]S. Kato, [1]M. Araidai, [1]K. Kamiya, [1]T. Yamamoto and K. Shiraishi[1]
Low-power Electronics Association & Project (LEAP), Japan; [1] *University of Tsukuba, Japan*

A new switching mechanism of charge-injection GeTe/Sb_2Te_3 phase change memory was investigated. DC and AC transient analysis provided deeper understanding of charge-injection enhancement. Electrical TEG measurements revealed the generation of resistance loop by DC sweep, reset switching of 4 ns, and MLC set with negative resistance for the first time.

11:40

2.3 – Common-Floating Gate Test Structure for Separation of Cycling-Induced Degradation Components in Split-Gate Flash Memory Cells

Nhan Do and Yuri Tkachev
Silicon Storage Technology, USA

The endurance limitation in split-gate flash memory is caused by electron traps in the tunneling oxide and in the floating gate channel silicon dioxide interface. We developed a novel test structure to separate these two degradation mechanisms. As a result, the amount of degradation in the floating gate channel can be accurately measured and suppressed. This improvement enables the new split-gate memory cell concept to be used in products that require high endurance performance.

12:00

2.4 – Accurate Modeling of Dynamic Variability of SRAM Cells in 28nm FDSOI Technology

J. El Husseini[1], A. Subirats[1,3], X. Garros[1], A. Makoseij[1], O. Thomas[1], V. Huard[2], F. Cacho[2], X. Federspiel[2] and G. Reimbold[1]

[1]*CEA-LETI, France;* [2]*ST Microelectronics, Crolles, France;* [3]*IMEP-LAHC, MINATEC, France*

The paper presents a new methodology to model the dynamic variability of SRAM cell in 28nm FDSOI technology. This approach can be easily integrated into SPICE and used for circuit degradation simulation. Based on this methodology, fast BTI stress measurements were carried out on SRAMsized MOSFETs in order to predict the bitcell's read margin degradation. Simulations results obtained on a 0.197 μm^2 SRAM cell are presented.

12:20–14:00 **Lunch**

SESSION 3: Process Characterization I: Contact Resistance

14:00–15:20

Co-Chairs: Hans P. Tuinhout, *NXP, The Netherlands*
Sathoshi Habu, *Agilent Technologies, Japan*

14:00

3.1 – A Test Structure and Analysis of Contact Resistance in FinFET Structure

Myung Gil Kang, Sang Hoon Lee, Mun Hyeon Kim, IL Ryong Kim, Chang Woo Oh, Dong-Won Kim, and Jong Shik Yoon
Semiconductor R&D Center, Samsung Electronics, Korea

In multi-gate transistors such as FinFETs and nano-wire FETs, it is difficult to extract contact resistance and source/drain diffusion resistance with conventional test structures such as Kelvin bridge. In this work, a simple and accurate extraction method of contact resistance and source/drain diffusion resistance is presented by using two MOSFET structures which share a common diffusion region. CMOS FinFETs on bulk Si using top-down process were used for the demonstration of contact resistance extraction method and we found that the contact resistance of FinFET contributes to 23.1 % and 23 % of total resistance for NFET and PFET, respectively.

14:20

3.2 – An Approach to Characterize Ultra-Thin Conducting Films Protected Against Native Oxidation by an *in-situ* Capping Layer

H. Van Bui, F. B. Wiggers, M. P. de Jong and A.Y. Kovalgin
MESA+, University of Twente, The Netherlands

We propose and demonstrate the applications of a test structure to characterize electrical properties of ultra-thin TiN films passivated by amorphous silicon (a-Si). The a-Si is to prevent the conducting layer from oxidation. Pt-contact pads are made on top of the a-Si. The good contact between the TiN and Pt,

which are separated by the a-Si layer, is obtained by the silicidation of a-Si and Pt at relatively low temperatures.

14:40

3.3 – Evaluation of Ultra-low Specific Contact Resistance Extraction by Cross-Bridge Kelvin Resistor Structure and Transmission Line Method Structure

Bing-Yue Tsui and Hsuan-Tzu Tseng
National Chiao-Tung University, Taiwan

This work evaluates the accuracy of the specific contact resistance (r_c) extraction by the cross-bridge Kelvin resistor (CBKR) structure and the self-aligned transmission line method (mTLM) structure considering three-dimensional effect. The mTLM structure is more accurate than the CBKR structure in theory. Its sensitivity to the process variation could be eliminated by averaging data. Nevertheless, the recessed contact interface would cause a complicated r_c extraction problem for both test structures at ultra-low $r_c \approx 10^{-8}\Omega$-cm^2.

15:00

3.4 – Gated Contact Chains for Process Characterization in FinFET Technologies

Tomasz Brozek, Stephen Lam, Shia Yu, Nobuharu Yokoyama[1], Mike Pak, Tom Liu, Rakesh Valishayee
PDF Solutions, USA; [1]*PDF Solutions, Japan*

Contact chain is a well known element of the diagnostic set of test structures used across many generations of silicon processes. Implementation of such test structures becomes challenging in new technologies with 3D devices, like FinFET. Contacts to active regions of such devices are inherently dependent on the architecture of epitaxial raised source and drain and for proper characterization require the presence of transistor gates, which set the environment for contacts. This paper describes example of test structures for contact process development for FinFET technologies. Instead of simple chain of contacts, each structure contains a series of active devices with common gate electrode used to turn on the chain of transistors to enable measurement of chain resistance. To discriminate between chain failures caused by an open contact or by other mechanism (e.g. bad transistor with very high threshold voltage) a series of measurement under various test conditions is performed and analysed to extract the contact failure rate. We also demonstrate application of the structures in FinFET process characterization.

15:20–17:20 Coffee, Poster and Exhibition Session

SESSION 4: Poster and Exhibitor presentations

15:20–15:45

Co-Chairs: Alain Toffoli, *CEA-LETI, France*
Anthony J. Walton, *Univ. Edinburgh, UK*

4.1 – A New Technique for Probing the Energy Distribution of Positive Charges in Gate Dielectric

Z. Ji, S. W. M. Hatta, J. F. Zhang, W. Zhang, J. Niblock[1], P. Bachmayr[1], L. Stauffer[1], K. Wright[1] and S. Greer[1]

Liverpool John Moores University, UK; [1] *Keithley, Cleveland, USA*

To simulate impact of stress-induced positive charges in gate dielectric on devices and circuits, it is essential to know their energy distribution both within and beyond substrate band-gap. A new technique is proposed. By implementing to standard parameter analyzer, it serves as a powerful tool for material and process screening.

4.2 – Low Specific Contact Resistivity Nickel to Silicon Carbide Determined Using a Two Contact Circular Test Structure

Yue Pan, Aaron M. Collins, Philip Tanner[1], Patrick W. Leech, Geoffrey K. Reeves and Anthony S. Holland

RMIT University, Melbourne, Australia, [1] *Queensland Microtechnology Facility, Brisbane, Australia*

We present the experimentally determined specific contact resistivity of as deposited Ni to 3-C silicon carbide using a novel test structure. The specific contact resistivity, extracted using this test structure and the corresponding methodology, is between 0.83 $\mu\Omega\text{cm}^2$ to 5.7 $\mu\Omega\text{cm}^2$.

4.3 – A Novel Apparatus For The Volume Estimation of In Vitro Thrombus Growth

A. Affanni, R. Specogna and F. Trevisan

DIEGM, University of Udine, Italy

We present a novel apparatus to measure the volume of thrombus induced in a lab-on-a-chip device under blood flow. Proposed inversion technique allows reconstructing thrombus volume versus time. This is not possible with current technology based on confocal microscopy, where thrombus volume is estimated only at the end of the experiment.

4.4 – Comparison of Channel Length Extracted from Gate Capacitance with That Extracted from Channel Resistance

Katsuhiro Tsuji and Kazuo Terada

Hiroshima City University, Japan

We compare the two effective channel lengths LCAP1 and LCAP2, which are extracted from the gate capacitances with and without the fringe component, with the effective channel length extracted from channel resistance LCEF. It is found that LCAP1 is about 30 nm longer than LCAP2 and almost coincides with LCEF for the samples made with 65-nm technology. It is considered that this difference is caused by the extension regions next to source and drain regions.

4.5 – 3D IC Testing Using a Chip Prober and a Transparent Membrane Probe Card

Naoya Watanabe, Michiyuki Eto[1], Kenji Kawano[1], and Masahiro Aoyagi

National Institute of Advanced Industrial Science and Technology, Tsukuba-shi, Japan; [1] *STK Technology Co., Ltd., Oita, Japan*

We performed pre- and post-bond testing of an SRAM/flash memory chip using a chip prober with a transparent membrane probe card. By deformation of PEN film (base material of probe card) during probing, low-load and damageless probing was possible and we successfully conducted pre-bond testing of 50 μm-thick SRAM/flash memory chip and post-bond testing of stacked chips.

4.6 – Characterisation of Residual Stress in Dielectric Films Studied by Automated Wafer Mapping

R. Walker, E. Sirotkin, G. Schiavone, J. G. Terry, S. Smith, A. R. Mount, [1]M. P. Y. Desmulliez and A. J. Walton

University of Edinburgh, UK; [1] *Heriot-Watt University, Edinburgh, UK*

SU-8 is a negative toned epoxy based photoresist, which is widely used as a structural and dielectric layer in the fabrication of MEMS devices. However this material normally exhibits high levels of stress during processing. This paper reports detailed quantitative data following previous work, where we demonstrated Parylene-C as a possible replacement for SU-8. Particularly, this paper details the characterisation of residual stress in (i) SU-8 films as a result of processing temperatures and (ii) post processing thermal treatment of Parylene-C. This characterisation includes wafer mapping strain using rotating pointer arm test structures, and deriving the stress from independent measurements of strain and Young's modulus.

4.7 – A Test Structure for Analysis of Temperature Distribution in Stacked IC with Sensing Device Array

T. Matsuda, K. Yamada, H. Iwata, T. Hatakeyama, M. Ishizuka and T. Ohzone[1]

Toyama Prefectural University, Japan; [1] *Dawn Enterprise, Nagoya, Japan*

A test structure for analysis of temperature distribution in stacked IC, which has a top tier chip attached on a bottom dummy chip with adhesive layer, is presented. The devices with four kinds of thickness of 50 - 410 μm were fabricated. Dependences of the temperature on distance from the heater resistor were analyzed with on-chip sensor arrays, as well as fast transient phenomena. The thinner top tier structures showed the higher temperature and affected the temperature distributions. The test structure can provide an effective way for analysis of thermal properties in various LSIs.

Wednesday 26th March

Location: Palazzo Antonini Cernazai

08:15–17.00 Registration

SESSION 5: Yield

09:00–10:40

Co-Chairs: Antoine Cros, *ST Microelectronics, France*
Christopher Hess, *PDF Solutions, USA*

09:00

5.1 – Processor Yield at 14nm and Beyond (Invited)

Greg Yeric

ARM Holdings, Austin, USA

Moore's law was created with an understanding of yield limitations on integrated circuits, but as we enter the 1x logic nodes, quantifying yield loss becomes exponentially more complicated. This is due primarily to the significant process complexities that are being added in an attempt to deliver historic scaling trends. The complexity drives a need for increasingly accurate quantification of cost/area/yield trade-offs. Even with this onslaught of process complexity, the underlying process scaling will fall short of expected scaling. We can offset this scaling gap with increased focus on additional areas of guard-banding, such as variability modeling and reliability modeling. If all of the above sounds like "test structures", it should. This paper will examine these technology trends and highlight areas of opportunity for test structure measurements.

09:40

5.2 – A Novel Compact Model of the Product Marginal Yield and its Application for Performance Maximization

Atsushi Tsuda, Takeshi Okagaki, Masako Fujii, Toshikazu Tsutsui, Yoshio Takazawa, Koji Shibutani, Shigeo Ogasawara, Miho Yokota, Kazunori Onozawa

Renesas Electronics Corporation, Japan

In this paper, we presented a novel compact model to calculate the product performance accurately. It becomes possible to estimate marginal yield before pilot wafer by input of a little Si information to compact model. In the result, we can quantitatively determine optimal transistor target by using our model.

10:00

5.3 – In-Situ Variability Characterization of Individual Transistors using Topology-Reconfigurable Ring Oscillators

A.K.M Mahfuzul Islam and Hidetoshi Onodera

Kyoto University, Japan

We propose a variability characterization methodology which enables characterization of individual transistors under swithing condition. We use a topology-reconfigurable ring oscillator (RO) where various nMOSFET and pMOSFET-sensitive topologies can be achieved. Using the frequency measurements of different topologies, estimation of each transistor parameters

become possible. Measurement and estimation results from a 65-nm process shows the validity of our proposed technique. We successfully characterized individual transistor static variation as well as RTN induced threshold voltage fluctuation.

10:20

5.4 – Circuits to Measure the Delay Variability of MOSFETs

Karthik Balakrishnan and Keith Jenkins

IBM T.J. Watson Research Center, USA

Two test circuits have been implemented and measured in order to characterize delay variability in individual MOSFETs. Measurement results show that both circuits have high sensitivities to gate resistance, which differentiate them from other circuits which characterize variations in traditional DC parameters such as threshold voltage and channel length.

10:40–11:00 Break

SESSION 6: RF Characterization

11:00–12:20

Co-Chairs: Alexey Kovalgin, *Univ. Twente, The Netherlands*
Larg H. Weiland, *PDF Solutions, USA*

11:00

6.1 – Effect of Seed Layers on the Performance of Planar Spiral Micro-Inductors

R. Walker, E. Sirotkin, J. G. Terry, S. Smith, [1]M. P. Y. Desmulliez and A. J. Walton

University of Edinburgh, UK; [1] *Heriot-Watt University, Edinburgh, UK*

This paper reports on the effect of the electrical performance related to magnetic seed layers used within planar power micro-inductors. These studies involve structural and magnetic characterisations of Ni80Fe20 films electro-deposited on non-magnetic and magnetic seed layers (i.e. copper and nickel respectively). Microelectronic mechanical test structures and X-ray analysis have been used to characterise the stress levels and structural properties of Ni80Fe20 films electro-deposited on both copper and nickel seed layers. In addition, planar spiral micro-inductors have been fabricated in order to confirm the improvement in the electrical performance from magnetic seed layers, as a result of enhanced magnetic and resistive contribution.

11:20

6.2 – A semi-distributed method for Inductor de-embedding

J. Dang, A. Noculak[1], F. Korndörfer[2], C. Jungemann[1], and B. Meinerzhagen

TU Braunschweig, Germany; [1] *Aachen University, Germany;* [2] *IHP, Frankfurt (Oder), Germany*

This paper presents a de-embedding method based on "pad" and "thru" test structures for on-wafer inductor characterization. A transmission line model in combination with parallel admittances describing the pads is used to describe the

"thru" test structure. This method is compared to the standard "open-short", "open-thru" and "pad-open-short" de-embedding methods and electromagnetic simulations. It is demonstrated that the proposed method is more accurate or saves chip area compared to the standard de-embedding methods.

11:40

6.3 – Matched Test Structures for Accurate Characterization in Millimeter Wave Range

Rachid Hamani[1,2], Cristian Andrei[1], Bernard Jarry[2], and Julien Lintignat[2]

[1]*NXP Semiconductors, France;* [1]*XLIM, Limoges, France*

This paper, presents a novel methodology for small signal equivalent circuit extraction suitable for high frequency characterization up to mm-wave range. This methodology allows the de-embedding and the extraction of RF characteristics by the use of a smart matching at 50% of the transistor connected in GSG probe pads. The method has been validated first on a test module based on RFMOS transistor fabricated in BiCMOS 0.25 μm technology from NXP Semiconductors. The results of matched RFMOS transistors at 30.5GHz are presented here and show good agreement between measurements/extractions and calculations (e.g. for). Second, a bipolar transistor matched test structure is investigated. An improvement of transmission gain of matched test structured from -12dB to -0.2dB has been found using measurements and simulated data.

12:00

6.4 – On Wafer Silicon Integrated Noise Source characterization up to 110 GHz based on Germanium-on-Silicon Photodiode

S. Oeuvrard[1,2], J.-F. Lampin[2], G. Ducournau[2], S. Lepilliet[2], F. Danneville[2], T. Quemerais[1], D. Gloria[1]

[1]*ST Microelectronics, France;* [2]*IEMN, Villeneuve d'Ascq, France*

In this work, a new concept of optical noise source has been developed and characterized, based on a Germanium-on-Silicon photodiode. Photodiodes RF output power measurements have been achieved up to 210 GHz, using an appropriate Optical/High frequency bench, and demonstrating available power in the range of -30dBm. It turned out that the Excess Noise Ratio of those photodiodes, after careful measurements and calculations, was in the range of 35 dB at 110 GHz.

12:20–14:10 **Lunch**

14:10–14:20 **ICMTS 2015 Presentation**

SESSION 7: Emerging Technologies

14:20–15:40

Co-Chairs: Colin McAndrew, *Freescale, USA*
Kazuo Terada, *Hiroshima CU, Japan*

14:20

7.1 –A Test Structure of Bypass Diodes for On-chip

High-Voltage Silicon Photovoltaic Cell Array
Isao Mori, Masanori Kubota and Yoshio Mita
University of Tokyo, Japan

A bypass diode is an effective solution for degradation issue of a partially-shaded photovoltaic cell array. We proposed a test structure of bypass diodes for the on-chip high voltage silicon photovoltaic cell array we have previously proposed. It shows an appropriate diode size and whether their fabrication process was performed successfully.

14:40

7.2 – A Single-Photon Avalanche Diode test chip in 150nm CMOS technology

Lucio Pancheri, Leo H. C. Braga[1], Hesong Xu[1], David Stoppa[1] and Gian-Franco Dalla Betta
DII, University of Trento, Italy; [1] *Fondazione Bruno Kessler, Trento, Italy*
The design of Single-Photon Avalanche Diode (SPAD) arrays requires a clear understanding of the correlation between device characteristics and the geometrical and structural device parameters. This work presents a test chip, designed in a 150-nm CMOS technology, tailored to the extraction of the main features for SPADs of different shapes and sizes.

15:00

7.3 – Test Structure for Electrical Characterization of Copper Nanowire Anisotropic Conductive Film (NW-ACF) for 3D Stacking Applications

Jing Tao, Alan Mathewson, Kafil M. Razeeb
Tyndall National Institute, Cork, Ireland
Copper nanowire arrays (≈200 nm diameter) grown in porous polymer template is a potential low temperature interconnection technology compared with metal/metal or solder microbump interconnects for 3D chip stacking. To advance this technology, good understanding of material and process related electrical properties is required. In this paper, a stacked test chip module with copper daisy chain pattern, which is finished by ≈1 μm indium bonding layer, has been designed to extract the resistance and capacitance data of the NW-ACF.

15:20

7.4 – Compressively-Stressed Test Structures for Opaque Micro-Structures Releasing Visualization

Tixier-Mita A., Lebrasseur E., Takahashi T., [1]Français O., [1]Le Pioufle B., Mita Yoshio, Fujita H., Toshiyoshi H.
University of Tokyo, Japan; [1] *Ecole Nationale Supérieure, Cachan, France*

Compressively-stressed test structures have been fabricated to precisely determine the releasing time of low stress and opaque MEMS. These test structures will deform as soon as it is released, in contrast to low stress target structures that remains flat. Thanks to the test structure, it becomes possible to detect the releasing with an optical microscope.

15:40–16:00 Break

SESSION 8: Material Characterization

16:00–17:20

Co-Chairs: Colin McAndrew, *Freescale, USA*
Greg Yeric, *ARM, USA*

16:00

8.1 – Air-CPW Test Structure for Broadband Permeability Spectra Measurements of Thin Ferromagnetic Films

E. Sirotkin, R. Walker, J. G. Terry, S. Smith, and A. J. Walton
Scottish Microelectronics Centre, University of Edinburgh, UK
In this paper we demonstrate a novel technique based on a coplanar waveguide (CPW) test structure for broadband characterization of the intrinsic permeability spectra of thin ferromagnetic films. This measurement is based on the analysis of S-parameters measured from the CPW test structure connected to Vector Network Analyzer (VNA) in transmission. The specific feature of the test structure is a small 50% 'air-CPW' section loaded with thin layer of material under test (MUT). This principal feature allows independent measurements and component separation of complex permeability and permittivity spectra of conductive ferromagnetic films. The technique can be conveniently applied for characterization of both continuous and patterned magnetic films.

16:20

8.2 – Process Parameter Calibration for Millimeter-Wave CMOS Back-End Device Design with Electromagnetic Field Analysis

S. Amakawa, A. Orii, K. Katayama, K. Takano, M. Motoyoshi, T. Yoshida, and M. Fujishima
Hiroshima University, Japan
This paper presents a systematic procedure for calibrating process parameters for electromagnetic field analysis. A few CMOS backend material parameters are first chosen as fitting parameters by sensitivity analysis, and then their values are unambiguously determined from contour maps showing electrical characteristics versus material parameters. Calibration with measured data for 1–170 GHz is shown to give a reasonable prediction even at higher frequencies.

16:40

8.3 – Characterization and Development of Materials for an Integrated High-Temperature Sensor Using Resistive Test Structures

A. Tabasnikov, A. S. Bunting, J. G. Terry, J. Murray, [1]G. Cummins, [2]C. Zhao, [2]J. Zhou, [2]R. Y. Fu, [1]M. P. Y. Desmulliez, A.J. Walton and S. Smith
University of Edinburgh, UK; [1] *Heriot-Watt University, Edinburgh, UK;* [2] *University of the West of Scotland, Paisley, UK*
This paper reports the application of test structures for the evaluation of tantalum nitride (TaN) as a material for integration with high temperature electronics. The process involves the reactive sputtering of TaN and its consequent annealing in a vacuum to reach the target specifications of low temperature

coefficient of resistance (TCR). The test wafer has been designed to both evaluate the temperature performance of thin films and to study the possibility of integrating different metal films into a single sensing device. The TaN resistors resulting from this work have a TCR of $-150 \cdot 10^{-6}$ °C^{-1}, which remains stable after 6 hours of annealing at 600 °C.

17:00

8.4 – Thickness Evaluation of Deposited PureB Layers in Micro-/Millimeter-Sized Windows to Si V. Mohammadi, S. Ramesh and L. K. Nanver
Delft University of Technology, The Netherlands

Resistance measurement structures are designed for monitoring thickness variations in nanometerthin pure-boron (PureB) layers deposited on Si for (photo-)diode applications where angstrom-level variations impact performance. In millimeter-large windows a fine resolution is achieved with metal-contact arrays patterned directly on the PureB. For micron-sized windows Kelvin structures provide a sensitive solution.

17:20 End of Session 8

18:00 Short excursion to Tiepolo Galleries, Palazzo Arcivescovile, Udine

20:00 Banquet, Casa della Contadinanza.

Thursday 27th March

Location: Palazzo Antonini Cernazai

SESSION 9: Process Characterization II: Devices and thin layers

09:00–10:40

Co-Chairs: Bing-Yue Tsui, *Nat. Chiao Tung Univ., Taiwan*
Yoshio Mita, *University of Tokyo, Japan*

09:00

9.1 – Calibration Methods for Silicon Nanowire BioFETs (Invited)
A. Vacic, J. M. Criscione, E. Stern, N. K. Rajan, T. Fahmy, and M. A. Reed
Institute for Nanoscience and Quantum Engineering, Yale University, USA

Nanowire Field Effect Transistors have emerged as a promising technology for point-of-care application. However, their application as quantitative sensors has not been well explored. In this work we propose a calibration scheme for multiplexed nanoribbon field effect sensors by utilizing the initial current rate rather than the end point detection. A linear response of nanosensors is observed in medically relevant range of analyte concentration. Moreover, we are able to show that top-down fabrication technique yields reproducible result and devices with uniform electrical characteristics. In addition, we demonstrate that device calibration can be done by using either baseline current or device transconductance normalization.

09:40

9.2 – Effects of Metal Spacing and Poly-Silicon Layers on Pulsed-Laser Single Event Transient Testing

Jinshun Bi, Chuanbin Zeng, Linchun Gao, Duoli Li, Gang Liu, Jiajun Luo and Zhengsheng Han

Chinese Academy of Sciences, Beijing, China

The influence of metal spacing and poly-crystalline silicon gate and silicide technology on single event transients occurring in pulsed laser irradiated test patterns was investigated, including SET rise time, fall time, pulse width, pulse maximum, and collected charge. Quantitative dependence of the transients on metal spacing and silicide processing is reported.

10:00

9.3 – Test Structure to Evaluate the Impact of Neighboring Features on Stress of Metal Interconnects

Brad Smith and Mehul Shroff

Freescale Semiconductor, Austin, USA

The stress-inducing effects of neighboring features were studied using special stress migration test structures with various layouts of neighboring combs. The structures with narrow widths showed no change in stress migration, with or without near neighbor structures. However, structures built with wider lines showed 3X worse stress migration performance when perpendicular combs were present nearby, almost independent of the spacing to the combs.

10:20

9.4 – Direct Probing Characterization Vehicle Test Chip For Wafer Level Exploration of Transistor Pattern on Product Chips

Christopher Hess, Kelvin Doong[1], Hans Eisenmann[2], Scott Lin[1], Larg Weiland, Amit Joag, Balasubramania Murugan and Sa Zhao

PDF Solutions, San Jose, USA; [1] PDF Solutions, Zhubei City, Taiwan; [2] PDF Solutions, Munich, Germany

Due to recent changes in the manufacturing of FEOL (front end of line) layers it is increasingly difficult to provide rapid learning cycles required to drive yield improvement on new product introduction (NPI). The Direct Probe Characterization Vehicle (DPCV) Test Chips presented here provides direct access to thousands of transistors on a product chip. Only two masks are needed (contact & metal 1) to provide access to the DUTs of the unchanged FEOL layers of a product chip. The DPCV test chip is capable of matching the distribution of product transistor pattern. Measurement data indicate that corrective actions to the design and/or process recipes will reduce the gap between measured product chip transistors and their expected behavior based on SPICE simulations.

10:40–11:00 Break

SESSION 10: Matching

11:00–12:20

Co-Chairs: Colin McAndrew, *Freescale, USA*
Greg Yeric, *ARM, USA*

11:00

10.1 – A Compact Array for Characterizing 32k Transistors in Wafer Scribe Lanes

Christopher S. Chen, Liping Li, Queennie Lim, Hong Hai Teh, Noor Fadillah Binti Omar, Chun Lee Ler and Jeffrey T. Watt
Process Technology Development, Altera Corporation

A new test structure was designed to enable characterization of 32k transistors in a wafer scribe lane using standard parametric test equipment. New methods were developed to mitigate decoder series resistance issues. Random variations in transistor threshold voltage measurement data followed the expected normal distribution up to 4.1 sigma.

11:20

10.2 – Analysis of Process Impact on Local Variability Thanks to Addressable Transistors Arrays

A. Cros, T. Quemerais, A. Bajolet, Y. Carminati, P. Normandon, F. Kergomard, N. Planes, D. Petit, F. Arnaud and J. Rosa
ST Microelectronics, Crolles, France

We designed an addressable transistor arrays to analyse local variability at the wafer scale. On FDSOI substrates, we measure no impact of the silicon thickness variations on short channel transistors, and demonstrate that the impact on large area transistors is no more visible when the Tsi is well controlled.

11:40

10.3 – Cascode Configuration as a Substitute to LDE MOSFET for Improved Electrical Mismatch Performance

L. Rahhal[1,2], G. Bertrand[1], A. Bajolet[1], J. Rosa[1] and G. Ghibaudo[2]

[1]*ST Microelectronics, Crolles, France;* [2]*IMEP-LAHC, Minatec, Grenoble, France*

The work presented in this paper investigates the possibly of replacing a Lateral Drain Extended MOS (LDEMOS) SOI transistors by a cascode configuration to improve electrical mismatch performance. Thus, the cascode connection of two MOS devices, known to sustain high drain voltage of LDEMOS SOI transistors, offers the same mismatch robustness of Silicon On Insulator (SOI) MOS transistors. The individual mismatch constants associated to Vt for the presented cascode configuration are shown to have similar values to those reported for individual MOS devices.

12:00

10.4 – A Cross-Coupled Common Centroid Test Structure Layout Method for High Precision MIM Capacitor Mismatch Measurements

Hans Tuinhout and Nicole Wils

NXP Semiconductors, Eindhoven, The Netherlands

A new layout method based on highly symmetrical quadruple connection rails enables much higher precision DUT-1-2-1-2 MIM capacitors mismatch characterization and gives significantly smaller systematic mismatch errors compared to approaches reported before. A record low random mismatch fluctuation standard deviation of 20 ppm (0.002%) is shown to be attainable for large MIM capacitor pairs.

12:20 Best paper announcement and closing remarks

12:40 Lunch

14:20 Excursion

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Tsuyoshi Sekitani	University of Tokyo	Japan
Luca Selmi	Università degli Studi di Udine	Italy
Brad Smith	Freescale Semiconductor	USA
Stewart Smith	Scottish Microelectronics Centre	UK
Lee Stauffer	Keithley Instruments Inc.	USA
Kenichi Takeda	Hitachi	Japan
Kiysohi Takeuchi	Renesas Electronics Corporation	Japan
Kazuo Terada	Hiroshima City University	Japan
Alain Toffoli	Cea/Leti - Minatec	France
Bing-Yue Tsui	National Chiao Tung University	Taiwan
Hans P.Tuinhout	NXP Semiconductors	The Netherlands
Bill Verzi	Agilent Technologies	USA
Anthony J.Walton	University of Edinburgh	UK
Larg H.Weiland	Pdf Solutions Inc.	USA
Greg Yeric	Arm	USA

ICMTS 2014 CONDENSED PROGRAM

Monday, March 24	
08:00	Registration
08:50	Tutorial opening
09:00	Test Structure Fund.
10:00	Break
10:20	Process Control and Tolerance for Analog Design
11:20	NVM Characterization
12:20	Lunch
14:00	Reliability Characterization in CMOS
15:00	Break
15:20	Nanoscale materials and devices characterization
16:20	Beyond CMOS Benchmarking and Test
17:20	End of Tutorials
	Welcome Reception

Tuesday, March 25	
08:00	Registration
08:50	Conference Opening
09:00	Session 1 Parameter extraction (with Invited)
10:40	Break
11:00	Session 2 Memory
12:20	Lunch
14:00	Session 3 Process charac.: contact resistance
15:20	Session 4 Coffee, Posters and Exhibition
17:20	End of Day 1

Wednesday, March 26	
08:15	Registration
09:00	Session 5 Yield (with Invited)
10:40	Break
11:00	Session 6 RF characterization
12:20	Lunch
14:10	ICMTS 2015
14:20	Session 7 Emerging tech.
15:40	Break
16:00	Session 8 Material charac.
17:20	End of Day 2
18:00	Short excursion
20:00	Banquet

Thursday, March 27	
08:30	Registration
09:00	Session 9 Process charac.: devices and thin layers (with Invited)
10:40	Break
11:00	Session 10 Matching
12:20	Best Paper and Closing remarks
12:40	Lunch
14:20	Excursion