ICMTS 2013 TECHNICAL PROGRAM (PRELIMINARY)

Tuesday, March 26

9:00 Greetings
Tatsuya Ohguro, *General Chair*
Kiyoshi Takeuchi, *Technical Program Chair*

SESSION 1: MEMS

9:10 – 10:50
Co-Chairs: Kjell Jeppson, *Chalmers University of Technology, Sweden*

1.1 An Integrated CMOS-MEMS Probe having Two-Tips per Cantilever for Individual Contact Sensing and Kelvin Measurement with Two Cantilevers
Kota Hosaka, Satoshi Morishita, Isao Mori, Masanori Kubota, and Yoshio Mita
University of Tokyo, Japan
The MEMS probe having two tips per cantilever needle is proposed to enable four-terminal (Kelvin) measurement using only two needles. The tips are 5μm in height and placed with 20μm of distance on the 500μm-long, 50μm-wide cantilever. The probe is post-processed on a low cost CMOS circuit, and the system may provide many new features such as individual touch force sensing and probe contact detection.

1.2 Characterization and Integration of Parylene as an Insulating Structural Layer for High Aspect Ratio Electroplated Copper Coils
R. Walker, E. Sirotkin, I. Schmueser, J.G. Terry, S. Smith, J.T.M. Stevenson and A.J. Walton
University of Edinburgh, UK
This paper reports the development of processing methods and test structures for the characterisation and evaluation of Parylene-C as an insulating structural layer material for integration with planar micro-inductors. The process involves the filling of high aspect ratio gaps between copper structures with Parylene and subsequent chemical mechanical planarisation. A test chip has been designed to characterise this process and the results presented. Subsequently complete micro-inductors, with magnetic cores, have been fabricated to demonstrate the capability of the process.

1.3 Micromechanical Test Structures for the Characterization of the Magnetic Response of Electroplated NiFe Cantilevers and their Viability for use in MEMS Switching Devices
G. Schiavone, J. Murray, J.G. Terry, S. Smith, M.P.Y. Desmulliez and A.J. Walton
University of Edinburgh, UK
This work presents the fabrication of a series of test devices aimed at demonstrating the viability of electroplated NiFe freestanding structures for use in magnetically actuated MEMS switches. Preliminary results show promising actuation responses and further testing will enable the quantitative measurement of these characteristics. In addition, this may allow for the mechanical characterization of freestanding structures in other materials by means of magnetic actuation, simply by depositing small quantities of NiFe or other magnetic materials in convenient areas of existing devices.

1.4 Investigation of Devices for In-Vivo Energy Harvesting through Blood Flow Excitation
Rosemary O'Keeffe, Nathan Jackson, Alan Mathewson, Kevin McCarthy
University College Cork, Ireland
Test structures were designed based on previously designed procedure for highly efficient AlN piezoelectricity generation. These devices were based on FEM models and have been used to determine the feasibility of in-vivo energy harvesting from blood flow as well as used to optimize the models for future generations of devices.

1.5 A New Measurement Set-up to Investigate the Charge Trapping Phenomena in RF MEMS Packaged Switches
Marco Barbato, Valentina Giliberto, and Gaudenzio Meneghesso
University of Padova, Italy
In this work we develop a new measurement set up able to predict the lifetime of packaged ohmic RF MEMS submitted to long actuation periods. Experimental results were carried out for long time period in

order to verify the degradation law relates to charge trapping and stiction problems on cantilever and clamped-clamped switches.

10:50 – 11:00 **Exhibition Presentations**

11:00 – 11:20 **Break**

SESSION 2: TSV and 3D

11:20 – 12:20
Co-Chairs: Yosiho Mita, *University of Tokyo, Japan*

2.1 Test Structure and Analysis for Accurate RF-Characterization of Tungsten Through Silicon Via (TSV) Grounding Devices
Volker Blaschke and Hadi Jebory
TowerJazz, Newport Beach, California, USA
We present an analysis on the extraction of the through silicon via (TSV) inductance from single port and two port S-parameter results. The test structure design is shown to significantly impact the extracted value and could cause inaccurate results and subsequently errors in the Spice model if not accounted for. We will show that an analytical model of the return circuit loop that the TSV forms with the test structure, does provide a useful assessment of the accuracy of the measured results. This analysis further provides important input for test structure design and when to use single port or two port test structures for TSV measurement.

2.2 Test Structures for Electrical Evaluation of High Aspect Ratio TSV Arrays Fabricated Using Planarised Sacrificial Photoresist
R. Zhang, Y. Li, C.C. Dunare, A.S. Bunting, S. Smith, J.T.M. Stevenson, A.J. Walton
University of Edinburgh, UK
An improved bottom-up electroplating technique has been successfully developed for the fabrication of TSV arrays with about 10:1 aspect ratio. 125,500 TSVs are formed in the area of a 6×6cm square with a pitch of 170 μm. A method of visually inspecting the via yield is presented and Kelvin test structures and contact chain test structures have been fabricated to electrically evaluate single and multiple TSVs respectively.

2.3 A Novel Silicon Interposer Capable of Measuring the Designs with Contacts on Both Side of Wafer
Jaber Derakhshandeh, Negin Golshani, Lis K. Nanver, Loek A. Steenweg, Wim van der Vlist
Delft University of Technology, Netherlands
In this paper we report the design and fabrication process of a novel silicon based interposer suitable for designs where contacts are in the both sides of wafer. This interposer transfers all contacts to the one side of the wafer so that the measurement can be done using one sided probe stations.

12:20 – 13:50 **Lunch**

SESSION 3: Capacitance

13:50 – 15:10
Co-Chairs: Larg H. Weiland, *PDF Solutions, USA*
Alain Toffoli, *CEA-LETI, France*

3.1 Characterization of Capacitance Mismatch Using Simple Difference Charge-Based Capacitance Measurement (DCBCM) Test Structure
Ken Sawada[1], Geert Van der Plas[2], Yuichi Miyamori[3], Tetsuya Oishi[3], Cherman Vladimir[2], Abdelkarim Mercha[2], Verkest Diederik[2], and Hiroaki Ammo[3]
[1]*Sony Corporation to IMEC,* [2]*IMEC, Belgium*
[3]*Sony Corporation, Japan*
We proposed new difference charge-based capacitance measurement (DCBCM) test structures for measuring capacitance mismatch. In DCBCM parasitic components can be eliminated and we can measure 100aF mismatch with 7.2aF accuracy. We demonstrate accurate mismatch characteristics on oltage-dependent capacitances. DCBCM gives measurement methods suitable for evaluating capacitance

mismatch beyond 20nm node.

3.2 Comparison of C-V Measurement Methods for RF-MEMS Capacitive Switches

Jiahui Wang, Cora Salm, and Jurriaan Schmitz
University of Twente, Netherlands

The applicability of several capacitance-voltage measurement methods is investigated for the on-wafer characterization of RF-MEMS capacitive switches. These devices combine few-picofarad capacitance with a high quality factor. The standard quasistatic and high-frequency measurements are employed, as well as the recently introduced very-low-frequency method. Significant differences are found around the pull-in and pull-out voltages.

3.3 Effective Channel Length Estimation Using Charge-Based Capacitance Measurement

Katsuhiro Tsuji and Kazuo Terada
Hiroshima City University, Japan

An effective channel length is estimated from the C-V curves of actual size MOSFETs which are measured using charge-based capacitance measurement (CBCM). To evaluate the accurate capacitances between the gate and the channel of sample MOSFETs, their parasitic capacitances are removed by using the test MOSFETs having various channel size and special test structures. A good linear relation between the gate-channel capacitance and the design channel length is obtained and then, the effective channel length is estimated from it. It is found that the obtained effective channel length is shorter than that extracted by the conventional channel resistance method.

3.4 A New Ultra-Fast Single Pulse Technique (UFSP) for Channel Effective Mobility Evaluation in MOSFETs

Z. Ji, J. Gillbert, J. F. Zhang, and W. Zhang
Liverpool John Moores University, UK

A new technique is proposed for mobility evaluation to overcome the shortcomings of conventional techniques. By measuring Id and Cgc simultaneously within 3μs, it removes adverse impact of Vd on mobility, avoids cable-switching, and minimizes charge trapping. Besides, it can work on high ‘leaky’ devices without special RF structure.

15:10 – 15:40 Break

SESSION 4: Noise and RF

15:40 – 17:00

Co-Chairs: Hi-Deok Lee, *Chungnam National University, Korea*
Tatsuya Ohguro, *Toshiba Corporation*

4.1 Optical High Frequency Test structure and Test Bench definition for on Wafer Silicon Integrated Noise Source characterization up to 110 GHz based on Germanium-on-Silicon Photodiode

S. Oeuvrard[1, 2], J.-F. Lampin[2], G. Ducournau[2], L. Virot[1, 3], J.M. Fedeli[3], J.M. Hartmann[3], F. Danneville[2], Y. Morandini[4], D. Gloria[1]
[1]*STMicroelectronics, France*
[2]*IEMN, France*
[3]*CEA LETI, France*
[4]*DOLPHIN INTEGRATION, France*

A new Optical-High-Frequency test structure and dedicated test bench have been developed to characterize a Germanium-on-Silicon photodiode intended to be used as an integrated noise source, a first step to Transistor Noise Figure on-wafer extraction. Continuous wave signals have been measured from these photodiodes, with state-of-the-art RF power higher than -20 dBm at 109 GHz.

4.2 Measurements of SRAM Sensitivity against AC Power Noise with Effects of Device Variation

Takuya Sawada[1], Kumpei Yoshikawa[1], Hidehiro Takata[2], Koji Nii[2], and Makoto Nagata[1,3]
[1]*Kobe University, Japan*
[2]*Renesas Electronics Corporation, Japan*
[3]*CREST, JST, Japan*

SRAM exhibits sensitivity of false operation against static and sinusoidal supply voltage variation. A measurement system in this paper combines direct RF power injection, on-chip power supply voltage

monitoring, and built-in self test of SRAM memory operations. The response of bit error rate against voltage variation is quantitatively demonstrated.

4.3 On the Length of THRU Standard for TRL De-embedding on Si Substrate above 110 GHz

A. Orii, M. Suizu, S. Amakawa, K. Katayama, K. Takano, M. Motoyoshi, T. Yoshida, and M. Fujishima
Hiroshima University, Japan

It is known that the THRU standard (a transmission line) used for thru-reflect-line (TRL) calibration/de-embedding for S parameter measurement has to be long enough for it to work reliably. But ideally, TRL standards should occupy as little precious silicon real estate as possible. This paper attempts to experimentally find out how long a THRU is long enough above 110 GHz. The results indicate that a THRU should be 400μm or longer, excluding pads and pad-to-line transitions.

4.4 Evaluation of 1/f Noise Variability in the Subthreshold Region of MOSFETs

Hans Tuinhout and Adrie Zegers-van Duijnhoven
NXP Semiconductors, Netherlands

A test module with multiple MOSFET types and different layout implementations is used for studying several under-explored aspects of 1/f noise modeling. Using a commercial noise characterization system, variability of 1/f noise is evaluated in weak-inversion, revealing important subtleties of low frequency noise.

Wednesday, March 27

SESSION 5: Variability and Yield

9:00 – 10:20

Co-Chairs: Yoichi Tamaki, *CASMAT, Japan*
Hans Tuinhout, *NXP Semiconductors, Netherlands*

5.1 Newly developed Test-Element-Group for Detecting Soft Failures of the Low-Resistance-Element using Doubly Nesting Array

Shingo Sato, Hiroki Shinkawata, Atsushi Tsuda, Tomoaki.Yoshizawa, and Takio Ohno
Renesas Electronics Corporation, Japan

We report newly developed Test-Element-Group for detecting soft failures of low-resistance-element like interconnect via using doubly nesting array. We detected the soft failure of fine via which resistance had about 10 times larger resistance than normal via using this structure manufactured in 40nm CMOS technology.

5.2 New Methodology for Drain Current Local Variability Characterization using Y Function Method

L. Rahhal[1,2], A. Bajolet[1], C. Diouf[1,2], A. Cros[1], J. Rosa[1], N. Planes[1] G. Ghibaudo[2]
[1]*STMicroelectronics, France*
[2]*IMEP-LAHC, France*

Y function is well known to overcome the influence of source/drain series resistance (Rsd) in MOSFETs. In this work we present a new methodology for drain current local variability characterization using Y function method. Thus, we demonstrate that the use of Y function statistical variability permits the extraction of Vt and β variability without the influence of Rsd values and the deduction of Rsd variability contribution to the to global drain current variability in strong inversion regime.

5.3 A Novel BJT Structure for High-Performance Analog Circuit Applications

Seon-Man Hwang, Hyuk-Min Kwon, Jae-Hyung Jang, Ho-Young Kwak, Sung-Kyu Kwon, Seung-Yong Sung, Jong-Kwan Shin, Jae-Nam Yu and Hi-Deok Lee
Chungnam National University, Korea

A novel structure is proposed to improve the matching characteristics of bipolar junction transistor (BJT) based on CMOS technology for high performance analog circuit applications. This paper includes the analysis of electrical and matching characteristics in collector current density (JC), base current density (JB) and current gain (β). Although the collector current density JC of the proposed structure is similar to that of the conventional structure, the base current density JB is lower than that of conventional structure, which results in higher current gain. The matching characteristics of the collector current density and the current gain of the proposed structure showed improvement of about 12.22% and 36.43%, respectively compared with the conventional structure.

5.4 Reconsideration of the Threshold Voltage Variability Estimated with Pair Transistor Cell Array

Kazuo Terada, Naoya Higuchi and Katsuhiro Tsuji
Hiroshima City University, Japan

The standard deviation of threshold voltage, σVTH, which is estimated with Pair Transistor cell Array (PTA), is examined using the test chip fabricated by 65-nm technology. It is found that the errors are caused by two problems: (1) the problem in the approximation and (2) leak current in the isolation region. Taking them into account, the application of PTA to the test structure in scribe line is studied.

10:20 – 10:50 Break

SESSION 6: Thermal and Power

10:50 – 12:10

Co-Chairs: Satoshi Habu, *Agilent Technologies Japan, Japan*
Stewart Smith, *University of Edinburgh, UK*

6.1 Comparison of Electrical Techniques for Temperature Evaluation in Power MOS Transistors

A. Ferrara[1], P.G. Steeneken[2], K. Reimann[2], A. Heringa[3], L. Yan[3], B.K. Boksteen[1], M. Swanenberg[2], G.E.J. Koops[3], A.J. Scholten[2], R. Surdeanu[3], J. Schmitz[1], R.J.E. Hueting[1]
[1]*University of Twente, Netherlands*
[2]*NXP Semiconductors, Netherlands*
[3]*NXP Semiconductors, Belgium*

Three electrical techniques (pulsed-gate, AC-conductance and sense-diode) for temperature evaluation in power MOS transistors are experimentally compared. On wafer measurements are performed on an SOI-LDMOS transistor design with embedded sense-diodes in the center and at the edge of the device. As a result, guidelines for the choice of the most adequate technique are provided.

6.2 Measurement and Investigation of Thermal Properties of the On-Chip Metallization for Integrated Power Technologies

Martin Pfost[1], Cristian Boianceanu[2], Dan-Ionuţ Simon[2], and Sebastian Sosin[2]
[1]*Reutlingen University, Germany*
[2]*Infineon Technologies, Romania*

Test structures to determine the influence of the metallization in integrated power technologies with pronounced self-heating are presented and variants with different metal layers and via configurations investigated. The measurement results are supported by numerical simulations, giving valuable insights into the heat flow and cooling capability of the on-chip metallization.

6.3 Investigation on Safe Operating Area and ESD Robustness in a 60-V BCD Process with Different Deep P-Well Test Structures

Chia-Tsen Dai and Ming-Dou Ker
National Chiao-Tung University, Taiwan

Safe operating area (SOA) is one of the noticeable reliability concerns for power MOSFETs during the normal circuit operating conditions. Besides, electrostatic discharge (ESD) reliability is another important reliability issue for the power IC products. To save the layout area of power IC with high-voltage (HV) devices, it is preferable for HV MOSFET to be self-protected without any additional ESD protection device, and to behave wide SOA region. In this work, the impact of deep P-Well (DPW) structure to the electrical SOA (eSOA) and ESD robustness of HV MOSFET has been investigated in a 0.25-μm 60-V BCD process. DPW structure is used to implement the RESURF (reduced surface field) in MOSFET to make it be able to sustain the high operating voltage. From the experimental results in silicon chip, the ESD robustness and wide eSOA of HV MOSFET can be improved by the modified DPW structure.

6.4 A Test Structure for Analysis of Temperature Distribution in CMOS LSI with Sensing Device Array

T. Matsuda[1], H. Hanai[1], H. Iwata[1], D. Kondo[1], T. Hatakeyama[1], M. Ishizuka[1], and T. Ohzone[2]
[1]*Toyama Prefectural University, Japan*
[2] *Dawn Enterprise, Japan*

A test structure for analysis of temperature distribution in CMOS LSI is presented. Fundamental thermal properties of LSI chip were measured and discussed with simulation results. The test structure consists of 24 sensor blocks, each of which has a resistor as an on-chip heater, a p-n diode array for temperature sensing

and selector switches. Dependence of heating time and distance from the resistor were analyzed as well as transient phenomena. The test structure can provide an effective methodology for analysis of fundamental thermal properties in LSIs packaged in various ways.

12:10 – 13:40 Lunch

13:40 – 13:50 ICMTS 2014 Presentation

SESSION 7: Parameter Extraction

13:50 – 15:10

Co-Chairs: Luca Selmi, *University of Udine, Italy*
Colin McAndrew, *Freescale Semiconductor, USA*

7.1 Analysis of Narrow Gate to Gate Space Dependence of MOS Gate-Source/Drain Capacitance by Using Contact-less and Drawn-out Source/Drain Test Structure

Yasuhisa Naruta and Shigetaka Kumashiro

Renesas Electronics Corporation, Japan

A new test structure which can provide voltage to the very narrow source/drain region between adjacent gates by drawing out the source/drain silicide layer has been developed. By using the test structure, the dependence of the gate-drain capacitance (Cgd) on the gate-gate space (Lsp) has been successfully measured until the minimum gate pitch where no contact can be placed. Decrease of Cgd with respect to the decrease of Lsp has been observed and its main cause is identified as the decrease of the gate-drain overlap length.

7.2 Three- and Four-Point Hamer-type MOSFET Parameter Extraction Methods Revisited

Kjell O. Jeppson

Chalmers University of Technology, Sweden

In this presentation three-point Hamer type and four-point Karlsson & Jeppson type MOSFET parameter extraction is revisited concerning selection of data points and method robustness. The method for fitting models described by rational functions to measured data proposed by Hamming is also discussed and it is shown how this method calculates its weighted data points. An alternative method where MOSFET resistance values are used instead of current values for the extraction procedure is also investigated in an attempt to increase extraction method robustness. Finally, it is shown how the three point extraction method can be applied not only to the triode region but also to the MOSFET saturation region for separating parameters for the body effect and the velocity saturation.

7.3 Die-to-Die and Within-Die Variation Extraction for Circuit Simulation with Surface-Potential Compact Model

Y. Ohnari, A.A. Khan, A. Dutta, M. Miura-Mattausch, and H. J. Mattausch

Hiroshima University, Japan

A 65nm CMOS TEG for die-to-die and within-die variation analysis is reported. From measured Vth and Ion variation data of transistor pairs, die-to-die and within-die microscopic-parameter variations of a surface-potential model are extracted. Consideration of only five microscopic parameters is found sufficient to capture the channel-length dependence of these variations.

7.4 BSIM4 Parameter Extraction for Tri-gate Si Nanowire Transistors

Chika Tanaka, Masumi Saitoh, Kensuke Ota, and Toshinori Numata

Toshiba Corporation, Japan

We investigated the BSIM4 parameter extraction procedure for tri-gate Si nanowire transistors with different geometries and fabrication processes using measurement data. Dependence of source/drain parasitic resistances on transistor geometry and fabrication process can be observed on the extracted parameters. Single sets of parameters can reproduce I-V characteristics with L_g down to 35nm.

15:10 – 15:40 Break

SESSION 8: Emerging Technologies

15:40 – 17:00

Co-Chairs: Anthony J. Walton, *University of Edinburgh, UK*

Bill Verzi, *Agilent Technologies, USA*

8.1 Benchmarking of a Surface Potential Based Organic Thin-Film Transistor Model against C10-DNTT High Performance Test Devices

T. K. Maiti, T. Hayashi, H. Mori, M. J. Kang, M. Miyake, T. Iizuka, K. Takimiya, M. Miura-Mattausch, and H. J. Mattausch

Hiroshima University, Japan

In this paper, a surface potential based compact model for organic thin-film transistors (OTFTs) including both tail and deep trap states across the band gap is presented and benchmarked against measured data from high-performance 2,9-didecyl-dinaphtho [2,3-b:2',3'-f] thieno [3,2-b] thiophene (C10-DNTT) based test devices. This model can accurately describe the OTFT test-structure current from week to strong inversion regime.

8.2 Electrical and Mechanical Characterization of a Large-area All-printed Organic Transistor Active Matrix with Floating-gate-based Non-uniformity Compensator

Tsuyoshi Sekitani, Tomoyuki Yokota, Takeyoshi Tokuhara, Naoya Take, and Takao Someya

University of Tokyo, Japan

We report electrical and mechanical characterizations of a large-scale, all-printed, ultraflexible organic transistor active matrix on 10-μm thin-film plastic substrates. The printed active matrix comprising printed floating-gate organic transistors have been manufactured utilizing high-definition screen-printing and inkjet-printing. By applying feedback control to the threshold voltages of the floating-gate organic transistors, the circuit can compensate the device-to-device non-uniformity, which is less than 5%. The 230×230 mm2printed active matrix circuit comprises 200×200screen-printed organic transistor cells, and the periodicity is 1.0mm. Because the circuit's substrate is made of 10-□m thin-film, critical bending radii of less than 0.5 mm are achieved.

8.3 Greek Cross Test Structures for Ink Jet Printed Electronics

Elkin Díaz, Eloi Ramon, and Jordi Carrabina

Universitat Autònoma de Barcelona, Spain

This paper reports on usage of Greek cross test structure to characterize inkjet printed electronics circuits. Geometric characteristics extracted from optical characterization can be correlated with electric measurements for square resistance. Design of inkjet printed Greek cross test structure should compensate or reduce the ink coalescence and coffee ring effects.

8.4 Process Control Monitors for Individual Carbon Nanotube Transistor Fabrication Processes

Kiran Chikkadi, Miroslav Haluska, Christofer Hierold, and Cosmin Roman

ETH Zurich, Switzerland

The manufacturing yield of carbon nanotube transistors is very sensitive to changes in process parameters, while controlling length, density and orientation of nanotubes simultaneously is still proving elusive in batch fabrication processes. Here, we show an electrode design with a yield of up to 45% working transistors despite our batch fabrication process being based on randomly grown nanotubes. Transistor parameter distributions of 765 devices are shown, demonstrating the potential of our design for process monitoring and control.

Thursday, March 28

SESSION 9: Memory

9:00 – 10:20

Co-Chairs: Kazuo Terada, *Hiroshima City University, Japan*

9.1 Automatic Test Methodology to Optimize Operating Conditions and Reliability of Conductive Bridge RAM

A. Toffoli, E. Vianello, G. Molas, L. Perniola, B. De Salvo, and G. Reimbold

CEA- LETI, France

To evaluate CBRAM technologies, we have implemented test structures including 1T1R cells both single and in array NOR configuration. Appropriated test sequences are combined, to investigate forming, seasoning and endurance phases. Voltages and pulse widths scans are used to investigate and adjust

programming parameters, and then smart controlled LRS and HRS cycling explore endurance performances. 1T1R Cells and Matrix test structures offer both quick and high statistical results to evaluate technologies robustness for various applications.

9.2 A Proper Approach to Characterize Retention-after- Cycling in 3D-Flash Devices

Fengying Qiao[1], Antonio Arreghini[2], Pieter Blomme[2], Geert Van den bosch[2], Liyang Pan[1], Jun Xu[1] and Jan Van Houdt[2]
[1]*Tsinghua University, China*
[2]*IMEC, Belgium*

We propose a procedure to evaluate retention-after- cycling in 3D-flash devices. The observed ID-VG degradation is compensated by a relaxation phase, consisting in baking samples for 24 hours at 200 ºC. The relaxation anneals interface traps and promotes lateral redistribution of charges, allowing proper extraction of device VT and hence more relevant comparison of retention before and after cycling.

9.3 A Novel Test Structure to Implement a Programmable Logic Array Using Split-Gate Flash Memory Cells

Henry Om'mani, Mandana Tadayoni, Nitya Thota, Ian Yue, and Nhan Do
Silicon Storage Technology, USA

We developed a novel configurable logic array test structure using a highly scalable 3rd generation split-gate flash memory cell that features low power and fast configuration time. This split-gate SuperFlash® configuration element (SCE) has been demonstrated with a 90nm embedded flash technology. The resulted SCE eliminates need for esoteric fabrication process, sense, and SRAM circuits and reduces configuration time for programmable array (PA) like FPGAs and CPLDs. Additionally, SCE ports inherent the advantages of SST's split-gate flash memory technology with compact area, low voltage read operation, low power poly-to-poly erase and source-side channel hot electron (SSCHE) injection programming mechanisms, and superior reliability.

9.4 On-wafer Integrated System for Fast Characterization and Parametric Test of New-Generation Non Volatile Memories

Erika Covi[1], Alessandro Cabrini[1], Loris Vendrame[2], Luca Bortesi[2], Roberto Gastaldi[2], and Guido Torelli[1]
[1]*Università di Pavia, Italy*
[2]*Micron Semiconductor Italia, Italy*

In new and future generations of Non Volatile Memories such as Phase Change Memories and Resistive-RAMs, having accurate and controllable program pulses is fundamental to adequately characterize the memory cell, since the obtained cell status is a function of the applied pulse parameters. In order to massively test new cells and enhance the conventional instrumentation flexibility, an accurate on-chip pulse generator, able to provide pulses with different amplitude, falling time, and duration, has been designed and experimentally evaluated.

10:20 – 10:40 Break

SESSION 10: Arrays and Ring Oscillators

10:40 – 12:00

Co-Chairs: Tsuyoshi Sekitani, *University of Tokyo, Japan*
Christopher Hess, *PDF Solutions, USA*

10.1 Tr Variance Evaluation induced by Probing Pressure and its Stress Extraction Methodology in 28nm High-K and Metal Gate process

T. Okagaki, T. Hasegawa, H. Takashino, M. Fujii, A. Tsuda, K. Shibutani, Y. Deguchi, M. Yokota, and K. Onozawa
Renesas Electronics Corporation, Japan

We discuss characteristics variance in detail, caused by probing stress in 28nm High-K and Metal Gate process. The Vth variation of nch large size transistor increases by 20% comparing with weak probing pressure(~0). Regarding small size transistors, probing stress impact both on Vth fluctuation and on Tpd fluctuation is small. Moreover, we extracted the space distribution of probing stress quantitatively. It is useful to calibrate a stress simulation methodology and to facilitate evaluation of the mechanical strength of the material.

10.2 Efficient Technique for Si Validation of Level Shifters

Puneet Sharma, Brad Smith, Donald Hall, Mike Nelson and Umesh Lohani
Freescale Semiconductor India, India

This paper presents a new structure of addressable parametric array to validate level shifter cells. Presented structure is very area efficient and allows direct measurement of input & output voltages. Experimental data confirmed the utility of this approach, validating level shifters in three different power domains including source biasing on the same 22 pad design. The simulation result shows good correlation with the measured data. Being a parametric structure enabled direct measurement of the output voltages, a critical parameter for level shifters.

10.3 Mosaic SRAM Cell TEGs with Intentionally-added Device Variability for Confirming the Ratio-less SRAM Operation

Hitoshi Okamura, Takahiko Saito, Hiroaki Goto, Masahiro Yamamoto and Kazuyuki Nakamura
Kyushu Institute of Technology, Japan

MOSAIC SRAM Cell TEGs consisting of memory cells having all combinations of gate sizes of transistors differing by two orders of magnitude were developed with 0.18um CMOS process to verify the operation margins for SRAM circuits. The measured results show the operation of the ratio-less SRAM is completely independent of the size of transistors in the memory cell.

10.4 Characterization and Simulation of NMOS Pass Transistor Reliability for FPGA Routing Circuits

Christopher S. Chen and Jeffrey T. Watt
Altera Corporation, USA

In this work, the impact of bias temperature instability is evaluated for routing pass gate circuits. Measured data is compared to aging models to demonstrate the importance of modeling circuit level aging effects. Aging models which are shown to be accurate at the transistor level are inadequate at the circuit level unless frequency dependent aging effects are taken into account.

12:00 Best Paper Announcement and Closing