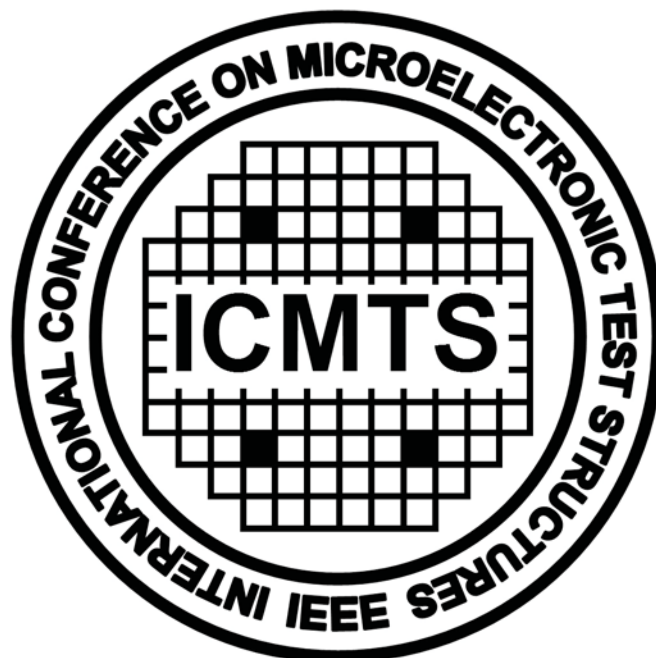
2012 International Conference on Microelectronic Test Structures 2012



25th IEEE ICMTS

!March 19-22, San Diego, USA

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Tutorial Program

09:05 - Introduction to Test Structure Design

Brad Smith

Freescale Semiconductor

This talk will cover the basics of test structure design to measure parameters such as sheet resistance, contact resistance, drive & leakage currents, threshold voltage, capacitance, etc. Emphasis will be placed on how measurement capabilities and process variations influence structure design. Design automation and future trends will also be covered.

10:05 - Why is wafer test and sort such a challenge? ... Fundamentals, Techniques, Trends, and New Ideas

Jerry Broz

International Test Solution

This is a broad tutorial covering key aspects of device testing practices and some of the associated infrastructure requirements (i.e., probe cards, tester hardware, and metrology systems). Advanced and MEMS probe technologies clearly dominate the memory segment; however, the volumes and demands of advanced probe cards for non-memory applications are growing rapidly. Probe requirements driving these test tooling technologies include test requirements, device configurations, good / bad die identification, traditional vs. advanced and MEMs probe technologies, temperature effects, and other factors that can affect cost of test. Various probe related challenges and solutions for reduced probe card repairs, on-line cleaning to maintain high yield and throughput, and damage control will be discussed.

11:05 - A designer's view on component mismatch

Marcel Pelgrom

NXP Semiconductors

Circuit design greatly depends on the ability to control and reproduce transistor and process parameters. Variation in processing was in the past countered by defining process corners. With the improved control over processing, this batch-to-batch variation is largely under control. Statistical variations between otherwise identical

components are generally described by "mis-match" parameters. Analog ICs with differential operation were already heavily affected by mismatch. In today's advanced technologies every circuit from SRAM cell to an I-Q mixer must deal with statistical variations.

13:25 - Characterization of Transistor Variability and Leakage in Nanometer Scale CMOS Technologies

Sharad Saxena

PDF Solution Inc

Transistor performance variation and leakage are some of the most critical challenges to the development and effective utilization of nanometer scale CMOS technologies. This tutorial will describe various sources of transistor variation and techniques for effective characterization of these sources of variation. Topics covered will include design of experiment (DOE) considerations for statistically valid characterization, efficient test structures, test hardware and algorithms, analysis of large volumes of data produced by variability characterization test chips. Case studies to illustrate the methodology and its applications will also be discussed.

14:25 - Test structures for placement on CMOS products & test vehicles

Manjul Bhushan

IBM

In this tutorial the design and utilization of test structures embedded in CMOS product chips will be described. These test structures provide valuable data for evaluating product performance and bridging it to the technology models and process variability in the manufacturing line. Performance, thermal and noise data are collected during product testing for sorting and reliability assessment and from products deployed in the field. Constraints on the available I/O's, power supply voltages, silicon space and interface to the testers used for product testing are easily met for certain types of test structure designs such as ring oscillators. For analog measurements on resistors and MOSFETs, additional circuitry and I/O's are required. Ideally, identical designs are placed on test vehicles and in scribe lines of product chips to assist in correlating the product data to the data collected in the silicon manufacturing line. Design and measurement strategies for meeting the requirements of different form factors, electrical interfaces, and test platforms for product and scribe line test structures will be covered. Placement and location of the test structures on silicon, test time minimization as well as simple data analysis techniques to provide rapid feedback will also be discussed.

15:25 - Characterization Techniques and Useful Test Structures for Evaluating Multi-gate FETs

Chadwin Young

SEMATECH

Multi-gate Field Effect Transistors (MugFETs) in a three-dimensional (3-D) configuration have garnered much attention recently. MugFETs can be fabricated on silicon-on-insulator (SOI) or bulk silicon, and they are especially attractive because their 3-D “fin” structure enables substantial immunity to short channel effects, without significant changes to conventional CMOS fabrication techniques. One MugFET design of interest is known as the FinFET, where a hard mask can be placed on the top surface of a fin structure to decouple it from the sidewall device operation. FinFETs can be fabricated with either the (110) sidewall surface or (100) sidewall where the crystal orientation of the fin sidewalls can have an impact on performance and reliability. These surface orientations or the fin structure itself may be more susceptible to performance enhancement or reliability degradation during stress. In addition, these devices will have to scale – just as silicon planar technologies – in order to meet future performance targets. Therefore, various test structures are required to investigate the pending implications of these devices for future technology nodes. This tutorial will focus on how test structures are used to determine and understand parameter extraction and physical phenomena of 3-D FinFET device structures.

16:25 - An introduction to 3D test structures

Daniel Perry

Qualcomm

3D chip stacking offers opportunities for improved performance, lower power, and better form factor, and also provides many new challenges for technologists. Integration of TSVs (Through Silicon Vias) into advanced CMOS processes, thinning of silicon to 10s of microns, and stacking thin die in very close proximity are disruptive to standard process flows and require careful study to understand the risks to future products. In this tutorial, the author will present a brief overview of 3D processing, unique test challenges of 3D test structures, and a high level overview of the test structures used to characterize the 3D chip stacking process. Test structures to be discussed include TSV and backside metal characterization, FET proximity to TSV, packaging impact to thin die, TSV process interaction, thermal characterization, yield, and reliability.

Technical Program

Tuesday March 20

08:00 - 08:45 Registration and Continental Breakfast

08:45 - 08:55 Welcome

08:55 - 10:15 Session 1 - Design Margin

Co-Chairs:

Christopher Hess	PDF Solution Inc., USA
Emilio Lora-Tamayo	Universitat Autònoma de Barcelona, Spain

[1-1] Ring Oscillator with Calibration Circuit for Accurate On-Chip IR-drop Measurement

Shinichi Nishizawa [1] and Hidetoshi Onodera [1,2]

[1]Graduate School of Informatics, Kyoto University, Yoshida-honmachi, Sakyo-ku, Kyoto 606-8501, JAPAN
[2]JST, CREST

In this paper, we propose a test structure for in-situ measurement of IR-drop over a power distribution network(PDN) which has been developed for verifying the accuracy of a PDN simulation model that includes on-chip network as well as off-chip parasitics.

[1-2] Calibration of Library element Optimization to improve Static Power

Venkat Kolagunta[2], Savithri Sundareswaran[1], Puneet Sharma[1], Donald Hall[1], Matthew A. Thompson[3],Brad Smith[1], Surya Veeraraghavan[1]

[1]Freescale Semiconductor, 7700 W. Parmer Lane, Austin, TX USA
[2]Global Foundries, 400 Stone Break Extension, Malta, NY USA
[3]PO Box 170489, Austin, TX USA

This paper demonstrates the application of ring oscillators to calibrate the physical layout optimization to improve performance and/or reduce standby power of library elements. Standby power consumption on library elements can be halved at very little performance penalty and is demonstrated in both silicon and simulations.

[1-3] A Novel Structure of MOSFET Array to Measure Off-Leakage Current with High Accuracy

Hidetoshi Oishi, Tsuyoshi Suzuki, Masaaki Bairo, Shigetaka Mori, Kazuhisa Ogawa and Hidetoshi Ohnuma

Semiconductor Technology Development Division, Core Device Development Group, R&D Platform, Sony Corporation
4-14-1, Asahi-cho, Atsugi-shi, Kanagawa, 243-0014, Japan

We develop a new test structure of MOSFET array with accurate off-leakage current (Ioff) measurement. The features of the structure are that each source and drain of MOSFET is connected to probing pad directory and that the combination of source and drain pads is unique for all MOSFETs to avoid Ioff contamination by unselected MOSFETs. This test structure is implemented in scribe line for 90nm technology and beyond, and is achieved good correlations of MOSFET characteristics between the array and non-array. In addition, MOSFETs in the array can be placed by 13 times higher density than that of non-array.

[1-4] A Universal Test Structure for the Direct Measurement of the Design Margin of Even-Stage Ring Oscillators with CMOS Latch

Yutaka Hirakawa, Ayami Motomura, Kohei Ota, Norihiro Mimura, Kazuyuki Nakamura

Center for Microelectronic Systems, Kyushu Institute of Technology
680-4 Kawazu, Iizuka, Fukuoka 820-8502, Japan

To validate our optimized design theory for Even Stage Ring Oscillators (ESRO), we have developed a Universal ESRO TEG (U-ESRO TEG) constructed with Equivalent Variable-W Transistors (EVWTs) and Initial-voltage Preset-able Inverters (IPIs). The design parameters can be changed with a single circuit, and it is possible to measure the operation margin and oscillation availability of an ESRO. Experimental results confirm the validity of our ESRO design theory.

10:15 - 10:45 Break

10:45 - 11:45 Session 2 - Variability

Co-Chairs:

Colin McAndrew	Freescale Semiconductor, USA
Antoine Cros	STMicroelectronics, France

[2-1] Inhomogeneous Ring Oscillator for WID Variability and RTN Characterization

Shuichi Fujimoto[1], Islam A.K.M Mahfzul[1], Takashi Matsumoto[1], and Hidetoshi Onodera[1,2]

[1]Graduate School of Informatics, Kyoto University
[2]JST, CREST

We propose an inhomogeneous ring oscillator (RO) whose performance is strongly influenced by a small set of transistors for characterizing transistor-bytransistor variability. Performance sensitivities of the transistors are enhanced by inserting a "singular point" into a homogeneous RO. Proposed ROs have been embedded into a 65nm RO-array test structure, and it is verified that the proposed ROs are highly sensitive to Within-Die local variability and Random Telegraph Noise.

[2-2] Addressable Test Structures for MOSFET Variability Analysis

Sunil Chitrashekaraiah, Shenglong Guo, Rainer Herberholz, David Vigar, Mark Redford[1]

CSR ltd, Churchill House, Cambridge, CB4 0WZ, United Kingdom
[1]CSR Technology Inc, 217 Devcon Drive, San Jose, CA, USA

Aggressive scaling of CMOS transistor has increased variations in threshold voltages, drive currents and gains. Circuits are expected to meet performance targets, which require detailed knowledge of variability to enable less pessimistic design methodologies. This paper presents a 4-bit addressable array-based test structure with a centre reference transistor allowing evaluation of variability in advanced technologies.

[2-3] Test Structures for Interdie Variations Monitoring in Presence of Statistical Random Variability

Giancarlo Castaneda[1,2], André Juge[1], Gérard Ghibaudo[2], Dominique Golanski[1], David Hoguet[1], Jean-Michel Portal[3], Bertrand Borot[1]

[1]STMicroelectronics 850, rue Jean Monnet, 38926 Crolles, France
[2]IMEP_LAHC, Minatec, INPG, 3, Parvis Louis Néel, BP257, 38016 Grenoble, France
[3]IM2NP IMT Technopole de Château Gombert France, 38, rue Joliot Curie, 13451 Marseille, France

We study the limitations of single transistor test structures for Process variations monitoring in presence of statistical random variability, and compare them with transistor array structures in 45 CMOS technology. By optimizing transistor array design considering statistical variability, layout effects, and interconnect parasitic, we first estimate and then verify on silicon that x5 reduction of statistical variability and excellent correlation with ring oscillator frequency can be reached for array structure.

Transistor arrays are demonstrated well suited for monitoring impact of process variations, whether die-todie, or wafer-to-wafer.

11:45 - 12:15 Exhibitor Presentation

12:15 - 13:45 Lunch

13:45 - 15:25 Session 3 - MEMS

Co-Chairs:

Yoshio Mita	University of Tokyo, Japan
Greg M. Yeric	ARM, USA

[3-1] Piezoresistive membrane deflection test structure for the evaluation of hermeticity in low cavity volume MEMS and microelectronic packages

S. Costello[1], M.P.Y. Desmulliez[1], S. McCracken[2], C. Lowrie[1], S. Cargill[1] and A.J. Walton[3]

[1]MIcroSystems Engineering Centre (MISEC), Institute for Integrated Systems (IIS), School of Engineering and Physical Sciences, Heriot-Watt University, Edinburgh, EH14 4AS, Scotland, U.K.
[2]MCS Ltd., Centre House, Midlothian Innovation Centre, Roslin, Midlothian, EH25 9RE, Scotland, U.K.
[3]Scottish Microelectronics Centre, Institute of Integrated Systems (IIS), School of Engineering, The University of Edinburgh, King's Buildings, Edinburgh, EH9 3JF, Scotland, UK.

This paper details the design, fabrication and characterisation of a piezoresistive membrane deflection test structure for theelectrical evaluation of hermeticity in low cavity volume package. This test structure uses the 0-level silicon cap as a deflecting-membrane to electrically monitor changes in package cavity pressure over time. The hermeticity of the package can then bedetermined in real-time and low leak rates can be measured using a pressurisation stage, which also accelerates the test. Theminimum detectable leak rate of the test structure without acceleration is 6.9×10-12 atm.cm3.s-1, which is two orders of magnitudelower than the limit of traditional helium fine leak test.

[3-2] A Diaphragm based Piezoelectric AlN Film Quality Test Structure

Nathan Jackson[1], Rosemary O'Keeffe[1], Robert O'Leary[1], Mike O'Neill[2], Finbarr Waldron[1], Alan Mathewson[1]

[1]Tyndall National Institute, University College Cork, Cork, Ireland
[2] Analog Devices Inc., Limerick, Ireland

Piezoelectric AlN is a commonly used material because of its unique properties and its CMOS compatibility. However, obtaining "good" quality c-axis oriented AlN is far from trivial, and typically requires multiple testing structures. Important factors for obtaining high quality AlN include: crystal orientation, piezoelectric constants, material thickness, alignment, and dielectric constant. This paper highlights a diaphragm test structure which allows all of these parameters to be measured, in order to determine the quality of the AlN film.

[3-3] A novel high-throughput on-wafer electromechanical sensitivity characterization system for piezoresistive cantilevers

G. Tosolini[1], L. G. Villanueva[2], F. Perez-Murano[1] and J. Bausells[1]

[1]Instituto de Microelectrónica de Barcelona IMB-CNM (CSIC), 08193 Bellaterra, Spain
[2]California Institute of Technology, Pasadena, CA, USA

Performing fast, accurate and repeatable mechanical, electrical and electromechanical characterization of the device properties for new piezoresistive MEMS is necessary in order to prove the reliability of the sensor and to validate the fabrication technology in view of future commercial applications. In this work we present the development of a new set up that allows on?wafer properties characterization reducing considerably the testing time.

[3-4] Modification and Characterisation of Material Hydrophobicity for Surface Acoustic Wave Driven Microfluidics

H. Zou, Y. Li, S. Smith, A.S. Bunting, A.J. Walton and J.G. Terry

Institute for Integrated Micro and Nano Systems (part of the Joint Research Institute for Integrated Systems), School of Engineering, The University of Edinburgh
Scottish Microelectronics Centre, The King's Buildings, Edinburgh, EH9 3JF, UK

Surface acoustic waves (SAW) generated in a piezoelectric substrate may be used to manipulate micro-scale droplets of liquid in a digital microfluidic system for lab-on-a-chip applications. The wettability of the surface over which a droplet is driven determines the ease and speed with which the droplet is propelled. This provides the opportunity to achieve fine control of SAW driven droplets simply by patterning of the surface into areas with different levels of wettability. This paper evaluates a number of different materials and surface preparation techniques and assesses their manufacturability and efficacy for thisapplication. Test structures have been designed and developed to help optimise a fabrication process using the biocompatible polymer Parylene. Early results obtained using airflow as a driving force show that it is possible to manipulate droplets through direction changes of up to 40°. Future work will use surface acoustic waves as the driving force to determine the extent to which droplets can be guided to desired locations.

[3-5] A Blur-Range Test Structure of Collimation-Controller-Integrated Silicon Shadow Mask for Three-Dimensional Surface Patterning with Sputtering

Satoshi Morishita, Masanori Kubota, and Yoshio Mita

Department of Electrical Engineering and Information Systems, The University of Tokyo, Tokyo, Japan

We propose a test structure for development of collimation-controller-integrated three-dimensional shadow mask to control pattern blurs by isotropic deposition such as sputtering. The collimator was intelligently employed to both suppress and intentionally introduce the blurring, depending on the substrate position. Consequently, we have successfully patterned Titanium electrodes over 225?m-deep, 720?m-wide trenches by 15?m-wide gaps, which have not been obtainable with standard 3-D shadow mask. The purpose of the test structure is to quantify blurring range by collimator to optimize its aperture widths by mask design. Clear relationship between blur-range and the gap was observed and shown to be predictable by its geometry (similitude of triangles).

15:25 - 15:55 Break

15:55 - 17:00 Session 4 - Poster

Co-Chairs:

Anthony J. Walton	University of Edinburgh, UK
Hi-Deok Lee	Chungnam Nat. University, Korea

[4-1] Study on Device Matrix Array Structure for MOSFET gm Variability Evaluation

Kazuo Terada[1], Ryo Takeda[1], Katsuhiro Tsuji[1], Takaaki Tsunomura[2], Akio Nishida[2] and Tohru Mogami[2]

[2]Faculty of Information Sciences, Hiroshima City University, 3-4-1, Ozuka-Higashi, Asa-Minami-Ku, Hiroshima, 731-3194, JAPAN
[2]MIRAI-Selete, 16-1, Onogawa, Tsukuba, Ibaraki 305-8569, JAPAN

The effect of the DMA (Device Matrix Array) structure on MOSFET gm-variability measurement is studied. By removing the transfer gate for the force terminal of the source electrode, the effect of the metal wiring resistance on Kelvin measurement can be measured and reduced. Taking them into account, we tried to extract the intrinsic MOSFET gm-variability from the measured current data.

[4-2] A Proposition on Test Circuit Structures Using Selectively Metal-Covered Transistors for a Laser Irradiation Failure Analysis

Hiroshi Hatano

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Shizuoka Institute of Science and Technology, Fukuroi-city, Shizuoka, 437-8555 Japan

A quick and easy laser experiment for photocurrent induced failure investigations has been described as a preliminary test method for single-event effect experiments. In order to focus a laser beam on a desired transistor in complex LSI circuits, novel test circuit structures using selectively metal-covered transistors have been proposed. Photocurrent induced failures have been successfully observed in a target CMOS inverter with an SR-FF detector. The laser irradiation failure has also been successfully observed in a selectively metal-covered CMOS SRAM test cell.

[4-3] Threshold Voltage Variation Extracted from MOSFET C-V Curves by Charge-Based Capacitance Measurement

Katsuhiro Tsuji[1], Kazuo Terada[1], Ryo Takeda[1],Takaaki Tsunomura[2], Akio Nishida[2] and Tohru Mogami[2]

[1]Faculty of Information Sciences, Hiroshima City University, 3-4-1, Ozuka-Higashi, Asa-Minami-Ku, Hiroshima, 731-3194, JAPAN
[2]MIRAI-Selete, 16-1, Onogawa, Tsukuba, Ibaraki, 305-8569, JAPAN

The threshold voltage variations for the MOSFETs having various channel structures are evaluated from their measured C-V curves. It is found that they show reasonable dependence on the channel structure and are smaller than those evaluated from the current-voltage (I-V) relations. As one of the reasons that the difference of between the variations extracted from C-V curves and those extracted from I-V relations arises, it is considered that the local channel dopant fluctuation increases the current variation. Furthermore, it is found that the evaluated flat-band voltage variations represent the reasonable behavior.

[4-4] Electrical Characterisation of Dry Microneedle Electrodes for Portable Bio-potential Recording Applications

Francesco Pini[1,2], Conor O'Mahony[2] and Kevin G. McCarthy[1]

[1]Dept. of Electrical and Electronic Engineering, University College Cork, Cork, Ireland
[2]Tyndall National Institute, University College Cork, Cork, Ireland

We present the electrical characterisation of an array of pyramidal microneedle structures used as electrodes for bio-potential recording. Test structures are described and implemented in order to measure the electrical parameters of the electrodes, such as impedance and DC offset voltage, and perform in-vivo measurement of bio-potential

signals (ECG, EMG). Results demonstrate the suitability of microneedle electrodes to be used for long-term wearable recording applications.

[4-5] Reliability Analysis of NAND Gates with Modified Channel Length in Series n-MOSFETs

T. Matsuda[1], Y. Tokumitsu[1], H. Hanai[1], H. Iwata[1] and T. Ohzone[2]

[1]Department of Information Systems Engineering, Toyama Prefectural University
[2]Dawn Enterprise, Nagoya, Japan

Reliability of NAND gates with series n-MOSFETs, which have a modified channel length, have been analyzed under voltage stress condition with a test structure of ring oscillator implemented in standard 90 nm CMOS process. Stress time tstrs dependence of degradation ratio of delay time td and operation current IOP follow a power law of tstrs. A channel length modification from 0.10 to 0.11 ?m for the topmost one in series connected n-MOSFETs of NAND gates provides not only leakage current reduction but reliability improvement with less performance degradation under high voltage stress condition.

[4-6] A Novel High Accurate Analytical Technique of the Leak Current for the Product Chip

T. Okagaki, N. Takeshita, S. Tanaka, S. Tateishi, K. Shibutani, T. Tsutsui, H. Abe, M. Yokota, K. Onozawa

Renesas Electronics Corp., 4-1 Mizuhara Itami, Hyogo 664-0005, Japan

We propose the novel technique to analyze the leak current of the product chip accurately. Comparison of calculated and measured leak current proves the validity of this technique. The small variation causation of the product's leak current is able to be analyzed. Moreover, leak current reduction guide is obtained with the detail component factor analysis. Applying to the in-line monitor, all wafers could be an analytical object.

[4-7] Simple Gate Charge (Qg) Measurement Technique for On-Wafer Statistical Monitoring and Modeling of Power Semiconductor Devices

Vijay Krishnamurthy, Alex Gyure, and Pascale Francis

Texas Instruments, Santa Clara, California, USA

Conventional measurement techniques for gate charge (Qg) require large array test-structures and additional circuitry. These techniques do not use standard ET test equipment, require careful calibration, and are expensive in terms of silicon area. Hence they are not amenable to on-wafer measurement. In this paper, we present a simple yet accurate CV method for on-wafer measurement and monitoring of gate

charge. Based on the principle that Q = ∫Idt = ∫CdV, this technique uses small PCM test-structures and basic ET equipment (LCR meter), yet is accurate to within 2

[4-8] Experimental Extraction of Substrate-Noise Coupling between MOSFETs and its Compact Modeling for Circuit Simulation

S. Emoto, T. Miyoshi, M. Miyake, H. J. Mattausch, M. Miura-Mattausch

Graduate School of Advanced Science of Matter, Hiroshima University, Higashi-Hiroshima, 739-8530, Japan

We have developed test structures to experimentally extract the substrate-noise coupling characteristics between MOSFETs. It was found that the noise propagation from the aggressor to the victim can be described on the basis of the small-signal properties observed at the substrate node of the aggressor, a quantity which is usually calculated during circuit simulation. An equivalent circuit was developed to predict the propagated noise intensity. The resulting prediction was verified to be in good agreement with the measured results. These findings consequently enable to include the substrate-noise coupling effect in a simple and effective way during conventional circuit simulation.

[4-9] Quantitative mapping of residual stress in micromachined materials by coupling independent strain and Young's modulus measurements

G. Schiavone[1], M.P.Y. Desmulliez[3], S. Smith[1], J. Murray[1,2], E. Sirotkin[1], J.G. Terry[1], A.R. Mount[2], A.J. Walton[1]

[1]Institute for Integrated Micro and Nano Systems, Joint Research Institute for Integrated Systems, School of Engineering,Scottish Microelectronics Centre, The University of Edinburgh, Edinburgh, UK
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The characterisation of MEMS material properties is of crucial importance for accurate design and fabrication phases during the development of new devices. Stress development within MEMS films, in particular, has been of great interest as it can prove to be detrimental for device performances and reliability. This work focuses on the coupling of previously reported strain measurements from mechanical test structures and new nano-indentation measurements on both micromachined films and cantilevers to obtain quantitative stress maps that can be applied to any micromachined material and can provide a means to monitor residual stress non uniformities due to specific process operations during fabrication.

[4-10] Dynamic Pixel Test Pattern for CMOS Image Sensor

KS Lee, HJ Lee, MJ Jang, JC Kim, ST Kim, JW Moon, IW Cho and KD Yoo

Hynix Semiconductor Inc., San 136-1 Ami-Ri Bubal-Eup Icheon-City, Kyoungi-Do, 467-701, Korea

We propose a dynamic pixel test pattern for CIS (CMOS Image Sensor) to measure the performance of the pixel unit including TX (Transfer Transistor), DX (Amplifier Transistor), RX (Reset Transistor), SX (Select Transistor), FD (floating Diffusion) and PD (Photo Diode). The proposed TP (Test Pattern) was implemented and verified using a 90nm CIS process. The proposed TP has well delivered the expected properties of pixel; blooming, pixel reset level, pixel output signal, pixel signal swing range and TX gate turn on pulse width which can only be guessed for a conventional TP. The measured parameters should help to optimize and improve the CIS

[4-11] Phase Change Memory Advanced Electrical Characterization for Conventional and Alternative Applications

A. Toffoli[1], Manan Suri[1], L. Perniola[1], A. Persico, C. Jahan, J.F. Nodin, V. Sousa[1], B. DeSalvo[1],G. Reimbold[1]

[1]CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 GRENOBLE Cedex 9, France

Research on phase change chalcogenide materials and Phase Change Memory (PCM) devices, is increasing and the recent proposals of alternative applications of PCM such as emulating the biological synapse in future bio-inspired computing systems has led to the need of fast, versatile and accurate solutions for advanced electrical characterization. In this paper, we introduce a new automated test solution capable of handling the requirements of High Frequency (HF) pulses, and DC resistance measurement used to characterize chalcogenide material integrated at the cell level. Improvement in measurement of SET and RESET threshold voltages is confirmed due to increased stability of the access resistance. The improved accuracy of the test system and its ability of fast statistical screening per wafer allow for appropriate characterization of the PCM for both conventional memory applications, and upcoming synaptic plasticity applications.

[4-12] A Novel Compact CBCM Method for High Resolution Measurement in 28nm CMOS Technology

Kin Hooi Dia, Willy Tsao, Cheng Hsing Chien, Zheng Zeng

MediaTek Inc., No. 1, Dusing Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan

Accurate measurement and analysis of interconnect capacitance is a critical component of nanometer technology verification. The Charged-Based Capacitance Measurement (CBCM) technique has been widely adopted as a robust technique to measure

on-chip capacitance test structures.In this paper we present a novel CBCM cell with a zero area overhead on-chip non-overlapping signal generation circuitry to reduce the number of probe pads for the test structure, and to enable the test structure to operate at GHz range. Also, we describe the circuit design technique and measurement calibration to improve the resolution limit in 28nm process technology node. These novel features combine to make it a very suitable for industrial applications for large amounts of accurate capacitance characterizations with a limited layout area. The results confirm the excellence of this test structure in measurement with error sensitivity of 2aF in 28nm process after silicon calibration.

[4-13] 32nm Yield Learning Using Addressable Defect Arrays

Muthu Karthikeyan[1], John Cassels[1], and Lior Arie[2]

[1]IBM Systems and Technology Group, 2070 Route 52, Hopewell Junction, NY, USA
[2]IBM Israel Systems and Technology Lab, Haifa, Israel

An addressable defect array is widely and effectively used as a yield monitor in technology development and early manufacturing. The Shorts and Opens Monitor (SOM) consists of scan-chain input/output, fully stackable DUTs, standard calibration resistors, and a robust periphery design. The SOM results greatly enable characterization of top yield detractors.

17:00 - 17:30 End

17:30 - 19:30 Poster Reception

Wednesday March 21

08:30 - 09:00 Registration and Continental Breakfast

09:00 - 10:40 Session 5 - Process Characterization

Co-Chairs:

Brad Smith	Freescale, USA
Tsuyoshi Sekitani	University of Tokyo, Japan

[5-1] A Test Circuit for Extremely Low Gate Leakage Current Measurement of 10 aA for 80,000 MOSFETs in 80 s

Y. Kumagai[1], T. Inatsuka[1], R. Kuroda[1], A. Teramoto[2], T. Suwa[2], S. Sugawa[1,2] and T. Ohmi[2]

[1]Graduate School of Engineering, Tohoku University, Japan
[2]New Industry Creation Hatchery Center, Tohoku University, Japan

We propose a test circuit which enables us to evaluate statistical characteristics of gate leakage current in a very short time with high accuracy (10-17 – 10-13 A, 87344 samples in 80 s). The measured absolute value of the gate leakage current is verified and the repeatability error is less than 1x10-17 A. Random telegraph signal of the gate leakage current and stress induced leakage current have been evaluated statistically. It is very useful for the development of new gate insulator films for miniaturized MOSFET and tunnel oxide of flash memory.

[5-2] New Evaluation Method of Low-k Dielectric Films by using a Gated PN-junction Diode and a Field MOS Transistor

Yoichi Tamaki, Masaki Ito, Masaru Hashino, and Yoshifumi Kawamoto

Consortium for Advanced Semiconductor Materials and Related Technologies (CASMAT), Tokyo, Japan

We have developed a new test method for evaluating low-k materials. The method is using two kinds of new test structures. One is a modified gated pn-junction diode and the other is a modified field MOS transistor. Three kinds of low-k materials were evaluated by using the test structures, and electrical characteristics for these materials were successfully measured. The advantage of the new method was discussed.

[5-3] A Compact Circuit for Wafer-Level Monitoring of an Operational Amplifier High-Frequency Performance using DC Parametric Test Equipment

Z. G. Sparling, Vance C. Tyree, Nathan Cox, P. Thomas Vernier

MOSIS Service, Information Sciences Institute, Viterbi School of Engineering, University of Southern California, Marina del Rey, USA

A test structure has been developed to permit wafer level measurement of the frequency response of an operational amplifier having a unity gain frequency of the order of 2 GHz using DC measurement equipment. This paper describes the design issues associated with implementing this test structure along with test data obtained from three fabrication runs in 180 nm CMOS.

[5-4] Improved precision methodology for access resistance extraction using Kelvin test structures

Antoine Cros[1], Gérard Morin[1], Giancarlo Castaneda[1,2], François Dieudonné[1], Julien Rosa[1]

[1]STMicroelectronics, Crolles Site, TR&D/STD/TPS/ECR, Crolles, France
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An improved methodology for MOSFETs access resistance extraction using Kelvin test structures is presented. By drastic reduction of the influence of the device stochastic variations, along with improved methodology for sub 50nm technologies, one site fast in-line extraction can be performed with precision, allowing measurement of systematic series resistance variation on wafer and wafer-to-wafer.

[5-5] Correlation of Optical and Electrical Test Structures for Characterisation of Copper Self- Annealing

J. Murray[1], S. Smith[2], G. Schiavone[2], J.G. Terry[2], A.R. Mount[1], A.J. Walton[2]

[1]School of Chemistry, Joseph Black Building, The University of Edinburgh, UK
[2]Institute for Integrated Micro and Nano Systems (part of the Joint Research Institute for Integrated Systems), School of Engineering,Scottish Microelectronics Centre, The University of Edinburgh, Edinburgh, UK

Electro-chemically deposited copper is widely known for its self-annealing properties at room temperature. The change in microstructure and grain growth with time is important for device reliability. This effect has been investigated by measuring the time dependence of sheet resistance and film stress using test structures for the first time. The different phases of self-annealing have been observed for a period of 30 hours. The influence of process parameters such as current density on metallization of electrochemically deposited copper (ECD) and the film characteristics has also been studied.

10:40 - 11:10 Break

11:10 - 12:10 Session 6 - RF

Co-Chairs:

Colin McAndrew	Freescale Semiconductor, USA
Tatsuya Ohguro	Toshiba Corp., Japan

[6-1] In-situ Calibration and Verification Techniques for the Characterization of Microwave Circuits and Devices

Isaac Martinez

Centellax Inc., Santa Rosa, CA, USA

This paper demonstrates the implementation on IC and thin film technology of a very broadband In-situ TRRM calibration and verification techniques adequate for the continuous measurement, characterization and modeling of microwave devices and structures from the low MHz range to V-band frequencies. The integration of calibration and verification structures on the same substrate as the DUT (Device-Under-Test) not only removes the need for extra de-embedding steps but also allows the generation of calibrated planes inside an IC structure and the compensation of non-idealities in the calibration standards. Compensation of the non-idealities of the calibration standards is accomplished by studying the response of the T-check and Beatty standard to variations in the real and imaginary parts of the load standard. Furthermore, once the calibration coefficients are programmed on any commercial VNA system the displayed data is that of the DUT itself which is usually located well beyond the probe-pad interface. Results of calibration, verification and actual measurements on 65nm RF CMOS technology seem to validate the effectiveness of this technique.

[6-2] An Extended De-embedding Method for On-Wafer Components

Yu-Ling Lin[1], Hsiao-Tsung Yen[1], Ho-Hsiang Chen[1], Chewn-Pu Jou[1], Chin-Wei Kuo[1], Min-Che Jeng[1], Fu-Lung Hsueh[1], Chih-Hua Hsiao[2], and Guo-Wei Huang[2]

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[2]Nano Device Laboratories, 9, Creation Rd.1, Science-Based Industrial Park, Hsin-Chu,Taiwan

On-wafer de-embedding method has been proposed for different method up to millimeter-wave (mm-wave) frequency range. An extended de-embedding method for on wafer devices up to 65GHz is proposed. Using Vertical connection of L-2L (VL2L) is presented in this paper, with a calibrated loss tangent value in mm-wave. It shows significant good and accurate results for on-wafer modeling up to 65GHz. VL2L are considered to be a good method for different kind of devices, such as capacitors.

Also, the results by 40nm and 65nm CMOS process and EM simulation are with good agreement.

[6-3] Development of a Novel System for Characterizing MOSFET Noise in Higher Frequency Regimes

Kenji Ohmori[1,2], Ryu Hasunuma[1,2], and Keisaku Yamada[1,2]

[1]Graduate School of Pure and Applied Sciences, University of Tsukuba, 1-1-1 Tennnodai, Tsukuba, Ibaraki, Japan
[2]JST-CREST, Japan

We present a novel approach for measuring high-frequency components of MOSFET noise under DC bias. For this purpose, a probe card equipped with a preamp has been devised so that the signal of drain current can be amplified with lesser loss. Using the probe card, we have successfully demonstrated that the noise property of MOSFET up to 20 MHz at the present moment. This approach will enable us to understand the device reliability under practical high-speed operations.

12:10 - 12:20 ICMTS 2013

12:20 - 13:50 Lunch

13:50 - 15:30 Session 7 - Parameter Extraction

Co-Chairs:

Kjell Jeppson	Chalmers University of Technology, Sweden
Kevin McCarthy	University College Cork, Ireland

[7-1] Very low frequency noise characterization of semiconductor devices

Hans Tuinhout, Adrie Zegers-van Duijnhoven and Anco Heringa

NXP Semiconductors - Central R&D, Eindhoven, The Netherlands

This paper presents a technique for measuring low frequency noise of semiconductor devices down to below 1 mHz. The technique is based on direct Fourier analysis of “DC” measurements of a bench-top semiconductor parameter analyzer, without using any additional instrumentation hardware like low-noise amplifiers, low-pass fil-ters or signal analyzer.

[7-2] Improved Procedure to Extract the Limiting Carrier Velocity in Ultra Scaled CMOS devices

P. Toniutti[1,2], R. Clerc[2], P. Palestri[1], C. Diouf[3], A. Cros[3], D. Esseni[1], F. Boeuf[3], G. Ghibaudo[2] and L. Selmi[1]

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[2]IMEP-LAHC, MINATEC, Grenoble, France
[3]ST-Microelectronics, Crolles, France

The validity of a previously published extraction technique for the limiting carrier velocity in nano-MOSFETs is examined by means of accurate Multi Subband Monte Carlo transport simulations. By comparing the extracted limiting velocity to the calculated injection velocity, we identify the sources of error of the extraction method. Then, we propose a new extraction method and extensively validate it. Our simulations and experimental results reconcile the values and trends of the extracted limiting velocity with the expectations stemming from quasi ballistic transport theory.

[7-3] Compact Thermal-Interaction Model for Dynamic within Chip Temperature Determination by Circuit Simulation

K. Matsuzawa, T. Iizuka, S. Yamaguchi, T. Hoshida, A. Kinoshita, T. Arakawa

Semiconductor Technology Academic Research Center, Shin-Yokohama, Kanagawa, 222-0033, Japan

We report an equivalent circuit for capturing the thermal propagation from a heat source, creating thermal energy by the self-heating effect, to other devices during circuit operation. It is verified that the equivalent circuit reproduces measured transient thermal propagation characteristics for different layouts. The test structures are also applied to extract the magnitude of the elements included in the equivalent circuit.

[7-4] Self-heating Parameter Extraction of Power MOSFETs Based on Transient Drain Current Measurements and on the 2-cell Self-heating Model

Risho Koh and Takahiro Iizuka

Technology Development Unit, RENESAS Electronics, 1753, Shimonumabe, Nakahara-ku, Kawasaki, Kanagawa, Japan

Self-heating parameter extraction for circuit simulation model is discussed based on the transient drain current measurement, by using a 18V power MOSFET as a test device. The fitting errors in the conventional one-cell self-heating model has been investigated and the influences of the spread resistance on the transient current are discussed to refine the modeling strategy. A simple two-cell model is also proposed and its excellent fitting capability for wide time ranges is demonstrated.

[7-5] Parameter Extraction for Relaxation-Time Based Non-Quasi-Static MOSFET Models

Zeqin Zhu[1], Colin C. McAndrew[2], Ik-Sung Lim[2] and Gennady Gildenblat[1]

[1]School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA
[2]Freescale Semiconductor, Tempe, AZ, USA

This paper presents a new extraction technique for non-quasi-static (NQS) delay time and gate resistance for relaxation-timeapproximation based MOS transistor models. The technique is based on analysis of ydg in strong inversion, as a function of both VGS and frequency, for VDS = 0. An effective delay eff is computed from measured data, and a plot of eff versus the theoretical NQS-only delay allows the NQS relaxation time parameter and the gate resistance to be determined self-consistently.

15:30 - 16:00 Break

16:00 - 17:00 Session 8 - Stress

Co-Chairs:

Stewart Smith	University of Edinburgh, UK
Kazuo Terada	Hiroshima City University, Japan

[8-1] Evaluation of Dynamic Bonding Stress and Interlayer Cracking using a Combo Sensor

Yoshihiko Miki, Hirobumi Watanabe

Corporate Technology Development Group, Ricoh Co., Ltd., 13-1, Himemuro-cho, Ikeda-city, Osaka, Japan

Crack defect in the interlayers of semiconductor chips due to assembly stress can be a serious problem. To analyze the crack-generating stress, we fabricated a combo sensor that enables simultaneous evaluation of stress and cracking under the bonding pad. Dynamic analysis of the bonding process with this sensor in situ showed that the cracks are generated by stress concentration in alloy aggregates that form during the initial stage of ultrasonic bonding.

[8-3] Simultaneous characterization of mechanical and electrical performances for ultraflexible and stretchable organic integrated circuits

Tsuyoshi Sekitani[1,2], Tomoyuki Yokota[1,2], Kazunori Kuribara[1,2], Takao Someya[1,2]

[1]Department of Electrical and Electronic Engineering and Department of Applied Physics, University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo, Japan

[2]Exploratory Research for Advanced Technology (ERATO), Japan Science and Technology Agency (JST), 2-11-16, Yayoi, Bunkyo-ku, Tokyo, Japan

We report simultaneous characterization of mechanical and electrical performances for ultraflexible and stretchable organic integrated circuits comprising high-performance organic semiconductors, carbon-nanotube based elastic conductors, and self-assembled monolayer. Employing a high-precision mechanical stage combining electrical functional terminals, electrical performances of ultraflexible organic complimentary circuits have been measured with being bent down to 50 um in bending radius.

[8-4] The MEMS 5-in-1 Standard Reference Materials (SRM 2494 and 2495)

Janet Cassard, Jon Geist, Michael Gaitan, and David G. Seiler

Semiconductor and Dimensional Metrology Division, Physical Measurement Laboratory, National Institute of Standards and Technology (NIST), USA

The MEMS 5-in-1 Standard Reference Material (SRM) contains test structures for five standard test methods on one test chip, so companies can compare their in-house measurements taken on the SRM with NIST measurements, thereby validating their use of the documentary standard test methods. Example NIST certified and reference values are given for an SRM 2494 monitor chip used at NIST for stability studies.

17:00 - 18:30 End

18:30 - 22:00 Banquet on the William D. Evans

Thursday March 22

08:30 - 09:00 Registration and Continental Breakfast

09:00 - 10:20 Session 9 - Matching

Co-Chairs:

Mark Poulter	Texas Instruments, USA
Hans Tuinhout	NXP Semiconductors, The Netherlands

[9-1] Self-Biasing and Self-Amplifying MOSFET Mismatch Test Structure

Colin C. McAndrew, Mike Zunino, and Brandt Braswell

Freescale Semiconductor, Tempe, AZ, USA

This paper presents a 4-transistor test structure for the measurement and characterization of MOSFET mismatch. The structure consists of a CMOS inverter with its output connected to its input, so it self-biases at the point of maximum sensitivity to parametric variations from mismatch, connected to a second identical inverter. The voltage difference between the outputs of the first and second inverters depends only on mismatch between the transistors, and is of order of 100's of mV and so is easily measurable even in a noisy or poor quality test environment. Several interesting applications of the new structure are also presented.

[9-2] Active "multi-fingers": Test structure to improve MOSFET matching in sub-threshold area

Y. Joly[1,2], L. Lopez[1], J.-M. Porta[2], H. Aziza[2], Y. Bert[1], F. Julien[1], P. Fornara[1]

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[2]IM2NP Laboratory (UMR CNRS 6242), 38 rue Frédéric Joliot Curie, 13451 Marseille, France

Low power analog applications are often designed under threshold and can be degraded by hump effect. This effect is explained with device width and body bias studies. A MOSFET matching improvement in sub-threshold area is demonstrated with active "multi-fingers" test structure.

[9-3] Characterization and Modeling Methodology for the Evaluation of Statistical Variation of MOSFETs

L Bortesi[1], L. Vendrame[1], P. Fantini[1], A.Spessot[1], and A. L. Lacaita[2]

[1]Micron Technology, Inc., R&D – Technology Development, Agrate Brianza, Italy
[2]Politecnico of Milano and IFN-CNR, Milano, Italy

This paper presents a thorough investigation of the main variability sources affecting both the digital and analog performances of CMOS devices. Through a wide statistical characterization of both single and matched pairs of CMOS devices, we are able to separately study the impact of the different variability sources (oxide thickness fluctuation, doping fluctuations, channel length and width variability, carrier mobility fluctuations ...) on the overall device performance. Finally, a compact model, allowing the accurate statistical simulation of circuits including all the aforementioned variability sources, is proposed, thus aiding the design of more robust high performance circuits.

[9-4] Impact of mask making imperfections on the performance of matching critical sub-circuit blocks

L. J. Choi[1], M. Poulter[1], J. de Santis[1], G. Cestra[1], L. Moberly[1], K. Gadepally[1], H. McCulloh[2], R. Beera[2], V. Garg[3], K. Green[3], and J. Prater[4]

[1]Texas Instruments Inc., 2900 Semiconductor Drive, Santa Clara, CA, USA
[2]Texas Instruments Inc., 5 Foden Road, South Portland, ME, USA
[3]Toppan Photomasks Inc., 131 Old Settlers Boulevard, Round Rock, TX, USA
[4]Texas Instruments Inc., 3800 Automation Way, Suite 100, Fort Collins, CO, USA

In this paper, we present an investigation of the impact of mask making imperfections on matching. Comparing optically measured and electrically derived data for line width errors allows pinpointing whether or not the mask limits the best achievable device matching. Treating matching critical sub-circuit blocks themselves as test structures, we demonstrate a direct methodology for assessing the impact of process and mask on the performance of high-precision analog products.

10:20 - 10:50 Break

10:50 - 12:10 Session 10 - Capacitance

Co-Chairs:	
Bill Verzi	Agilent Technologies, USA
Alain Toffoli	CEA, France

[10-1] Combined C-V/I-V Front-End-Of-Line Measurement

Stas Polonsky[1], Simeon Realov[2], Jiun-Hsin Liao[3], Michael Hargrove[4], and Mark Ketchen[1]

[1]IBM Research, T. J. Watson Research Center, Route 134, Yorktown Heights, NY, USA
[2]Department of Electrical Engineering, Columbia University , New York, NY, USA
[3]IBM Systems and Technology Group, 2070 Route 52, Hopewell Junction, NY, USA
[4]GLOBALFOUNDRIES Technology Development, 2070 Route 52, Hopewell Junction, NY, USA

We present a simple test structure to measure C-V and I-V curves of the same nominal size FET. The structure is simple enough to be used for technology development, requires only first metal for routing, and allows parallel test. It is an extension of FEOL QVCM technique, reported at this conference in 2011, and uses dc current measurement for C-V extraction with atto-Farad resolution. The utility of the presented technique is illustrated with 22 nm SOI device characterization.

[10-2] Nano CV Probe Characterization Analysis Comparison with Conventional CV Probe Pad Analysis

Terence Kane, Michael P. Tenney

IBM Systems and Technology Group, Hopewell Junction, New York, Terence .Kane 2070 Route 52, Hopewell Junction, NY, USA

The introduction of nano CV characterization of discrete MOSFET devices and the method of performing scanning capacitance imaging has been previously presented.1 By nano probing at CA contact level discrete MOSFET devices that are routinely analyzed at probe pad level with conventional CV easurments, a means of comparison can be established to compare the results obtained by both methods. More importantly, the nano CV measurements obtained at CA contact level can be validated by this comparison.2-6 This paper will describe nano CV measurements of discrete devices and show comparison results obtained at probe pad level that confirms the validity and accuracy of nano CV measurements.

[10-3] A Novel CBCM Test Structure for MOSFET CCTG Measurement in Advanced 28nm Technology

Willy Tsao, Kin Hooi Dia, Zheng Zeng, Cheng Hsing Chien

MediaTek Inc., No. 1, Dusing Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan

In the advanced CMOS technology nodes, overlap capacitance (Cov), gate fringing capacitance (Cf) and contact-to-gate capacitance (Cctg) have been increasingly important components of transistor parasitic. Accurate Cov could be extract from MOSFET Cgc curve with metal routing de-embedded structure. But Cf and Cctg could not be extracted and separated clearly with traditional AC testkey. Traditionally, Cctg and Cf are simulated and extracted by 3D solver such as Raphael simulator but lack of the correlation between Silicon and simulation. In this paper, we introduce CBCM into MOSFET FEOL Cctg and Cf measurement and extraction. With good

capacitance measurement resolution of CBCM methodology and specially designed test structurers, Cctg and Cf can be successfully measured and extracted without mega routing of multiplier device. The test structures and extraction methodology are described in this paper, the extraction results from a 28nm process is also presented. This is the first published paper in MOSFET transistor FEOL parasitic (Cf+Cctg) measurement from 28nm process real Si.

[10-4] Fast and Accurate Characterization of Interconnect Capacitance Network Using Degenerated Exhaustive Direct Charge Measurement (DEDCM)

Masaharu Goto, Jun Taniguchi and Kenichi Takano

Agilent Technologies International Japan Ltd., Tokyo, Japan

Continuing scaling down trend of semiconductor process node has increased the necessity of comprehensive interconnect capacitance testing, however, the measurement has only been made between limited combinations of conductor groups due to test time constrains. In this paper, we propose new interconnect capacitance measurement method, Degenerated Exhaustive Direct Charge Measurements (DEDCM). This method enables measuring all interconnect capacitance components accurately and faster.

12:10 - 12:20 Closing Ceremony

12:20 End

12:20