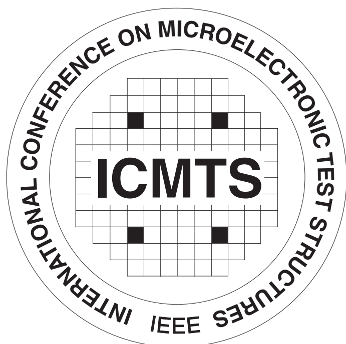
24th ICMTS

2011 IEEE International Conference on Microelectronic Test Structures



April 4-7, 2011
Royal Academy of Arts and Sciences
Kloveniersburgwal 29
Amsterdam, The Netherlands

Sponsored by:
The IEEE Electron Devices Society

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WELCOME LETTER

Dear Colleagues,

The 24th International Conference on Microelectronic Test Structures will be held in downtown Amsterdam (The Netherlands) at the Royal Academy of Arts and Sciences, Kloveniersburgwal 29, Amsterdam. This year it is organized in cooperation with the University of Twente and the MESA+ Institute for Nanotechnology. It is sponsored by the IEEE Electron Devices Society. The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The conference will be held on April 5-7, 2011, and will be preceded by a one-day Tutorial Short Course on Microelectronic Test Structures on April 4.

The first ICMTS was held in Long Beach in 1988, and since then the conference has cycled between Europe, North America, and Asia. It will be held in The Netherlands for the first time this year. As in previous editions the conference will be preceded by a one-day Tutorial Short Course on microelectronic test structures and there will also be a related equipment exhibition focused on test structure measurements and related companies.

Venue of the Conference is the Trippenhuis, conveniently situated within walking distance of the Central Train Station, in the heart of the old town. Hotels, restaurants and tourist attractions are abundantly found in the near vicinity. The Trippenhuis itself, seat of the Royal Academy of Arts and Sciences, is a monumental building erected in the year 1655. It was built as the residence of the Trip brothers and their households. Louys and Hendrick Trip were successful dealers in arms. Many decorations and ornaments in the building refer to their profession, including the barrel-shape chimneys at the rooftop. Later, the building served several purposes, also as the first location of the State Museum (Rijksmuseum). As such it was home of Rembrandt's famous Nightwatch painting in the period 1817-1885.

An attractive social programme is offered to the conference delegates and accompanying persons. This includes a Welcome Reception on Monday, a Conference Banquet on Wednesday, and a diverse social programme on Thursday afternoon. The social programme will consist of walking tours with a choice of nearby tourist attractions, guided by experts in both Dutch culture and microelectronic test structures. We hope to welcome you in Amsterdam in April!

Sincerely

Jurriaan Schmitz, General Chairman
Luca Selmi, Technical Chair
Annemiek Janssen, Local Arrangements Chair

GENERAL INFORMATION

Conference Information

The 2011 International Conference on Microelectronic Test Structures is financially sponsored by the IEEE Electron Devices Society. The conference is also being supported by the University of Twente and its University Fund; and the MESA+ Institute for Nanotechnology. The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The Conference will be preceded by a one-day Tutorial Short Course covering a variety of technical areas related to Microelectronic Test Structures.

The Tutorials, Welcome Reception, and the Technical sessions will all be held at the Trippenhuis. The address is: Kloveniersburgwal 29, Amsterdam.

Website and Email Contacts

ICMTS Website:
http://icmts2011.ewi.utwente.nl/
General Contact:
a.m.r.j.janssen@utwente.nl
Technical Contact:
icmts2011@uniud.it

Presentations

The official language of the conference is English. All regular conference contributions will be presented orally this year. The time allowed for regular presentations is 15 minutes plus 5 minutes for discussion. We welcome two Invited Speakers to the conference this year: Dr. Koen Martens (IMEC) and Dr. Jan Willem Maes (ASM). The Invited Speakers are allocated 35 minutes plus 5 minutes for questions.

The Tinbergen lecture hall, venue of the Tutorial and Technical Program

The conference hall offers up to 200 seats and offers all required facilities including PC, beamer, and audio equipment. All presentations will be uploaded on the Conference PC before the start of

the conference, to allow a smooth transition between consecutive presentations. Hence, all presentation materials should be sent to a.m.r.j.janssen@utwente.nl before the 21st March 2011. Adobe PDF and PowerPoint (.ppt and .pptx) formats are accepted. In addition, all presenters are requested to bring the original files as backup. All speakers are requested to report to their session chairperson 10 minutes before the session begins. They can then familiarize themselves with the control panel, and ensure that their presentation files are correctly loaded on the computer system well before the session starts.

Best Paper Award

The program committee will select one of the regular conference contributions for the Best Paper Award. The Best Paper will be announced at the end of the conference. The award will be handed out at ICMTS 2012. During the Conference Banquet, last year's Best Paper Award will be handed out to the recipients. The Award was won last year with the paper entitled "Small embedded sensors for accurate temperature measurements in DMOS power transistor" authored by Martin Pfost and coworkers.

Conference Proceedings

The conference proceedings will be published in paper and on a USB-stick. One copy of the paper proceedings and one USB stick are included in the registration fee. Additional copies will be available at the conference for 30€ per copy.

Conference Registration

Registration Fees

Early Registration (Before January 31st, 2011)

	Member*	Non Member	Student**
Tutorial	100€	120€	50€/60€
Technical Sessions	270€	330€	160€/190€

Late Registration (After February 1st, 2011)

	Member*	Non Member	Student**
Tutorial	120€	145€	70€/85€
Technical Sessions	330€	400€	220€/265€

On-site Registration (Registration at the conference)

On-site registration goes at the Late Registration fee plus an extra 10€ for the Tutorials, and an extra 20€ for the Technical Program.

* Must be a member of the IEEE

** Lower prices for student members of IEEE

Registration fees include admission to the technical sessions, equipment exhibits, morning and afternoon coffee breaks, the welcome reception, lunch (Monday – tutorial, Tuesday, Wednesday and Thursday – conference) and the conference banquet. It also includes one paper copy of the proceedings and a USB stick.

Payment of Registration Fees

Payment should be made using the Conference Website: http://icmts2011.ewi.utwente.nl/ . Onsite, the registration payment can be in cash or using a credit card (MasterCard, Visa or American Express). The confirmation of your IEEE Membership or Student status will be conducted during Registration at the Conference.

Cancellation

Due to advance financial commitments, refunds of registration fees requested after March 1st, 2011 cannot be guaranteed and will only be considered after the conference. A processing fee of 50€ will be deducted from all refunds.

Equipment Exhibition

During the conference an equipment exhibition will be held in the foyer outside the conference room. The exhibition will display equipment and systems closely associated with the design, fabrication, analysis and characterisation of test structures. Companies working in related fields present themselves and their products. This exhibition will permit one-to-one discussions between exhibitors and conference attendees on the latest practices and test equipment. For more details see the ICMTS website. The exhibition opening times are given below along with a preliminary list of exhibitors. The full list will be distributed at the conference.

April 4	9:00–17:00	Set up – Tutorial
April 5, 6	9:00–17:00	Conference
April 7	9:00–12:00	Conference and Close-down

Exhibitors List (at time of press)
Agilent Technologies
Cascade Microtech
Celadon Systems
COREWafer
MASER Engineering
Keithley Instruments

Messages

If you need to be contacted during the Conference Sessions, a message can be left at the registration desk between the hours of 9:00am and 5:00pm, April 4-6, and from 9:00am to 12 noon on April 7. Messages will be placed on a Message Board beside the registration desk.

Messages can be posted for attendees by calling Mrs. Annemiek Janssen (+31 613937828) or by emailing her using the conference address a.m.r.j.janssen@utwente.nl.

Internet access

The conference area is equipped with wireless internet outside the lecture hall. Two permanent workstations are at the delegates' disposal for internet access.

Lunch Venue

During ICMTS the tutorial and conference lunches will be served at the Trippenhuis just next door to the lecture hall and the Exhibition.

Conference Banquet

The conference banquet will be held in the famous restaurant Sluizer at Utrechtsestraat 41-45. The restaurant has a high reputation for its fish dishes, and serves a variety of Dutch and French cuisine.

Sluizer Restaurant, outside

Sluizer Restaurant, inside

The conference registration fees include one banquet ticket. Guest tickets will be available for sale at the registration desk for 70€.

Excursion

The excursion will take place Thursday afternoon after lunch, between 13:30 and 17:30 approximately. It will be in the form of small-party city exploration tours (on foot) targeting one or two tourist highlights, such as Anne Frank's House and the Heineken Brewery. Details of the excursion will be announced at the conference, where registration will take place.

Amsterdam Information

Getting there

Amsterdam Schiphol Airport is about 20 km from the centre of the city. There is a good and frequent train connection to/from Amsterdam Central Station (six trains every hour during daytime), costs 3.80€ for a one way trip of fifteen minutes. Amsterdam is connected to the high-speed train line Thalys connecting to Bruxelles and Paris, as well as many other international destinations. Please note that due to the construction of a new underground line, parts of and around the Amsterdam Central Station are inaccessible. Taxis are available at the west entrance/exit.

The venue is within 15 minutes walking from Amsterdam's Central Train Station. All conference hotels are within walking distance. Several metro lines (51, 53, 54) stop at the subway (Metro) station Nieuwmarkt. Its exit *Nieuwe Hoogstraat* is just around the corner of the Trippenhuis. The *OV-chipkaart* (PT Smart Card) is the new way to pay for public transport in Amsterdam. You can travel using just one card, whether it is in the train, bus, tram or metro. The OV-chipkaart is the size of a credit card and has a built-in chip.

For conference visitors a disposable OV-chipkaart is advised. You can buy disposable cards at GVB Tickets & Info (Municipal Transport Company) across from the Central Train Station, and with tram and bus drivers and conductors. At the Ticket Vending and Add Value machines you can pay cash and with PIN, chip or credit card.

For more information on public transport in Amsterdam, check www.gvb.nl.

Maps

Amsterdam City Map

The website http://www.amsterdam.info/map/ (powered by Google) is suggested for orientation.

Climate

The Amsterdam weather in early April is rather unpredictable. The daily maximum temperature in early April is around 12 °C but night frost cannot be excluded. March and April happen to be the least rainy months in Amsterdam, but still it is likely that some rain will fall. Warm clothing, comfortable shoes and an umbrella are advised.

Accommodation

Downtown Amsterdam offers hundreds of hotels and guest houses covering a wide range of prices and standards. A web-based hotel reservation facility has been created for ICMTS guests, accessible from the ICMTS home page. All selected hotels offer nightly rates in the 115-160€ range and are within walking distance from the conference venue.

Currency

The official currency in The Netherlands is the Euro (€). Banks normally open on weekdays between 9:00am until 4:00 pm. At Schiphol airport, banks are open all days. ATMs are available at Schiphol Airport, at the Central Train Station, and throughout the city.

Electricity and telephone

The Dutch electricity net is 230 V/50 Hz and uses the European plug (Europlug). The cellular phone network is GSM 900/1800. All mobile operators support GPRS. KPN and Vodafone offer UMTS service in some parts of The Netherlands.

National Emergency numbers

For emergencies, Police, fire brigade, ambulance: tel.: 112. For contacting the police, no emergency: tel.: 0900 8844.

Safety and crime

Amsterdam is considered as a relatively safe city. In general, violent crimes do not occur very often. However be aware of pickpocketing. Pickpockets are mainly active in the summer and in the train travelling between Amsterdam Central Station and Schiphol Airport. They can also find you in a tram or when you are watching one of the many street artists perform. Watch your belongings carefully.

The Amsterdam Tourist Assistance Service (ATAS) provides a special service to tourists who are robbed or otherwise victimised while visiting the city of Amsterdam. It is located at Nieuwezijds Voorburgwal 104-108. Tel.: +31 20 6253246.

Embassies and consulates

Dutch embassies and consulates abroad and foreign embassies and consulates in the Netherlands can be found on www.minbuza.nl.

Whether a prospective visitor requires a visa depends on his nationality and how long he intends to stay in the Netherlands. Nationals of many countries require a visa for an uninterrupted stay of up to three months.

Sight-seeing Amsterdam

Amsterdam has a lot to offer: the historic centre along the canals, the museums, churches, arts & craft stores, antique stores, the contemporary architecture in the former harbour areas, and the theaters and concert halls that offer both classic and modern repertoire.

You can explore Amsterdam and its surroundings on foot, by bike, coach or boat. Information is available at the Amsterdam VVV Offices (Tourist Information Office) at Platform 2 of the Amsterdam Central Station, at Stationsplein across the Central Station and at the Holland Information desk at Schiphol Plaza. For more information about the city's history and current activities check the following websites:

www.iamsterdam.com and www.holland.com.

The *I amsterdam Card* gives you free admission to the city's main museums, a free canal cruise and free public transportation. The *I amsterdam Card* also entitles you to 25% discount at various attractions and restaurants. The*I amsterdam Card* is available for 24 hours (38€), 48 hours (48€) or 72 hours (58€). See www.iamsterdam.com.

Many visitors of Amsterdam have the Rijksmuseum and Van Gogh Museum on their list of must-sees. Other attractions include: the Rembrandt House, the Stedelijk Museum, the Amsterdam Historical Museum, Anne Frank House, the Royal Palace, the Jewish Historical Museum, the Hermitage Amsterdam, the Hortus Botanicus, Artis Zoo, the Concertgebouw, the Muziektheater, and the Muziekgebouw aan het IJ. For these and other places to go in Amsterdam, see www.amsterdam.info.

The Amsterdam Canals, UNESCO World Heritage.

TUTORIALS

Tutorial Lecturer Biographies

Richard A. Allen

Richard Allen received his B.S. and M.S. degrees (both in Physics) from Rensselaer Polytechnic Institute, Troy, New York, U.S.A. and his M.B.A. from Columbia Union College (now Washington Adventist University) Takoma Park, Maryland, U.S.A. His career has focused on the development of test structures for microelectronics and MEMS applications. Early in his careen at the Jet Propulsion Laboratory in Pasadena, California U.S.A., he worked on the development of test structures for in-situ monitoring space radiation effects. Since 1990 at the National Institute of Standards and Technology, Gaithersburg, Maryland U.S.A., his research has been in test structures for measurement standards for VLSI, microfluidics, and MEMS applications. He served as Tutorial Chair for the 2006 ICMTS, the Technical Chair for the 2009 ICMTS, and will serve as General Chair of the 2012 ICMTS.

Kitty van Dijk

Kitty van Dijk received her MSc (1992) and PhD (1997) degree in Solid State Physics from the Technical University of Delft, and from the University of Nijmegen, respectively, both in The Netherlands. After post-doc positions at the UCLA (USA), and the Technical University of Lisbon (Portugal), she joined in 1998 the Research and Development group of ASMI at IMEC in Leuven, Belgium, working on gate-oxide quality. In 2000 she moved to NXP (former Philips) Semiconductors in Nijmegen, where she started on non-volatile memory (NVM) reliability, eventually broadening to process and product reliability in general. Her special interest is the interaction between process and product reliability, with a focus to Automotive or extreme mission profile qualifications. At this moment she works in the NVM process development section where she is responsible for the NVM process qualifications at External Foundries.

Yoshio Mita

Yoshio MITA is an associate professor of the Department of Electrical and Electronics Engineering, the University of Tokyo.

He got his Bachelor, Master, and Ph.D degrees of Electrical Engineering from the University of Tokyo in 1995, 1997 and 2000, respectively. His Ph.D work was on the VLSI integrated intelligent Micro Electro Mechanical Systems that he called "Smart MEMS". After his PhD, he served as an assistant professor of the VLSI Design and Education Center (VDEC), and was promoted to Lecturer in the Department of Electrical Engineering in 2001 and then to Associate Professor in 2005.

His current research interests include VLSI integrated MEMS, nanostructures, and nano electrical devices by MEMS semiconductor technology.

From May to August 2007, he was a visiting academic at the Scottish Microelectronic Centre (SMC) in the University of Edinburgh,

Scotland, where he initiated research on autonomous distributed micro mobile devices, using low-voltage electro wetting on dielectrics (EWOD) technology. From September 2007 to September 2008 he was an invited professor at the national informatic research center (INRIA) in Paris, where he conducted prospective research of MEMS application as safety sensors in vehicules.

Edwin T. Carlen

Edwin T. Carlen studied physics and electrical engineering and received the Ph.D. degree from the University of Michigan, Ann Arbor in electrical engineering in 2001. While at Michigan he worked on a variety of projects related to stochastic process modeling, TCAD, BioMEMS and MEMS. From 2000-2003 he worked for Corning- Intellisense as a Senior MEMS development engineer responsible for photonic switching and integrated optics research and development. From 2003-2005 he was a Principle Member of the Technical staff at The Charles Stark Draper Laboratory in Cambridge, MA, developing biosensors for label-free detection of protein binding. In 2006, he joined the scientific staff as the 3TU Assistant Professor in the BIOS/Lab on a Chip Group at the University of Twente and MESA+ Institute for Nanotechnology, The Netherlands. His research is broadly aimed at engineering materials at the atomic and mesoscopic scales for applications such as medical diagnostics, measurement of thermodynamic properties of ligand-receptor binding, and energy conversion. Currently, his research is focused on the design, fabrication, and characterization of nanometer-size electronic, optical and mechanical sensors that exploit nano-scale physical and chemical properties that enhance the sensitivity of detecting receptor-target binding from ultra-low target concentrations in miniaturized small sample volume chemical analysis platforms. For the last few years his group has concentrated on the development of silicon nanowire potentiometric biosensors and plasmonic nanostructures for surface enhanced Raman scattering that are applied to Raman spectroscopy of surface adsorbed molecules in solution.

Robin Degraeve

Robin Degraeve received the M. Sc. degree in electrical engineering from the University of Ghent, Belgium in 1992. He joined the R&D Laboratory IMEC in Leuven, Belgium, where he is currently working in the Advanced Electrical Characterization and Reliability group as a senior researcher. In 1998, he received his Ph.D. degree from the Catholic University of Leuven, Belgium. His major field of expertise is the characterization and degradation of thin insulating layers and related reliability issues in advanced CMOS applications. His research includes the study of degradation and breakdown phenomena (Time-dependent Dielectric Breakdown and Bias Temperature Instability) in ultra-thin gate oxide layers and alternative high-k materials, the understanding of tunnel oxide-related reliability issues in flash memories, the characterization of novel high-k materials for future flash technologies (e.g. TANOS), and the understanding of the operation and reliability issues in resistive RAM memories. He has special interest in future trends and paradigm shifts in reliability, like the defi-

nition of reliability as time-dependent variability. He presented short courses at several conferences (IRPS, P2ID, ESREF, IRW, UCPSS, ICMTS) and served as a member of the program committee of IRPS, IEDM, INFOS and SISC.

Christopher Hess

Christopher Hess received the diploma degree in electrical engineering and the Dr.-Ing. (Ph.D.) degree in computer science from the University of Karlsruhe, Germany. In 1992 he was a founding member of the Defect Diagnosis Group at the University of Karlsruhe. In 1998 he joined PDF Solutions in San Jose, CA. As a Fellow he is currently responsible for Yield & Performance Characterization.

Since 1992, he has been involved in the design of hundreds of test chips for the microelectronics industry over numerous technologies. For years, his main R&D focus is on efficient merging of experiments by minimizing chip area usage and manufacturing cycle time. His activities also include developing new architectures of testing equipment providing several orders of magnitude more data from high density test chips compared to testing traditional stand alone experiments. Most recently he is working on high density test chips for scribe line applications.

Dr. Hess has published about 50 conference and journal papers and he holds more than 10 patents. He is a Senior Member of the IEEE and the Electron Device Society as well as a technical committee member of several semiconductor manufacturing related conferences. He has served as Technical Chairman of the 2000 International Conference on Microelectronic Test Structures (ICMTS) and General Chairman of ICMTS in 2003.

Peter J. Hulbert

Peter J. Hulbert is a Product and Applications Development Engineer with Keithley Instruments in Cleveland. He received his bachelors degree in Physics from Washington State University. His career in measurement instrumentation has overlapped a good portion of the electromagnetic spectrum from ionizing radiation to the far infrared. He has held various positions at Keithley associated with semiconductors and their application. He can be reached at phulbert@keithley.com.

Tutorial Program

Monday 4th April

Location: Trippenhuis

08:00–17.00 Registration

09:00-09:05 Introduction

Johan Klootwijk, Tutorial Chairman

09:05–09:55

1. Test structure fundamentals

Richard Allen

NIST, USA

This presentation will begin with a review of the history of test structures and their application to silicon processes. The presentation will emphasize the measurement of parameters such as sheet resistance, line width (critical dimension), contact resistance, and capacitance using four-point Kelvin measurements, which serve as the basis for most accurate measurements of process and device parameters using test structure. Measurement and equipment developments will also be addressed, focusing on procedures for obtaining accurate and repeatable measurements.

09:55–10:45

2. Test-structures for CMOS process qualification

Kitty van Dijk

NXP Semiconductors, The Netherlands

Process qualifications consist of a wafer level reliability part and a product level reliability part. Wafer Level Reliability (WLR) tests address the fundamental reliability degradation of single transistors. For product level reliability, JEDEC and Military standards are available in which is described what tests to perform on your product. But what test structures can be used to link the WLR results with the product level reliability? How to deal with processes at external Foundries that you want to use beyond the Foundries own qualification requirements? What to test on your test structures, and how to perform those tests? Those questions will be addressed in this presentation.

10:45–11:15 Break

11:15–12:05

3. MEMS, More-than-Moore, and test structures

Yoshio Mita

University of Tokyo, Japan

Micro Electro Mechanical Systems (MEMS) are providing the VLSI world with new functionalities such as electro-mechanical transductions, electro-chemical reactions, and electro-optical interactions. From viewpoint of VLSI world MEMS is expected to open new "More-than-Moore" fields. As the nature of MEMS devices and process technologies is their variety, the importance of test structures as well as testing methods are increasing continuously.

According to the author, the test structures and testing methods' world can be categorized by three sentenses: of the MEMS,

by the MEMS, and for the MEMS. (1) "Test Structures OF THE MEMS devices" include micro structures that are used to extract material and process parameters. (2) "Testing BY THE MEMS devices" may enable very precize measurements or measurements in the very special environments that has not been exploited by any other methods. Recent trends of MEMS devices is integration with the VLSI circuits so that the (3) "Test Structures FOR THE MEMS Integrated Circuits" are emerging accordingly. The integrated circuit not only can be used as local controller in normal operation mode, but be used for self-testing circuitry. In the tutorial, the author would like to explore with audience the world of MEMS test structures, together with maximum number of live demonstrations.

12:05–12:55

4. Silicon nanowire sensors: physics, fabrication, and electrical and electrochemical characterization

Edwin T. Carlen

University of Twente, The Netherlands

Over the past several years many research groups around the world have reported the application of silicon nanowires as optical, mechanical, and electronic devices. In this tutorial, I will review some of these device types and applications, and then followed by a description of some real-world results and observations of ongoing work in our group in the modeling, fabrication, electrical and electrochemical characterization of silicon nanowire field-effect biosensors.

12:55–14:25 Lunch

14:25–15:15

5. Ultra-thin dielectrics in ultra-small devices: a double challenge for characterization and reliability evaluation.

Robin Degraeve

IMEC, Belgium

Scaling the gate oxide thickness to the 1 and sub-1 nm range required the introduction of high-k materials, which are far more defective than SiO2. The characterization and reliability research community was faced with the challenge of developing advanced methods to measure the high-k defect density distribution and derive its impact on reliability issue like Time-Dependent Dielectric Breakdown (TDDB) and Bias Temperature Instability (BTI). In this tutorial an overview of some of these techniques (pulsed hysteresis, bulk charge pumping, etc..) is presented and their fundamental working principles are explained. A second challenge for the research community originates from the inevitable scaling to very small lateral device dimensions. As a consequence the effect of individual defect sites becomes dominant, resulting in a wide spread of device parameters. Also reliability becomes a stochastic process that requires a thorough statistical approach. In the tutorial, the evolution in reliability statistics for TDDB and BTI is discussed starting from the microscopic understanding of breakdown paths and charge centers resp.

15:15–16:05

6. Efficient usage of test structures

Christopher Hess

Pdf Solutions, USA

Test Structures are used for an ever increasing set of applications. Thus, more and more test structures have to be designed, manufactured, tested and analyzed. Focusing on Yield and Variability, the Tutorial will provide methods to increase the Number of Experiments, while decreasing Mask Cost and Test Time. Furthermore, the tutorial will provide an overview how those methods can be applied to more efficiently utilize product scribe line area to allow advanced process control monitoring.

16:05–16:55

7. Ultra fast IV characterization

Peter J. Hulbert

Keithley Instruments, USA

This tutorial will cover various aspects of fast source and measurement characterization: definitions, measurement fundamentals, challenges and best practices. We will illustrate these concepts with typical applications such as self-heating effects and non-volatile memory.

Welcome reception

CONFERENCE

Tuesday 5th April

Location: Trippenhuis

08:00–17.00 Registration

09:00–09:10 Opening Remarks
Jurriaan Schmitz, General Chairman
Luca Selmi, Technical Program Chairman

SESSION 1: Capacitance

09:10–11:10
Co-Chairs: Satoshi Habu, *Agilent Technologies, Japan*
Christopher Hess, *PDF Solutions, USA*

09:10

Invited paper –Admittance Characterization and Interface Trap Property Extraction for Ge/III-V MOS Structures

Koen Martens
IMEC, Belgium

MOS admittance characteristics, essential for extracting crucial parameters of MOS devices, can be heavily distorted because of Ge/III-V properties such as poor interface passivation and bandgap. These distortions can result in far-reaching misinterpretations and large errors in extracted parameters. The differing admittance characteristics and related adapted interface trap extraction methods are elaborated for Ge/III-V MOS.

09:50

1.1 – Front-End-Of-Line Quadrature-Clocked Voltage-Dependent Capacitance Measurement

S. Polonsky, P. Solomon, J.H. Liao[1], L. Medina[1], M. Ketchen
IBM T.J. Watson Research Center, NY; [1]IBM Systems and Technology Group, Hopewell Junction, USA

We report on Front-End-Of-Line Quadrature-clocked Voltage-dependent Capacitance Measurements (QVCM), a charge based capacitance measurement technique applicable to modern logic CMOS technologies with leaky gate oxides. QVCM test structures are designed using only first level of metal and support parallel test of multiple devices. Results for 45 nm SOI FETs illustrate the power of the developed technique.

10:10

1.2 – Evaluation of MOSFET C-V Curve Variation Using Test Structure for Charge-Based Capacitance Measurement

K. Tsuji[1], K. Terada[1], R. Kikuchi[1], T. Tsunomura[2], A. Nishida[2] and T. Mogami[2]
[1]Hiroshima City University; [2]MIRAI Selete, Japan

Test structure for Charge-Based Capacitance Measurement, CBCM, is improved, to achieve higher accuracy of measuring capacitance-voltage (C-V) curves for actual size MOSFETs. Capacitance mismatch between the device under test and the

reference is avoided by using Charge-Injection-Induced-Error-Free CBCM (CIEF CBCM) method. To increase the bias voltage range both P- and N-channel MOSFETs are parallel-connected in the pseudo-inverter. It is found that the C-V curves, which are measured with this test structure and are corrected for removing the size effect, coincide with those measured by the conventional method, and then, the corrected capacitances give more accurate gate capacitances of MOSFETs.

10:30

1.3 – Modeling the Frequency Dependence of MOSFET Gate Capacitance

Z. Zhu[1], G. Gildenblat[1], C. McAndrew[2]

[1] *Arizona State University;* [2] *Freescale Semiconductor, USA*

This paper investigates the frequency dependence of gate capacitance C_{gg} of MOS structures. In inversion C_{gg} decreases as frequency increases due to charge inertia effects. In accumulation C_{gg} also decreases as frequency increases; we demonstrate this is due to bulk resistance. We show that the non-quasi-static PSP compact model can accurately model the frequency dependence of C_{gg} in all regions of operation for MOS transistors, and derive a new analytic frequency dependence model for C_{gg} in accumulation and depletion.

10:50

1.4 – A Simple System for on-die Measurement of atto-Farad Capacitance

E. Baruch, S. Shperber, R. Levy, Y. Weizman, J. Fridburg, R. Marks

Freescale Semiconductors Israel

Charge Injection Error Free (CIEF) Charge-Base Capacitance Measurement (CBCM) technique provides a simple way for accurate measurements on-chip interconnect parasitic capacitance. We report here for the first time capacitance measurements of on-chip interconnect with resolution values of 1aF or better. We analyze the setup requirements to allow such capability, and show stable coupling capacitance measurement results at the 1aF resolution.

11:10–11:20 **Exhibitor presentation**

11:20–11:40 **Break**

SESSION 2: Yield

11:40–12:40

Co-Chairs: Larg H. Weiland, *PDF Solutions, USA*
Kelvin Yih-Yuh Doong, *TSMC, Taiwan*

11:40

2.1 – A Versatile Defectivity Monitor Designed for Efficient Test and Failure Analysis

M. Lauderdale, B. Smith

Freescale Semiconductors, Austin, USA

This paper describes development, design, and test of a short flow defectivity monitor. Careful consideration was taken to size arrays for the appropriate D0 sensitivity. Additionally a

method was developed to quickly test large portions of the wafer then narrow the search area for FA. This method can be applied to very simple short flows.

12:00

2.2 – Low Cost Wafer Level Parallel Test Strategy for Reliability Assessments in sub-32 nm Technology Nodes

M. Rafik, F. Dieudonné, G. Morin

ST Microelectronics, Crolles, France

In this paper we describe the wafer level parallel testing strategy developed for reliability assessments in sub-32nm technology nodes. In fact, with the reduction of reliability margins and the apparition of TDDB specific issue, an improvement of test capabilities turns out to be mandatory. In this respect, specific TDDB test structures have been implemented in order to increase sampling for a given test duration. Furthermore, a prober bench that enable parallel multi-site testing has been developed. At a significantly lower price compared to industrial solutions proposed for parallel testing, this solution offers more flexibility in terms of test configuration. Finally, through this strategy a significant gain in terms of test time is achieved and also provides more confidence in the relevancy of reliability assessments.

12:20

2.3 – Product Relevant Device Leakage Scribe Characterization Vehicle Test Chip For Efficient Full Wafer Testing

C. Hess, R. Firu, R.Vallisheyee, S.Yu, P. Zhao[1], S. Zhao

PDF Solutions Inc., San Jose, USA; [1]PDF Solutions Inc., Shangai, China

Being successful in semiconductor manufacturing of sub 50nm devices requires controlling variability of device leakage. Full wafer monitoring is essential to provide significant data. The Device Leakage Scribe Characterization Vehicle (CV) Test Chip presented here fits well within the scribe area constraints of product wafers. Its devices under test (DUT) are using product relevant layout pattern to support new product introduction. Those DUTs are passively connected into device arrays to increase the signal to noise ratio of the device leakage measurements, which is essential to enable full wafer testing within existing test time restrictions on product wafers.

12:40–14:10 **Lunch**

SESSION 3: Parameter extraction

14:10–15:10

Co-Chairs: Kjell Jeppson, *Chalmers University, Sweden*
Franz Sischka, *Agilent Technologies, Germany*

14:10

3.1 – Improved Parameter Extraction Procedures for the R3 Model

C. McAndrew, T. Bettinger

Freescale Semiconductors, USA

This paper presents improved extraction algorithms for parameters of the R3 resistor model. For poly resistors we show how the depletion pinching parameters can be computed so that there are no numerical problems. For diffused resistors we provide a data analysis procedure that enables robust estimation of the depletion pinching parameters in the presence both of measurement noise and of velocity saturation or self-heating effects, and show that self-heating can be significantly more important than velocity saturation even for very long resistors.

14:30

3.2 – Contact Resistance Measurement Structures for High Frequencies

D. Roy, R. M. T. Pijper, L. F. Tiemeijer and R. A.M. Wolters[1]
NXP-TSMC Research Center, Eindhoven; [1]also at MESA+ Institute for Nanotechnology, The Netherlands

Knowledge of the electrical contact resistances offered by a device at its operating conditions is important for modeling and optimizing the performance of the device. The contact resistances are normally extracted by four point DC current-voltage measurements on dedicated measurement structures. In this article a modified TLM test structure with a ground-signal-ground configuration has been devised. Contact resistance measurements were performed on these structures from 1 MHz to 4 GHz. The extracted values are also compared with the measurements performed on the same structures in DC. The electrical model of the metal-to-PCM structures with different specific contact resistance will be discussed.

14:50

3.3 – Strategy for In-Line MOS Transistor Transport Optimization

A. Cros
ST Microelectronics, Crolles, France

We show that short channel transistors transport can be efficiently monitored from in-line measurement of the low field mobility at constant effective gate length, possibly corrected for Vth variations due to short channel effects. This method is independent from Cox, effective dimensions and access resistance, and well correlated to the saturation current variations.

15:10–15:40 **Break**

SESSION 4: MEMS

15:40–17:00

Co-Chairs: Emilio Lora-Tamayo, *Universitat Autonoma Barcelona, Spain*
Yoshio Mita, *University of Tokyo, Japan*

15:40

4.1 – Characterisation of Electroplated NiFe Films using Test Structures and Wafer Mapped Measurements

J. Murray, G. Schiavone, S. Smith, J. Terry, A.R. Mount[1], A.J. Walton

School of Engineering, The University of Edinburgh; [1]School of Chemistry, The University of Edinburgh, UK
Nickel-iron magnetic alloys have useful magnetic properties that are of interest to the MEMS industry but the high stress levels that can develop during the fabrication processes pose a real challenge. This paper addresses the characterisation of NiFe films using suspended rotating structures, electrical test structures and XRF. An automated measurement system has been set up that facilitates rapid wafer mapping to compare stress levels at different stages of the fabrication process. This has been used together with other wafer mapped parameters such as alloy composition, sheet resistances and layer thickness measurements to identify correlations and provide an increased understanding of the relationship between the process control factors.

16:00

4.2 – Exploring Capacitance-Voltage Measurements to find the Piezoelectric Coefficient of Aluminum Nitride

T. van Hemert, D. Sarakiotis, S.Jose, R.J.E. Hueting and J. Schmitz
MESA+ Institute for Nanotechnology, University of Twente, The Netherlands
In this work we extracted the piezoelectric coefficient of aluminium nitride.We showed how the piezoelectric coefficients can be extracted using a bias dependent capacitance model. For this purpose we used metal-piezoelectric-metal capacitors. We analyzed these using CV measurements and verified the dependence on geometry, layer thickness, biasing and sweep direction. The data revealed that parasitics such as fringe capacitance ought to be taken into account. We obtained a piezoelectric coefficient d_{33}=−53pm/V.

16:20

4.3 – Interdigitated Electrode Modelling for Applications in Dielectrophoresis

C. Chung, S. Smith, A. Menachery, P. Bagnaninchi, A.J. Walton and R. Pethig
University of Edinburgh, Edinburgh, UK
Electrical test structures have been designed to enable the characterisation of interdigitated electrode structures with lossy dielectrics, as used in dielectrophoresis. Test masks have been fabricated to explore the impact of array size, finger separation and resistive parameters on the applied electric field. A circuit model based on a distributed RC network is proposed and evaluated, demonstrating close agreement with actual impedance measurements.

16:40

4.4 – Test Structures and a Measurement System for Characterising the Lifetime of EWOD Devices

D. Gruber[1], Y. Li, S. Smith, A. Tiwari, F.Deng, A.A. Stokes[1], J.G. Terry, A.S.Bunting, L. Mackay[1], P. Langridge-Smith[1], A.J. Walton
School of Engineering, University of Edinburgh, [1]SIRCAMS, School of Chemistry, University of Edinburgh, UK

This paper presents a methodology together with a characterisation system for rapidly and quantitatively evaluating the lifetime of Electro-Wetting-on-Dielectrics (EWOD) microfluidic devices. By studying the contact angle (CA) change when electrowetting forces are applied on the test structure, the number of times a droplet can be repeatedly moved between two EWOD electrodes can be characterised. This paper describes the development of an automated measurement system and test structures that can be used to rapidly characterise and optimise EWOD dielectric layer compositions together with the determination of the driving voltage that results in the longest lifetime of the device.

17:00 End of Session 4

Wednesday 6th April

Location: Trippenhuis

08:30–17.00 Registration

SESSION 5: RF and noise characterization

09:00–10:20

Co-Chairs: Hi-Deok Lee, *Chungnam National Univ., Korea*
Kevin McCarthy, *University College Cork, Ireland*

09:00

5.1 – Decoupling of RTS Noise in High Density CMOS Image Sensor Using New Test Structures

J.-D. Bok, I.-S. Han, H.-M. Kwon, S.-U. Park, Y.-J. Jung, S.-H. Park, W.-I. Choi, M.-L. Ha[1], J.-I. Lee[1] and H.-D. Lee
Chungnam National University; [1]Dongbu HiTec Semiconductor Inc., Korea

In this work, RTS (Random Telegraph Signal) noise of the CMOS image sensor using new test structures is characterized. RTS noise of driver transistor and source follower transistor as well as the source follower bock itself are measured using the test structures. The probability of the monitoring the RTS noise of driver transistor and source follower transistor is 76 % and 52 %, respectively. However, the probability of the happening of RTS noise for the source follower block is about 74 %. Therefore, it can be said that the driver transistor dominates the RTS noise of the source follower block.

09:20

5.2 – Microsecond Pulsed DC Matching Measurements on MOSFETs in Strong and Weak Inversion

P. Andricciola, H. Tuinhout, N. Wils and J. Schmitz[1]
NXP Semiconductors; [1]University of Twente, The Netherlands

We present a first successful attempt to use microsecond DC pulses for matching measurements on 60-nm transistors down to low current levels. We demonstrate that the interface states that contribute to the mismatch in the weak and moderate inversion region are faster than 1 μs.

09:40

5.3 – Nonlinear Network Analyzer Measurements For Better Transistor Modeling

F.Sischka

Agilent Technologies, Böblingen, Germany

In today's RF applications, silicon transistors are more and more competing with III/V technology transistors. This means that MOS (LDMOS) and bipolar (HBT) transistors are operated under large signal conditions, applying time domain signals with amplitudes in the range of Volts, while the transistor modeling was usually performed conventionally with just small-signal excitation in the Milli-Volt domain, i.e. by S-Parameters. With the availability of Nonlinear Vector Network Analyzers (NVNA), measurements of transistor spectra with magnitude and phase become easily possible. And this permits to do device modeling also in the more realistic large signal RF domain. The new measurement and modeling domain therefore leads to improved compact models and improved modeling strategies.

10:00

5.4 – Silicon High Frequency Test Structures Improvement for Millimeter Wave Varactors Characterization Optimization and Modeling

F. Sonnerat[1,4], R. Debroucke[1,3], Y. Morandini[1,2], D. Gloria[1] and J.-D. Arnould[4]

[1]*ST Microelectronics, Crolles;* [2]*IBM-SRDC, Crolles;* [3]*IEMN, Villeneuve d'Ascq;* [4]*IMEP, Grenoble, France*

Innovative test structures must be designed to characterize these varactors with low capacitance values (down to aF) and an influent parasitic environment. Structures with reduced pad and modified metal stack added to an optimized test structure positioning have been validated up to 110 GHz.

10:20–10:30 **ICMTS 2012 - Presentation**

10:30–11:00 **Break**

SESSION 6: Process technology

11:00–12:40

Co-Chairs: Greg Yeric, *ARM, USA*
Alan Mathewson, *Tyndall National Inst., Ireland*

11:00

Invited paper – Innovative Thin Film Deposition Technologies Enabling New Materials and New Device Integration Roadmaps

Jan Willem Maes

ASM, The Netherlands

Innovative thin film deposition technologies play a key role in new device scaling strategies that are increasingly based on the use of new materials and 3D approaches. Smart tailor-made equipment solutions have enabled processes that were previously considered impossible for volume manufacturing. Examples of atomic layer deposition and epitaxy techniques for logic and memory devices will be presented as well as spin-offs to applications in solar cells and hard disks.

11:40

6.1 – Lateral Bipolar Structures for Evaluating the Effectiveness of Surface Doping Techniques

G. Lorito, L. Qi, and L.K. Nanver
DIMES, Delft University of Technology, The Netherlands

A lateral bipolar test structure is presented for evaluating the effectiveness of surface doping techniques used to fabricate ultrashallow diodes and ohmic contacts. Simple measurements provide a separation of hole and electron currents. Applicability is supported by measurement of Schottky and pn diodes fabricated by dopant deposition plus laser activation.

12:00

6.2 – Electrical Estimation of Channel Dopant Uniformity Using Test MOSFET Array

K. Terada, K. Sanai, S. Matsuoka, K. Tsuji, T. Tsunomura[1], A. Nishida[1] and T. Mogami[1]
Hiroshima City University, [1]MIRAI-Selete, Japan

The dopant uniformity in an MOSFET channel is estimated using the test MOSFET array which includes many MOSFETs with different channel length. Takeuchi coefficient as a function of the channel length is calculated from the measured threshold voltage data. The electrical channel length as a function of the gate voltage is extracted using channel resistance method. It is found that those data for MOSFETs having various channel structures show the similar degree of the dopant uniformity.

12:20

6.3 – An Efficient Array Structure to Characterize the Impact of Through Silicon Vias on FET Devices

D. Perry[1], J. Cho[2], S. Domae[3], P.Asimakopoulos[4], A.Yakovlev[4], P. Marchal[5], G. Van der Plas[5], N. Minas[5]
[1]*Qualcomm, San Diego, USA; Assegnees from* [2]*Samsung and* [3]*Panasonic to IMEC,* [4]*Newcastle University, UK;* [5]*IMEC, Belgium*

We present an array structure to evaluate impact of a through silicon via on neighboring FET devices. Several FET options and TSV configurations are explored. We show correlation between electrical measurements and mechanical stress models. Finally we discuss future improvements to the test structure.

12:40–14:10 **Lunch**

SESSION 7: Dielectrics

14:10–15:30

Co-Chairs: Luigi Pantisano, *IMEC, Belgium*
Antoine Cros, *ST Microelectronics, France*

14:10

7.1 – New Test Structure for Evaluating Low-k Dielectric Interconnect Layers by Using Ring-Oscillators and Metal Comb/Serpentine Patterns.

Y. Tamaki[1], M. Ito[1], Y. Takimoto[2], M. Hashino[1], and Y. Kawamoto[1].
[1]*Consortium for Advanced Semiconductor Materials and Related Technologies (CASMAT),* [2]*JSR Corp., Japan*

We have developed a new test structure for evaluating low-k materials. New structure is composed of several ring-oscillators with metal comb loads and metal serpentine patterns. Metal serpentine pattern was used for correcting the shape effect. Four kinds of low-k materials were evaluated by using the test structures, and relative dielectric constants for these materials were successfully measured. The advantage of the new structure has been confirmed.

14:30

7.2 – Characterization and Modelling of Gate Current Injection in Embedded Non-Volatile Flash Memory

A. Zaka[1,2,3], D. Garetto[4,5], D. Rideau[1], P. Palestri[3], J.-P. Manceau[4], E. Dornel[4], Q. Raphay[2], R. Clerc[2], Y. Leblebici[5], C. Tavernier[1], and H. Jaouen[1]

[1]*ST Microelectronics, Crolles,* [2]*IMEP, Grenoble, France,* [3]*DIEGM, University of Udine, Italy;* [4]*IBM STG, Crolles, France;* [5]*EPFL, Switzerland*

In this paper, extensive characterization of Hot Carrier Injection (HCI) is investigated using flash devices which constitute excellent test structures due to the stored information in the floating gate. A semi-analytical approach has been developed, including a non-local injection model, capable of modeling cell's electrostatics and gate injection currents during program/erase operation regimes.

14:50

7.3 – Gated Diode in Breakdown Voltage Collapse Regime: A Test Vehicle for Oxide Characterisation

A. Rusu[1], M. Badila[2], Alex Rusu[1]

[1]*University Politehnica of Bucarest, Romania;* [2]*On Semiconductors, Santa Clara, USA*

A new method for oxide characterization, based on direct measurement of the flat-band voltage shift is presented. This opportunity appears in the breakdown voltage collapse, for a gated diode operated in the common-cathode configuration. Additionally, the proposed method provides uniform conditions for voltage drop across the oxide and carrier multiplication.

15:10

7.4 – Experimental Procedure for Accurate Trap Density Study by Low Frequency Charge Pumping Measurements

A. Datta[1], F. Driussi[1], D. Esseni[1], G. Molas[2] and E. Nowak[2]

[1]*DIEGM, University of Udine, Italy;* [2]*CEA-LETI MINATEC, Grenoble, France*

Important experimental artifacts due to the gate leakage are identified during Low Frequency Charge Pumping (LFCP) experiments performed on SNOS cells to probe the SiN traps. Gate leakage is shown to impair the LFCP data detected at the S/D and bulk terminals and detailed experimental analysis is carried out on SNOS and MOSFETs to investigate how the effect of the gate leakage can be compensated for to recover reliable LFCP measurements.

15:30–16:00 **Break**

SESSION 8: Variability

16:00–17:00

Co-Chairs: Loren Linholm, *Consultant*
Bill Verzi, *Agilent Technologies, USA*

16:00

8.1 – Device Variability and Correlation Control by Automated Tuning of SPICE Cards to PCM Measurements

A. Revelant[1,2], L. Lucci[1], L. Selmi[2], B. Ankele[1]
[1]*Infineon Technologies Villach, Austria;* [2]*DIEGM University of Udine, Italy*

We present an enhanced methodology to calibrate nominal SPICE models to individual or average PCM measurements at the die, wafer or lot level. The method is validated in a state-of-the-art mixed-signal system-on-chip product development environment for the 65nm CMOS technology node. The proposed approach overcomes previous difficulties in the structured handling of huge amounts of PCM data. It is especially useful to tackle model-hardware correlation problems in a multi-foundry design environment and to complement common tools available to the designers to control process variability such as worst-case corner models and Monte Carlo simulations.

16:20

8.2 – Variation-sensitive Monitor Circuits for Estimation of Die-to-Die Process Variation

I.A.K.M. Mahfuzul[1], A. Tsuchiya[1], K. Kobayashi[2] and H. Onodera[1,3]
[1]*Kyoto University,* [2]*Kyoto Institute of Technology,*
[3]*JST-CREST, Japan*

We propose a set of ring oscillators(RO) with different sensitivities to extract Die-to-Die process parameter variation. We develop an estimation method suitable to extract process parameters from different ROs. We fabricated test structure and successfully extracted process parameter variation. Variation results are correlated with the variation in PCM data.

16:40

8.3 – Simple Current and Capacitance Methods for Bulk FinFET Height Extraction And Correlation to Device Variability

T. Chiarella, B. Parvais, N. Horiguchi, M. Togo, C. Kerner, L. Witters, P. Absil, S. Biesemans, T. Hoffmann
IMEC, Leuven, Belgium

Interest in finFET devices is expected to grow as Moore's law continues to drive the scaling down of logic devices. Both SOI and bulk finFET could fulfill these requirements but device dimension control is expected to penalize the latter. In this work, simple C-V and I-V characterization methods are used to evaluate the fin height impact on performance and variability. Both accurately validate the cross-sectional TEM dimensions and confirm the within wafer variation.

17:00 **End of Session 8**

Conference Banquet

Thursday 7th April

Location: Trippenhuis

08:30–09.00 Registration

SESSION 9: Temperature Characterization

09:00–10:20

Co-Chairs: Colin Mc Andrew, *Motorola, USA*
Stewart Smith, *University of Edinburgh, UK*

09:00

9.1 – Gap-Closing Test Structures for Wafer Temperature Budget Determination

E. J. Faber[1], R.A.M. Wolters[1,2], J.Schmitz[1]

[1] *MESA+ Institute for Nanotechnology, University of Twente,* [2] *NXP Semiconductors, The Netherlands*

We present patterned, parallel metal gap (0.5-3 μm) arrays on thin (50-100 nm) silicon layers as powerless temperature sensors. Initially, these structures have a high resistance but upon temperature exposure the consecutive closing of gaps via confined silicidation results in large resistance drops. These devices are flexible, fast and easy to operate.

09:20

9.2 – High Temperature On-wafer Measurement Structure for DMOS Characterization

C. Boianceanu[1], D. Simon[1], R. Blanaru[1], D. Costachescu[1], M. Pfost[2]

Infineon Technologies Romania, [2] *R. Bosch Center for Power Electronics, Reutlingen univ. Germany*

Modern DMOS transistors for power applications dissipate significant amount of energy, leading to substantial heating. Thus appears the necessity of DMOS characterization at high temperatures. In this paper we present a test structure, with integrated heating elements, used for device characterization up to 500°C.

09:40

9.3 – Design of a Test Chip with Small Embedded Temperature Sensor Structures Realized in a Common-Drain Power Trench Technology

H. Köck[1,4], R. Illing[2], T. Ostermann[2], S. Decker[3], D. Dibra[3], G.Pobegen[1], S. de Filippis[1,5], M. Glavanovics[1], D. Pogany[4]

[1] *Kompetenzzentrum Automobil- und Industrie-Elektronik, Villach;* [2] *Infineon Technologies AG, Villach, Austria;* [3] *Infineon Technologies AG, Neubiberg, Germany;* [4] *TUWien, Austria;* [5] *University of Naples Federico II, Italy*

Two types of novel temperature sensor structures, bipolar and resistive, realized in a common-drain power trench technology are introduced in a test chip. Both sensors integrated into an active DMOS cell array enable accurate transient junction temperature measurements. Different metallization layer compositions facilitate calibrated infrared thermography analysis for verification.

10:00

9.4 – Scalable Thermal Resistance Model for single and multi-finger Silicon-on-Insulator MOSFETs

S. Khandelwal[1], J. Watts[2], E. Tamilmani[3], L. Wagner[4]
[1]*Norwegian Univ. of Science and Technology, Norway;* [2]*IBM Burlington, USA;* [3]*IBM Bangalore, India;* [4]*IBM East Fishkill, USA*

This paper presents thermal resistance model for silicon-on-insulator MOSFETs. The proposed model accounts for various heat dissipation paths in the device accurately and is accurate for both multi and single finger devices. Model development is based on carefully designed test structures to account for different heat dissipations paths. Improvement in the drain current fits across devices when using proposed model over standard BSIMSOI4.3 validates the model.

10:20–10:50 **Break**

SESSION 10: Matching

10:50–12:10

Co-Chairs: Mark Poulter, *National Semiconductor, USA*
Alain Toffoli, *CEA-LETI, France*

10:50

10.1 – Matching Characteristics of Metal Resistors

H. Namba, T. Hashimoto, K. Hayashi, M. Furumiya
Renesas Electronics Corp., Japan

This paper describes feasibility study on metal wiring resistors, mismatch characteristics of metal wiring is investigated. It is found that tungsten resistor fabricated by damascene method has as high precision as poly-silicon and poly-silicon with silicide resistors. Tungsten can provide electrical, mechanical robustness and highly reliable resistors.

11:10

10.2 – Radiation Effects Upon the Mismatch of Identically Laid-out Transistor Pairs

J. Verbeeck[1,2], P. Leroux[2], M. Steyaert[1]
[1]*K.U.Leuven, Dept. ESAT-MICAS;* [2]*K.H.Kempen, Dept. IBW-RELIC, Belgium*

This paper presents the DC behavior of transistors with finger layout and with gate enclosed layout in a 0.18 μm CMOS technology under the influence of gamma-radiation. The threshold voltage shift and the drain current mismatch before and after irradiation has been investigated up to a total ionizing dose of 100kGy.

11:30

10.3 – Novel BJT Test Structure for High Performance Matching Characteristics in CMOS Based Analog Applications

Y.-J. Jung, B.-S. Park, I.-S. Han, H.-M. Kwon, S.-U. Park, J.-D. Bok, Y.-S. Chung[1], M.-G. Lim[1], J.-H. Lee[1] and H.-D. Lee

Chungnam National University; [1]Magnachip Semiconductor Inc., Korea

A novel test structure of bipolar junction transistors based on CMOS technology is proposed for high performance analog circuit applications. The matching characteristics of collector current, IC and current gain β of the proposed structure show improvement of about 31% and 2 %, respectively than those of the conventional structure, although the area of proposed structure is smaller than that of the conventional structure.

11:50

10.4 – Sensing Mobility Mismatch due to Local Interconnect Mechanical Stress in CMOS Technology

S. Blayac[1], C. Rivero[2], P. Fornara[2], L. Lopez[2], N. Demange[2]

[1]Ecole des Mines de Saint Etienne; [2]ST Microelectronics, Rousset, France

For CMOS technology, the increase of interconnects metal density is responsible for heterogeneous mechanical stress fields in active region of silicon. This mismatch originated by interconnects metal lines stress is measured through the use of piezoresistive test structures. Local mechanical stress can thus be monitored in a process control compatible approach.

12:10 **Best paper announcement and closing remarks**

12:30 **Lunch**

14:00 **Excursion**

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Alain Toffoli	CEA/LETI	France
Hans P. Tuinhout	NXP Semiconductors	The Netherlands
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Anthony J. Walton	University of Edinburgh	UK
Larg H. Weiland	PDF Solutions Inc.	USA
Greg M. Yeric	ARM	USA

ICMTS 2011 CONDENSED PROGRAM

Monday, April 4

Time	Event
08:00	Registration
09:00	Introduction
09:05	Test Structure Fundamentals
09:55	Process Qualification
10:45	Break
11:15	MEMS Test Structures
12:05	Nanowire sensors
12:55	Lunch
14:25	Ultrathin Dielectrics
15:15	Efficient Usage of Test Structures
16:05	Ultra Fast IV Characterization
16:55	Closing Remarks
	Welcome Reception

Tuesday, April 5

Time	Event
08:00	Registration
09:00	Opening Remarks
09:10	Session 1 Capacitance (with Invited)
11:10	Exhibitor Presentation
11:20	Break
11:40	Session 2 Yield
12:40	Lunch
14:10	Session 3 Parameter Extraction
15:10	Break
15:40	Session 4 MEMS
17:00	End of Session 4

Wednesday, April 6

Time	Event
08:30	Registration
09:00	Session 5 RF and Noise
10:20	ICMTS 2012 Presentation
10:30	Break
11:00	Session 6 Process Technology (with Invited)
12:40	Lunch
14:10	Session 7 Dielectrics
15:30	Break
16:00	Session 8 Variability
17:00	End of Session 8
	Banquet

Thursday, April 7

Time	Event
08:30	Registration
09:00	Session 9 Temperature Characterization
10:20	Break
10:50	Session 10 Matching
12:10	Best Paper and Closing remarks
12:30	Lunch
14:00	Excursion