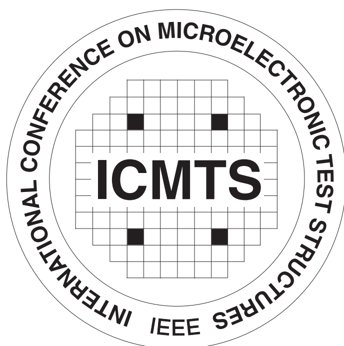
21st ICMTS

2008 IEEE International Conference on Microelectronic Test Structures



March 24-27, 2008
Appleton Tower
The University of Edinburgh
Edinburgh, UK

Sponsored by:
The IEEE Electron Devices Society
The IEEE Solid State Circuits Society

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WELCOME LETTER

Dear Colleagues

The 2008 IEEE International Conference on Microelectronic Test Structures (ICMTS) will be held at the University of Edinburgh, which recently celebrated its 400th anniversary. ICMTS has come of age and this meeting celebrates its 21st anniversary by visiting Edinburgh for the second time. The conference is being run in cooperation with the University of Edinburgh and the Scottish Microelectronics Centre. As was the case for the first ICMTS conference, it is is being sponsored by the IEEE Electron Devices Society, and for the first time the meeting is also being technically co-sponsored by the IEEE Solid State Circuits Society.

The first ICMTS was held in Long Beach in 1988, and since then the conference has cycled between Europe, North America, and Asia. Over the past two decades it has brought together designers and users of test structures to discuss recent developments and future directions. As in previous years the conference will be preceded by a one-day Tutorial Short Course on microelectronic test structures and there will also be a related equipment exhibition focused on test structure measurements. We are very fortunate to be holding the conference banquet in the Playfair Library. Its eleven bays of books supporting a coffered vaulted ceiling make it one of Edinburgh's grandest interiors. The conference will be held at the Appleton Tower in the University of Edinburgh, which is located close the heart of Scotland's capital city.

With its stunning Georgian and Victorian architecture, and winding medieval streets, it's easy to see why Edinburgh has been listed as a World Heritage Site. Edinburgh has one of the most beautiful cityscapes in the world with the famous castle perched atop the crags of an ancient volcano dominating the urban skyline. At the opposite end of "The Royal Mile" lies the Palace of Holyrood. This is the Queen's official residence in Scotland and contains historic apartments where Mary, Queen of Scots lived. The capital is bustling with arts, culture, sports and attractions and is famous for playing host to the world's largest arts festival. The city is the birthplace of James Clerk Maxwell, Sir Arthur Conan Doyle, author of the Sherlock Holmes novels and Alexander Graham Bell, inventor of the telephone. After dark, Edinburgh has a lively nightlife with stylish bars and pubs, restaurants, clubs and live entertainment to rival any European City. We are sure that everyone will enjoy attending the various sessions that make up ICMTS and derive great benefit from the numerous networking opportunities. We look forward to welcoming you to Edinburgh.

Sincerely

Anthony Walton, General Chairman
Jurriaan Schmitz, Technical Chair
Stewart Smith, Conference Vice Chair

GENERAL INFORMATION

Conference Information

The 2008 International Conference on Microelectronic Test Structures is financially sponsored by the IEEE Electron Devices Society with the IEEE Solid State Circuits Society as technical co-sponsors.The conference is also being supported by the University of Edinburgh and the Scottish Microelectronics Centre. The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The Conference will be preceded by a one-day Tutorial Short Course covering a variety of technical areas related to Microelectronic Test Structures.

Website and Email Contacts

ICMTS Website:
 http//:www.see.ed.ac.uk/ICMTS/
General Contact:
 icmts2008@see.ed.ac.uk
Technical Contact:
 icmts2008@ewi.utwente.nl

Presentations

The official language of the conference is English. The ICMTS considers both oral and poster presentations to be of equal value and importance to the conference. The time allowed for oral presentations is 15 minutes with 5 minutes for discussion. All those authors who have been selected for a combined oral and poster presentation should be prepared to make a 5 minute oral presentation describing their research. There will be no questions after the presentation as these will be followed by an opportunity to discuss the work with the author at their poster. It is suggested these talks should be limited to five slides.

Appleton Tower lecture hall

A Windows PC with Microsoft Powerpoint 2003 and Adobe Acrobat 7 will be available in the conference hall. It is highly rec-

ommended that this PC is used to facilitate smooth transitions between presentations. All presentation materials should be sent to icmts2008@ewi.utwente.nl before the 12th March 2008. In addition, all presenters are requested to bring the original files as backup. There will be no 35mm slide projector available. All speakers are requested to report to the registration desk located in front of the conference room before the session begins and ensure that any updates to their presentation files are loaded on the computer system well before the session starts. Poster boards of A0 size will be available for posters.

Both the tutorial and the technical sessions will be held in the University of Edinburgh's Appleton Tower building at 11 Crichton Street (see central area map page 9).

Best Paper Award

Both oral and combination oral/poster papers will be judged by the same criteria in determining the best paper award for the conference. The best paper will be announced at the end of the conference and the award will be made at ICMTS 2009.

Conference Proceedings

The conference proceedings will be published in paper and CD-ROM format. One copy of the paper proceedings and one CD-ROM are included in the registration fee. Additional copies will be available at the conference for £20 per copy.

Conference Registration

Registration Fees

Early Registration (Before January 31st, 2008)

	Member*	Non Member	Student**
Tutorial	£100	£120	£50/£60
Technical Sessions	£250	£280	£150/£180

Late Registration (After February 1st, 2008)

	Member*	Non Member	Student**
Tutorial	£110	£130	£55/£65
Technical Sessions	£280	£310	£175/£205

On-site Registration (Registration at the conference)

	Member*	Non Member	Student**
Tutorial	£120	£140	£60/£70
Technical Sessions	£310	£340	£200/£230

* Must be a member of the IEEE

** Lower prices for student members of IEEE

Registration fees include admission to the technical sessions, equipment exhibits, morning and afternoon coffee breaks, the welcome reception, lunch (Monday – tutorial, Tuesday, Wednesday and Thursday – conference) and the conference banquet. It also includes one paper copy of the proceedings and a CD-ROM.

Payment of Registration Fees

Payment should be made using the University of Edinburgh's on-line payments system:

https://www.era.finance.ed.ac.uk/

which can also be accessed via a link on the ICMTS website:

www.see.ed.ac.uk/ICMTS/

Upon entering the payment web page you will be requested to input an email address and password to create a new account. Further information can be obtained by clicking the link "How to use this site". Once your contact information has been entered you will be presented with a page with drop down menus. Select the specified option from the menus in the following order:

Department: "School of Engineering & Electronics"

Category: "Conference"

Product: "IEEE ICMTS Conference"

Selecting "IEEE ICMTS Conference" will reveal the registration options. Once you have selected one of the options a link marked "Add further comments" should appear at the bottom left corner of the page. If you are an IEEE member please use this to enter your membership number. This option can also be used to inform the organisers of any special dietary requirements or to make any other comment. Once you have selected your registration options and made a payment you will be contacted by email to confirm your registration.

Cancellation

Due to advance financial commitments, refunds of registration fees requested after March 1st, 2008 cannot be guaranteed and will only be considered after the conference. A processing fee of £40 will be deducted from all refunds.

Appleton Tower foyer

Equipment Exhibition

During the conference an equipment exhibition will be held in the foyer outside the conference room in the Appleton Tower. The exhibition will display equipment and systems closely associated with the design, fabrication, analysis and characterisation of test structures.

This equipment exhibition will permit one-on-one discussions between exhibitors and conference attendees on the latest test equipment (for more details see the ICMTS website). The exhibition opening times are given below along with a preliminary list of exhibitors. The full list will be distributed at the conference.

March 24	13:00–17:00	Set up – Tutorial
March 25, 26	9:00–17:00	Conference
March 27	9:00–12:00	Conference and Close-down

Exhibitors List (at time of press)
Agilent Technologies
Cascade Microtech
Celadon Systems
Keithley Instruments
SUSS MicroTec

Messages

If you need to be contacted during the Conference Sessions, a message can be left at the registration desk in the Appleton Tower concourse between the hours of 9:00am and 5:00pm, March 24, 25, 26, and from 9:00 to 12:00pm on March 27. Messages will be placed on a Message Board beside the registration desk.

Messages can be posted for attendees by calling +44-(0)-131-650-5566 or by emailing the conference address icmts08@see.ed.ac.uk

Lunch Venue

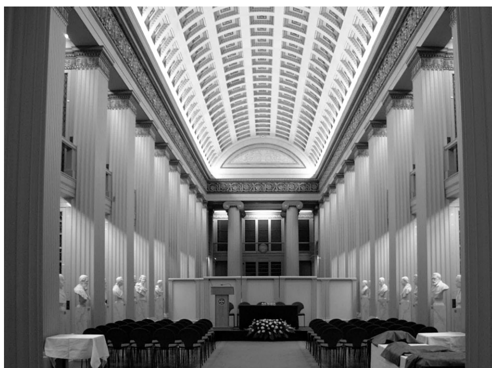
Teviot Row House

During ICMTS the tutorial and conference lunches will be served at Teviot Row House, Bristo Square (see central area map page 9). Colloquially known simply as “Teviot” (pronounced “Tee-vee-ot”) this is one of the Student Union buildings and is run by Edinburgh University Students’ Association (EUSA). Teviot is the oldest purpose built Student Union Building in the world, having been opened on Saturday, October 19th, 1889.

Teviot was built in a 16th Century Scots architectural style with crowstepped gables clasped by drum towers of the Falkland or Holyrood type but with large, late Gothic traceried windows. It has six bars, a canteen, a coffee shop, a debating chamber (used for functions), a dining room, and many other meeting rooms available for booking by student societies.

Conference Banquet

The conference banquet will be held in the Playfair Library Hall situated on the south side of the Old College quadrangle, South Bridge (see central area map page 9). The neo-classical interior of the Library Hall features an arched and coffered ceiling.



Playfair Library Hall

The Hall was designed by William Playfair, renowned also for the Assembly Hall at New College, the Royal Scottish Academy and National Gallery on the Mound, the National Monument on Calton Hill, and the city's Regent, Carlton, and Royal Terraces.

The conference registration fees include one banquet ticket. Guest tickets will be available for sale at the registration desk for £50.

Excursion

Details of the excursion will be published at a later date. If you would like to take part in the excursion please express an interest when registering for the conference. The excursion is planned for 13.30 on Thursday the 27th of March and lunch will be provided from 12.30.

Edinburgh Information

The historic city of Edinburgh is dominated by the Castle, standing high above the surrounding area on the Castle Rock. This is one of two extinct volcanos in the city, the other being Arthur's Seat. Princes Street lies directly beneath the castle with Princes Street gardens

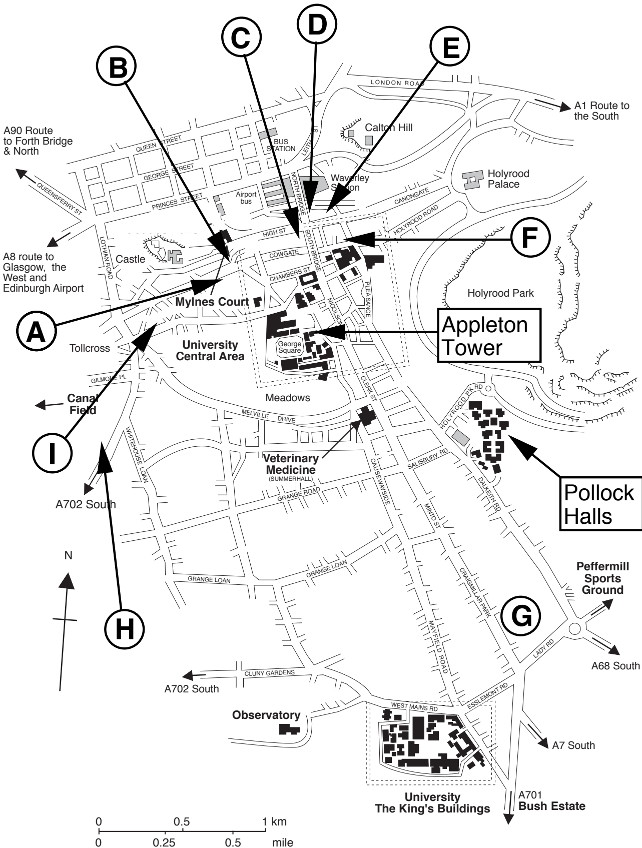
separating the two. This makes Edinburgh perhaps unique with its main shopping street having buildings on only one side of the road.

At opposite ends of the famous Royal Mile are the Castle and Holyrood Palace. The Palace is the Edinburgh home of the Royal Family and is open to visitors when they are not in residence.

Being the capital city, Edinburgh has all the expected amenities such as museums, art galleries, theatres, and gardens as well as being surrounded by a large number of golf courses. Within a short drive is beautiful countryside and coastline together with many historic houses and castles. A few hours drive away is the north of Scotland with the magnificent scenery provided by the mountains, lochs, and islands of the west coast.

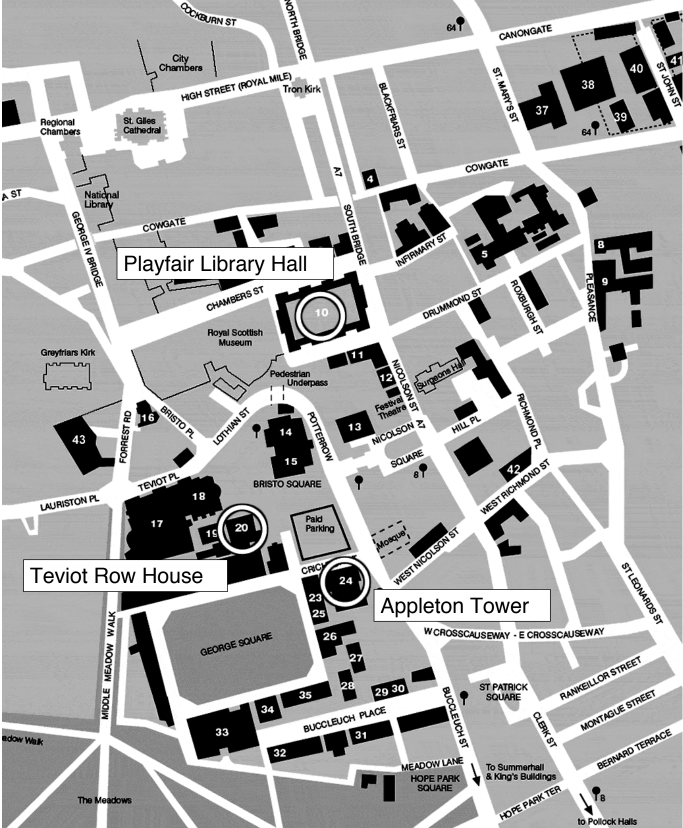
Maps

Edinburgh City Map



The Edinburgh city map shows the main buildings of Edinburgh University, including the College of Science and Engineering at the King's Buildings to the south of the city centre. Highlighted are the locations of a number of hotels; full details can be found in the accommodation section (page 10).

Central Area Map



This map shows the main locations for ICMTS around the University of Edinburgh's central area in the City Centre. Appleton Tower will host the Tutorial and Technical sessions in addition to the welcome reception on Monday the 24th of March. Teviot Row House is one of the main student unions and will be the location for lunch during the tutorial and the three days of the conference. Playfair Library Hall in the University's Old College building is the location for the conference banquet on the evening of the 26th of March.

Climate

The Scottish climate is not renowned for being the most consistent in the world and the temperature in Edinburgh in March can vary from around 10°C (50F) to as low as 1°C (34F) so it is worth bringing warm clothing. Being in the East, the rainfall is much lower than on the West coast of the UK, averaging around 40mm/1.6" in March. That coupled with the fact that Edinburgh can be quite windy means that an umbrella may not be terribly useful.

Accommodation

University Accommodation

A limited number of rooms have been block booked at the University's Pollock Halls of Residence site (See Edinburgh city map on page 8). However, these rooms are only available for the 3 nights of the 24th, 25th and 26th of March. No rooms are available on Sunday 23rd or Thursday 27th. Prices are as follows:

Standard single rooms with shared facilities: £29.00 per night.

Single en-suite bedrooms in Holland House: £39.00 per night.

En-suite bedrooms within Chancellor's Court:
Single occupancy: £49.00, Twin occupancy £69.00.

A full Scottish breakfast is included in the price of the room. Bookings should be made directly with Edinburgh First by calling +44-(0)-131-651-2007. Full payment must be made at the time with a credit card. Please quote "ICMTS 2008" when booking. These rooms are only guaranteed until the 24th of January.

Hotels

There are hundreds of hotels and guest houses in Edinburgh with a wide range of prices and standards. A good place to start looking is the national tourist board website Visit Scotland.
http://www.visitscotland.com/

There are a number of hotels we can recommend either due to proximity to the conference venue or because the university has arranged special rates. See the Edinburgh city map on page 8 for locations. Most of the hotels featured on the "Royal Mile Hotels" website are within walking distance of the conference venue.
http://www.royal-mile-hotels.com/

A: Apex Edinburgh International ****
31-35 Grassmarket
Edinburgh, EH1 2HS
Scotland, UK
Tel: +44-(0)-131-300-3456
Fax: +44-(0)-131-220-5345
Email: edinburgh.reservations@apexhotels.co.uk
Web: http://www.apexhotels.co.uk/
Number of rooms: 171
Prices from about £90

B: The Grassmarket Hotel **

94-96 Grassmarket
Edinburgh, EH1 2JR
Scotland, UK
Tel: +44-(0)-131-220-2299
Can be booked online at a variety of different sites such as expedia.
Number of rooms: 44
Prices from about £50

C: Hotel Ibis Edinburgh Centre **

6 Hunter Square (off Royal Mile)
Edinburgh, EH1 1QW
Scotland, UK
Tel: +44-(0)-131-240-7000
Fax: +44-(0)-131-240-7007
Web: http://www.ibishotel.com/
Number of Rooms: 99
Prices from about £60

D: Barceló Carlton Hotel ****

19 North Bridge
Edinburgh, EH1 1SD
Scotland, UK
Tel: +44-(0)-131-472-3000
Fax: +44-(0)-131-556-2691
Email: carlton@paramount-hotels.co.uk
Web: http://www.paramount-hotels.co.uk/
Number of rooms: 189
The University has an arranged rate for visitors of £89 for a single room, with breakfast. Please contact the conference organisers at ICMTS2008@see.ed.ac.uk to organise bookings.

E: Jury's Inn Edinburgh ***

43 Jeffrey St
Edinburgh, EH1 1DH
Scotland, UK
Tel: +44-(0)-131-200-3300
Fax: +44-(0)-870-701-4444
Web: http://www.jurysinns.com/
Number of Rooms: 186
The University has an arranged rate for visitors of £78 bed and breakfast, but it may be possible to get a cheaper rate online for the room alone. Please mention that you want the Edinburgh University rate when booking and note that this is subject to availability.

F: Express By Holiday Inn: Edinburgh-Royal Mile

300 Cowgate
Edinburgh, EH1 1NA
Scotland, UK
Tel: +44-(0)-870-400-9670
Fax: +44-(0)-141-333-0526
Email: alan.taylor@hiexpressedinburgh.co.uk
Web: http://www.ichotelsgroup.com/h/d/pc/925/en/hd/edbrm
Number of Rooms: 78
Prices from about £68

G: Kildonan Lodge Hotel
27 Craigmillar Park
Newington
Edinburgh, EH16 5PE
Scotland, UK
Tel: +44-(0)-131-667-2793
Fax: +44-(0)-131-667-9777
Email: info@kildonanlodgehotel.co.uk
Web: http://www.kildonanlodgehotel.co.uk/
Number of rooms: 12
Prices from £39 to £65
There are very regular buses running past the hotel into Edinburgh which pass close to Appleton Tower.

H: Best Western Bruntsfield Hotel ****
69 Bruntsfield Place
Edinburgh, EH10 4HH
Scotland, UK
Tel: +44-(0)-131-229-1393
Fax: +44-(0)-131-229-5634
Email: reservations@thebruntsfield.co.uk
Web: http://www.thebruntsfield.co.uk/
Number of rooms: 67
Prices from £80

I: Best Western Edinburgh City Hotel ***
79 Lauriston Place
Edinburgh, EH3 9HZ
Scotland, UK
Tel: +44-(0)-131-622-7979
Fax: +44-(0)-131-622-7900
Email: reservations@bestwesternedinburghcity.co.uk
Web: http://www.bestwesternedinburghcity.co.uk/
Number of rooms: 52
Prices from £160
Business discounts available.

Transportation

Air

Edinburgh International Airport has regular services to many UK and international destinations. There is a dedicated regular bus service (Airlink 100) into the city centre (cost: £3 single, £5 return) which takes you to the Waverley Bridge, next to the railway station. There is also a door-to-door shuttle bus service (£8 single) which will take you right to your hotel. More information on the airport and transport links can be found at:

http://www.edinburghairport.com/
http://www.flybybus.com/
http://www.edinburghshuttle.com/

Rail

All trains arrive at Waverley Station in the centre of the city, although some trains also stop at Haymarket, which is a smaller station in the west end. Walking from Waverley to the central University areas takes approximately 15 minutes, and there are good bus connections to take you further afield.

For comprehensive train information contact National Rail Enquiries on +44-(0)- 8457-48-49-50. They will be able to give you journey details for the whole of the UK, and direct you to the relevant train companies to book tickets. http://www.nationalrail.co.uk/ More general travel information can be found at Traveline Scotland available on +44-(0)-871-200-22-33.

http://www.travelinescotland.com/

Travel Within the City

Lothian Buses provide the main bus services within the City of Edinburgh. Their website (address below) provides a journey planner or you can call them on +44-(0)-131-555-6363, just tell them where you are and where you want to go, and you'll be told all you need to know. The buses do not give any change - the single flat rate fare for anywhere in the city is £1 while a day ticket is £2.50.

http://www.lothianbuses.co.uk/

Buses that run close to Appleton Tower include the 41 and 42 on Potterow/Buccleuch St. and a number of different buses which run along Clerk St., such as the 3, 5, 7, 8, 14, 30, 31, 33, 37, 47 and 49.

TUTORIALS

Tutorial Lecturer Biographies

Richard A. Allen

Since receiving his B.S. and M.S. degrees (both in Physics) Richard Allen has worked in the development of microelectronic test structures, first at the Jet Propulsion Laboratory in Pasadena, California and since 1990 at the National Institute of Standards and Technology, Gaithersburg, Maryland. At JPL, his research was in the development of test structures for in-situ monitoring space radiation effects; at NIST, his research has been in test structures for metrology applications for VLSI, microfluidics, and MEMS applications. He served as Tutorial Chair for the 2006 ICMTS.

Joost van Beek

Ir. Joost van Beek (1969) received his MSc degree in Applied Physics and a Degree in Technological Design from the Technical University of Eindhoven. From 1996 to 1998 Joost van Beek held a post-doc position at the Massachusetts Institute of Technology. At MIT he worked in the field of micro-machining of UV blocking filters for space applications. From 1998 till 2006 he was a Senior Scientist at Philips Research, now NXP, and was active in the field of RF Integrated Passive Devices and MEMS switches. Currently, Joost van Beek is a Senior Scientist at NXP Semiconductors and is involved in research on MEMS oscillators and filters.

Colin McAndrew

Colin McAndrew received the Ph.D. degree in Systems Design Engineering from the University of Waterloo, Ontario, Canada, in 1984. From 1987 to 1995 he was at AT&T Bell Laboratories, Allentown PA. Since 1995 he has been with Freescale Semiconductor (formerly Motorola), in Tempe, AZ. He received best paper awards for ICMTS in 1993 and CICC in 2002, and the BCTM Award in 2005. He is a Fellow of the IEEE, an editor of the IEEE Transactions on Electron Devices, and is or has been on the technical program committees for the IEEE BCTM, ICMTS, CICC, and BMAS conferences.

Luca Selmi

Luca Selmi received the PhD in Electronic Engineering from the University of Bologna in 1992. In 2000 he became Full Professor of Electronics at the University of Udine, Italy. During 1989-1990 he was a visiting scientist at Hewlett Packard Microwave Technology Division, Santa Rosa, California where he worked on the characterization of high frequency III-V devices and the design of RF integrated circuits. In 1995-1996 he was a member of the technical subcommittee on "Modeling and Simulation" of the IEEE International Electron Device Meeting (IEDM). In 2001-2002 he was a member of the technical subcommittee on "Circuit and Interconnect Reliability" of the

same conference. He has been or still is TPC member of the Semiconductor Interface Specialist Conference (SISC) of the Insulating Films on Semiconductors Conference (INFOS) and of the "Characterization and Reliability" subcommittee of the European Solid State Research Conference (ESSDERC). Luca Selmi's research interests include characterization, modeling and simulation of silicon devices, with emphasis on transport phenomena, Monte Carlo transport simulation techniques and hot carrier effects in MOSFETs, silicon bipolars and Non Volatile Memory cells, quasi ballistic transport in nanoMOSFETs, CHE and CHISEL injection in MOSFETs and NVM cells, hot electron effects at low voltages, gate leakage currents and reliability of ultra thin oxides, Bulk and SOI MOSFET scaling in the deca-nanometer range.

Luca Selmi co-authored approximately 150 papers on refereed international journals (mostly IEEE-TED, IEEE-EDL) and proceedings of major international conference, including approximately 30 papers at the International Electron Devices Meeting (IEDM) two of which invited, and 1 book chapter on Flash memory cells. He holds one US and international patent. Luca Selmi is a member of IEEE Electron Device Society.

Peter J. Hulbert

Peter J. Hulbert is a Semiconductor Applications Engineer with Keithley Instruments in Cleveland. He received his bachelors degree in Physics from Washington State University, and has held various positions at Keithley associated with semiconductors and their application. He can be reached at phulbert@keithley.com.

Henk van Zeijl

Dr. ing. H.W. van Zeijl studied at the poly technical institute Rijswijk where he received the B.S. degree in physics in 1981. In that year he joined the Interuniversity reactor institute in Delft where he worked in the field of neutron diffraction and instrumental neutron activation analysis. In 1986 he joined the Delft Institute of Microelectronics and Submicron technology (DIMES). From 1989 till 1998 he was responsible for the mask fabrication and lithography in the DIMES IC process research sector. During that period he assisted in different research programs. In 1998 he developed a lithography course "Applied I-line lithography", two years later the course "Integrated circuit fabrication technology". These courses, both full week training for engineers from relevant fields in the industry are held for more than forty times and are also transferred to the Tshinghua University in Beijing. Besides these educational activities he cooperated in different research project related to Lithography and MEMs. In 2005 he completed his PhD thesis entitled "Bipolar transistors with self aligned emitter-base metallization and back-wafer-aligned collector contacts" and is now a senior researcher at DIMES. Currently he is involved in different research projects related to MEMs and 3D integration and was recently appointed as a lecturer. He is a (co-)author of more than 40 technical papers.

Christopher Hess

Christopher Hess received the diploma degree in electrical engineering from the University of Karlsruhe, Germany in 1992, and the Dr.-Ing. (Ph.D.) degree in computer science from the University of Karlsruhe, Germany in 1998. In 1992 he was a founding member of the Defect Diagnosis Group at the University of Karlsruhe. In 1998 he joined PDF Solutions in San Jose, CA. As a Fellow he is currently responsible for Yield & Performance Characterization.

Since 1992, he has been involved in the design of more than 100 test chips for the microelectronics industry over numerous technologies. For years, his main R&D focus is on efficient merging of experiments by minimizing chip area usage and manufacturing cycle time. His activities also include developing new architectures of testing equipment providing several orders of magnitude more data from high density test chips compared to testing traditional stand alone experiments. Most recently he is working on high density test chips for scribe line applications.

Dr. Hess has published about 40 conference and journal papers and he holds 10 patents. He is a member of the IEEE and the Electron Device Society as well as a technical committee member of several semiconductor manufacturing related conferences. He has served as Technical Chairman of the 2000 International Conference on Microelectronic Test Structures (ICMTS) and General Chairman of ICMTS in 2003.

Robin Degraeve

Robin Degraeve received the M.Sc. degree in electrical engineering from the University of Gent, Belgium, in 1992, and the Ph.D. degree from the Catholic University of Leuven, Belgium, in 1998.

He joined the Interuniversity Microelectronics Center (IMEC), Leuven, in 1992 in the CMOS Reliability and Characterization group, where he is currently working as a Senior Researcher. His work has been focusing on reliability aspects of thin insulating layers under electrical stress. His current interests and activities include hot-carrier related reliability issues in MOSFETs, the study of the physics of degradation and breakdown phenomena in gate oxide films, the reliability of flash memory devices, the reliability of ultrathin oxide and oxynitride layers for VLSI technologies, and the reliability of high-k materials as gate insulators for future CMOS generations and memory applications.

Tutorial Program

Monday, March 24th

Location: Appleton Tower

08:00–17.00 Registration

09:00 Introduction – Johan Klootwijk, *Philips Research Europe*

09:05

1. Test Structure Fundamentals

Richard A. Allen, *National Institute of Standards and Technology, USA*

This presentation will begin with a review of test structures detailing their history and hot topics over the past 20 years. The presentation will include a description of test structures for measuring sheet resistance, line width and contact resistance. Measurement and equipment developments will also be addressed, focusing on procedures for obtaining accurate and repeatable measurements.

09.55

2. MEMS Test Structures

Joost van Beek, *NXP Semiconductors, The Netherlands*

This tutorial addresses test and characterization techniques unique to MEMS. Emphasis is put on the characterization of MEMS switches and resonators and their hermetic package. Methods to investigate electro-mechanical characteristics, failure modes, and lifetime of this specific class of MEMS will be elaborated.

10.45 Break

11:15

3. Spice Modeling: Best Practices and Circuit Simulation Basics

Colin McAndrew, *Freescale Semiconductor, USA*

Historically, for the most part SPICE "modeling" meant extraction of parameters of models, and only a small number of people actually developed the SPICE models (equations and code). The advent of Verilog-A has meant that many process design kits (PDKs) now come with customized models that vary from the very simple (interface elements or simple polynomial nonlinear resistor and capacitor models, for example) to the very complex (drift-region resistance and charge models for LDMOS devices, for example). And customized Verilog-A models are required for mixed-discipline elements for which there are no basic SPICE models, e.g. MEMs devices and LCDs. So more people are now becoming involved with SPICE model development. Writing a good model requires an understanding of how circuit simulators work, and of what are the appropriate capabilities of Verilog-A to use (and to not use!). This tutorial provides on overview of SPICE simulation algorithms and how SPICE works, to help guide making high-level choices related to how to structure and formulate models. The tutorial also provides a detailed, low-level look at common issues and problems in models, as examples of how NOT to write models, and details best practices for writing good models.

12:05

4. Characterization of Mobility and Carrier Transport properties of Ultra Thin Body MOS Devices

Luca Selmi, *University of Undine, Italy*

The Ultra Thin Body MOSFET, operated in either single or double gate mode, is nowadays regarded as the most promising device architecture at the scaling limit. In these devices the drain current is confined in a thin semiconducting layer where the electron and hole transport properties are affected by size and bias induced quantization. In order to boost the I_{on} of UTB MOSFETs, an appropriate choice of channel semiconductor material (Si, SiGe, Ge, III-V), crystal orientation and strain has to be adopted and optimized in combination with the film thickness. All these possibilities have recently raised widespread interest in the characterization and modelling of transport in ultra thin films.

The presentation will review test structures and characterization methods commonly adopted to investigate the carrier transport properties of both long channel and short channel UTB devices. Simple design criteria for optimized test structures will be illustrated. The impact on the results of the choice of appropriate operating conditions for single or double gate devices will also be addressed.

12.55 Lunch

14:25

5. Pulsed IV Characterization

Peter J. Hulbert, *Keithley Instruments, USA*

This tutorial will introduce concepts used for pulse-based testing on semiconductor devices. It will start with definitions of DC and pulse testing, and then extend to cover common pulse test approaches. The tutorial will conclude with some common pulse applications along with a “tips & tricks” section.

15:15

6. Through Wafer Vias for System in Package

Henk van Zeijl, *Delft University of Technology, The Netherlands*

For emerging technologies like 3D integration, dual side processing and through wafer etching are key enabling technologies. Contrary to single side processing, there are no adequate optical procedures to evaluate the post etch dual side overlay (the registration between 2 lithographic layers). Nevertheless, to measure this overlay, electrical line width measurement (ELM) principles are applied on a multi-resistor test structure. Moreover, with this multi resistor design, not only post etch dual side overlay, but also post etch dimensions can be measured. In this tutorial, the design, process integration, electrical characterization and application of dual side electrical overlay test structures is discussed.

After a brief introduction to the ELM principle and limitations, the operating principle of the electrical overlay test structure is explained. To integrate such a structure in a through wafer etch process, either with anisotropic wet etching or deep reactive ion etching (DRIE), the thin film resistor material must

be compatible with these processes. However, the choice of thin film material has consequences for the electrical probing. Furthermore, the etch process may distort the geometry of the resistors into shapes like taper, bow or edge roughness that will affect the measurement accuracy. The above mentioned material and geometry issues and solutions will be discussed.

Finally the applications of the electrical test structure in through wafer etch processes like anisotropic wet etching with KOH and DRIE, the results and etch process characteristics will be discussed in this tutorial as well.

16:05 Break

16:35

7. Efficient Usage of Test Structures

Christopher Hess, *PDF Solutions, USA*

Test Structures are used for an ever increasing set of applications. Thus, more and more test structures have to be designed, manufactured, tested and analyzed. Focusing on Yield and Variability, the Tutorial will give an overview how to balance and manage the following challenges:

1. Increase the Number of Experiments

2. Decrease Mask Cost

3. Decrease Test Time

4. Faster Data Feedback

17:25

8. Measurement and analysis of thin (sub 10 nm) insulating layer degradation

Robin Degraeve, *IMEC, Belgium*

Electrical stress causes the formation of defects in thin insulating layers (SiO_2, SiON or stacks containing high-k dielectrics), resulting in increased leakage current and finally complete dielectric breakdown. This tutorial aims at presenting an overview of the different stages of dielectric degradation. Depending on the (test) devices used, different measurement techniques are needed to observe oxide degradation. The tutorial further focuses on basic statistical analysis of data and consequent optimisation of the test structures.

18:15 Closing Remarks

WELCOME RECEPTION

Monday, March 24th

Location: Appleton Tower

18:30-20:00 Welcome Reception - Scotch Whisky Tasting

In order to welcome you to ICMTS 2008 and give you a taste of Scotland this event is an opportunity to sample a number of Scotch Malt Whiskies and learn more about the process by which they are produced. Other refreshments will also be provided.

TECHNICAL PROGRAM

Tuesday 25th March

Location: Appleton Tower

08:00–17.00 Registration

09:00 Opening Remarks
Anthony J. Walton, General Chairman
Jurriaan Schmitz, Technical Program Chairman

SESSION 1: Matching I – Characterisation

09:10–10:30
Co-Chairs: Greg M. Yeric, *Synopsys, USA*
Hans P. Tuinhout, *NXP-TSMC Research Center, The Netherlands*

09:10

1.1 – Operational Amplifier Based Test Structure For Transistor Threshold Voltage Variation

Brian L. Ji, Dale J. Pearson, Isaac Lauer, Franco Stellari, David J. Frank, Leland Chang, and Mark B. Ketchen
IBM T.J. Watson Research Center, NY, USA

We have developed a new test structure comprising MOSFET arrays and on-chip operational amplifier feedback loop for measuring threshold voltage variation. The test structure also includes an on-chip clock generator and address decoders to scan through the arrays. It can be used in inline test environment to provide rapid assessment on Vt variations for technology development and chip manufacturing. Hardware results on 65nm technology node are presented.

09:30

1.2 – A Study of Variation in Characteristics and Subthreshold Humps for 65-nm SRAM Using Newly Developed SRAM Cell Array Test Structure

A. Mizumura[1], T. Suzuki[1], T. Arima[2], H. Maeda[2], and H. Ammo[1]
[1]*Semiconductor Technology Development Division, Sony Corp.* [2]*Sony LSI Design Incorporated, Kanagawa, Japan*

Variation in the characteristics (Vth and Ion) of driver and load MOSFETs in SRAM cells was investigated by using a newly developed SRAM cell array test structure and is reported here for the first time. Subthreshold humps were also monitored in SRAM cells with an algorithm that can automatically recognize the occurrence of humps. By extracting the variations in MOSFET characteristics and by estimating the impact of subthreshold humps in SRAM cells, it is possible to design SRAM circuits more accurately.

09:50

1.3 – Mismatch Characterization of a High Precision Resistor Array Test Structure

Weidong Tian, Philipp Steinmann, Eric Beach, Imran Khan and Praful Madhani

Texas Instruments Inc. USA

In this paper we will describe a 2x(2xn) pads resistor array test structure. It provides a flexible and convenient way to study resistors in an array. We will focus on various matching properties of the precision thin film resistors, specifically, between two resistors (neighbor and far away pair), between two resistor combinations, and between any one of the resistors with the average of the whole array. Both random and systematic mismatch properties are studied. In addition, we will illustrate key factors for resistor matching from both process and layout perspective. The array layout can be copied directly from and into a circuit design.

10:10

1.4 – Rapid Characterization of Parametric Distributions Using a Multi-meter

Jerry Hayes, Kanak Agarwal, Sani Nassif

IBM Austin Research Labs, TX, USA

A technique is presented for fast, direct characterization of the statistical mean and sigma of parametric distributions using standard multi-meter test equipment. The technique is shown to be sufficiently general and can be applied to a wide range of characterization strategies.

10:30–11:00 **Break**

SESSION 2: Resistivity

11:00–12:00

Co-Chairs: Satoshi Habu, *Agilent Technologies, Japan*
Richard A. Allen, *NIST, USA*

11:00

2.1 – Beyond van der Pauw: Sheet Resistance Determination of Arbitrarily Shaped Planar Four-Terminal Devices with Extended Contacts

Martin Cornils and Oliver Paul

Department of Microsystems Engineering (IMTEK), University of Freiburg, Germany

We report an extension of van der Pauw's method to determine the sheet resistance R_{sq} from arbitrarily shaped planar devices with four extended peripheral contacts. By performing six independent electrical resistance measurements on such devices, followed by the simultaneous solution of six transcendental equations, R_{sq} is straightforwardly extracted. The method uses conformal mapping in combination with the method of images. It was successfully applied to CMOS test structures and is supported by finite-element analysis.

11:20

2.2 – Investigation of Electrical and Optical CD Measurement Techniques for the Characterisation of On-Mask GHOST Proximity Corrected Features

A. Tsiamis[1], S. Smith[1], M. McCallum[2], A.C. Hourd[3], O. Toublan[4], J.T.M. Stevenson[1] and A.J. Walton[1]

[1] *The University of Edinburgh,* [2] *Nikon Precision Europe GmbH,* [3] *Compugraphics International Ltd., UK* [4] *Mentor Graphics Ltd., France*

This paper reports the measurement results from a set of electrical, on-mask test structures based on industry standard test feature layouts normally used to investigate process proximity effects and improve optical proximity correction (OPC) models. The electrical test structures were fabricated on a binary photomask using the GHOST proximity correction technique to compensate for typical e-beam induced proximity errors. This is one of the first times that electrical test structures have been used to evaluate GHOST exposure. The test structures were measured electrically and optically with a dedicated photomask metrology tool and the results from the two techniques are presented.

11:40

2.3 – Comparison of Measurement Techniques for Advanced Photomask Metrology

S. Smith[1], A. Tsiamis[1], M. McCallum[2], A.C. Hourd[3], J.T.M. Stevenson[1], A.J. Walton[1], R.G. Dixson[4], R.A. Allen[4], J.E. Potzick[4], M.W. Cresswell[4] and N.G. Orji[4]

[1] *The University of Edinburgh,* [2] *Nikon Precision Europe GmbH,* [3] *Compugraphics International Ltd.,* [4] *National Institute of Standards and Technology*

This paper compares electrical, optical and AFM measurements of critical dimension (CD) made on a chrome on quartz photomask. Test structures suitable for direct, on-mask electrical probing have been measured using the three techniques and the results show very good agreement between the electrical measurements and those made with a calibrated CD-AFM system.

12:00–13:30 **Lunch**

SESSION 3: Yield and Reliability I

13:30–14:50

Co-Chairs: Christopher Hess, *PDF Solutions, USA*
Kelvin Yih-Yuh Doong, *TSMC, Taiwan*

13:30

3.1 – Electromigration : from package to wafer level thanks to a heating coil structure

C. Chappaz, P. Waltz, L. Castellon

STMicroelectronics, Crolles CEDEX, France

An efficient and precise method for Black's parameters extraction at wafer level is proposed. Using an innovative device including a standard NIST with a dedicated heating coil, electromigration tests can be successfully leaded at wafer level for

activation energy (Ea) and current acceleration factor (n) extraction. Comparison with package results emphasizes a very good behavior of the structure.

13:50

3.2 – Life condition monitoring on smart power devices using a sequence of current and charge-based capacitance measurements

Zhenqiu Ning[1], Erwin de Vylder[1], Filip Bauwens[1], Basil Vlachakis[1], H-X Delecourt[1], Renaud Gillon[1], Patrick Van Torre[2] and Dan Hegsted[1]

[1]*AMI Semiconductor Belgium bvba, Belgium,* [2]*Hogeschool Gent, Belgium*

The precise life condition monitoring on smart power devices is important for smart power circuit design. To perform such a monitoring, a technique based on charge-based capacitance measurement has been developed, by which all DC, AC measurements and stress are implemented in sequence on one single device. Measurement, accelerated stress and re-measurement are repeated on a logarithmic time sequence, and key parameters for the life condition monitoring are extracted. The degradation of the key parameters is characterized as a measure for the life condition monitoring.

14:10

3.3 – Mixed Test Structure for Process Variation and Hard Defect Detection

F. Rigaud[1,2], J.M. Portal[1], H. Aziza[1], D. Née[2], J. Vast[2], F. Argoud[2], B. Borot[3]

[1]*L2MP - Laboratoire Matériaux et Microélectronique de Provence,* [2]*STMicroelectronics, Rousset,* [3]*STMicroelectronics, Crolles, France*

The objective of this paper is to present a mixed test structure designed to characterize yield loss due to hard defect and back-end process variation (PV) at die and wafer level. A brief overview of the structure, designed in a STMicroelectronics 130nm technology, is given. This structure is based on a SRAM memory array for hard defect detection. Moreover each memory cell can be configured in Ring Oscillator (RO) mode for back-end PV characterization. The structure is tested in both modes (SRAM, RO) using a single test flow. Experimental results are given and confirm the ability of the structure to monitor PV and defect density.

14:30

3.4 – Short-flow Test Chip Utilizing Fast Testing for Random Defect Density Monitoring in 45nm

Muthu Karthikeyan[1], William Cote[1], Louis Medina[1], Amy Henning[1], William Ferrante[1], Mark Craig[2], and Thomas Merbeth[3]

[1]*IBM Systems and Technology Group, NY, USA,* [2]*AMD Austin, TX, USA,* [3]*AMD Saxony, Dresden, Germany*

We describe the development and use of a comprehensive 45nm short-flow test chip to improve random defect limited yield.

The DC test structures are tested in parallel-mode using the per-pin Parametric Measurement Unit of a functional tester, resulting in a 4x reduction in test time over conventional parametric testing. The large critical area test structures enable reliable measurement of defect densities by failure mechanism. The short cycle time makes this test chip an excellent routine defect monitor as well as a useful vehicle for validating process changes.

14:50–15:20 **Break**

SESSION 4: Poster Presentations

15:20–15:55

Co-Chairs: Akis Doganis, *TSMC, Taiwan*
Yoichi Tamaki, *Hitachi Ltd., Japan*

15:20

4.1 – Conduit Diffusion of Dopants in Tungsten Silicide Layers

S. Liao, M. Bain, D.W. McNeill, B.M. Armstrong and H.S. Gamble

Queen's University Belfast, UK

Novel test diode structures have been manufactured to characterise conduit diffusion in tungsten silicide layers. Bipolar diode action has indicated that long-range diffusion of phosphorus ($\sim 38.5\mu$m) has been achieved experimentally for anneal schedules of 30 minutes at 9000C. The concept of conduit diffusion has been demonstrated experimentally for application in advanced bipolar transistor technology.

15:25

4.2 – A Novel High Speed Automatic Layout System to Place and Route Test Structures for Parametric Test Capability

Andrew J. West[1], Samrat Mondal[2], Devjyoti Patra[2], Kalyan Goswami[2] and Shamik Sural[2]

[1]*National Semiconductor Corp, Santa Clara, CA, USA,* [2]*Indian Institute of Technology, Kharagpur, India*

In this paper, we have created a generalized framework for the automated placement and routing of analog test structures. We have exploited the concept of terminal properties when placing and routing the test structures and generated a library of place and routing strategies for different architectures. This new approach significantly reduces layout time, maximizes the re-use of place and route routines and facilitates the introduction of a holistic parametric test design flow.

15:30

4.3 – A Test Structure for Channel Length Engineering of NAND Gates in Standard Cell Library

T. Matsuda[1], Y. Sugiyama[1], J. Takakuwa[1], H. Iwata[1], T. Ohzone[2]

[1]*Department of Information Systems Engineering, Toyama Prefectural University,* [2]*Dawn Enterprise, Japan*

A channel length engineering technique for optimization of primitive cells in standard cell libraries is proposed and a test

structure to analyze the operation performance and leakage current of 3-input NAND is presented. Since the topmost transistor N1 in the three series connected n-MOSFETs in 3-input NAND has the largest V_{DS}, subthreshold leakage current can be reduced by optimizing L (N1). The leakage current of NANDs for input vector of (0, 1, 1) decreases by about 22 $\sim$ 40% with the change of L (N1) from 0.1 to 0.11 μm. The channel length engineering of series connected MOSFETs provides a leakage reduction method for standard cells without area overhead and large increase of delay time.

15:35

4.4 – Test Structure for Characterising Low Voltage Coplanar EWOD System

Yifan Li[1], Yoshio Mita[1,2], Les Haworth[1], William Parkes[1], Masanori Kubota[2], Anthony Walton[1]
[1] *University of Edinburgh, UK,* [2] *University of Tokyo, Japan*

This paper presents test structures designed for studying the relationship between the operation voltage and the configuration of electrode area for coplanar EWOD (ElectroWetting On Dielectrics) devices. Robust anodic Ta_2O_5 dielectric and thin aFP (amorphous fluoropolymer) have been used to fabricate the structures. Test structures have been used to characterise the significant contact angle change on asymmetric configurations, 114° to 81° on CYTOP (aFP from Asahi Glass Co. Ltd.) with less than 20V applied. This demonstrates that by modifying the design, the operating voltage can be reduced by nearly half, compared to the existing symmetric coplanar EWOD structures. Droplet manipulation on a coplanar EWOD system with this new design has been successfully demonstrated, with a driving voltage of 15V.

15:40

4.5 – Measurement of the MOSFET Drain Current Variation Under High Gate Voltage

Tetsuo Chagawa[1], Kazuo Terada[1], Jianyu Xiang[1], Katsuhiro Tsuji[1], Takaaki Tsunomura[2] and Akio Nishida[2]
[1] *Faculty of Information Sciences, Hiroshima City University, Japan,* [2] *MIRAI-Selete, Tsukuba, Japan*

The method for accurately measuring the drain current of the MOSFETs, which are integrated in an array and are biased at high gate voltage, is studied. Feedback loop in Kelvin connection is made by software to obtain both accurate and stable measurement. The experimental data show that the software-Kelvin method is accurate and it is applicable to evaluate the accuracy of fast hardware-Kelvin measurement.

15:45

4.6 – Spacing Impact on MOSFET Mismatch

A. Cathignol[1,3] , S. Mennillo[2], S. Bordez[1], L. Vendrame[2], G. Ghibaudo[3]
[1] *STMicroelectronics, Crolles, France,* [2] *STMicroelectronics, Advanced R&D, Italy,* [3] *IMEP, Minatec, Grenoble, France*

Many test structures embedded in various technologies were measured to study the spacing impact on MOSFET mismatch. This impact is showed to highly depend on technology, device

family, device type and bias conditions. The analysis of spatial correlation allows to properly model spacing impact on many devices mismatch. Finally, a worst case model that only requires standard matched pairs at minimum spacing is proposed to provide designers the maximum matching degradation that may affect spaced devices.

15:50

4.7 – Highly Automated Test Chip Layout and Test Plan Development for Parametric Electrical Test

Ann Gabrys, Wendy Greig, Andrew J. West, Philipp Lindorfer, and William French

National Semiconductor Corp., Santa Clara, CA, USA

This work outlines a fully integrated device development procedure that automates test chip development, including placement and routing algorithms, and electrical test program generation. This procedure improves over classic test chip and electrical test program development by reducing the development timeline and allowing more complete and elegant experimental device design, as well as eliminating many of the opportunities for human error while maximizing reuse between technologies.

15:55

4.8 – Circular Geometry MOS Transistor Analysis of SOI Substrates for High Energy Physics Particle Detectors

S.L. Suder[1], F.H. Ruddell[1], J.H. Montgomery[1], B.M. Armstrong[1], H.S. Gamble[1], G. Casse[2], T. Bowcock[2], P.P. Allport[2]

[1]*Northern Ireland Semiconductor Research Centre, Queen's University Belfast, UK,* [2]*Liverpool Detector Centre, University of Liverpool, UK*

SOI substrates are important for the fabrication of monolithic active pixel high energy physics particle detectors. In this work self-aligned circular geometry MOS transistor test structures were fabricated on ion split bonded SOI substrates to evaluate the interface between the high resistivity handle silicon and the SOI buried oxide. Pre- and post- proton irradiation transistor measurements are presented, showing an increased SOI buried oxide trapped charge of only $3.45 \times 10^{11}\mathrm{cm}^{-2}$ for a dose of 2.7 Mrad.

16:00–16:30 **Exhibition Presentations**

16:30–18:00 **Poster and Exhibition Session**

Wednesday 26th March

Location: Appleton Tower

08:30–17.00 Registration

SESSION 5: 3D Integration

09:00–10:20

Co-Chairs: Yoshio Mita, *University of Tokyo, Japan*
Emilio Lora-Tamayo, *Universitat Autonoma de Barcelona, Spain*

09:00

5.1 – Prediction of Stress-Induced Characteristics Changes for Small-scale Analog IC

Naohiro Ueda, Hideyuki Aota, Eri Nishiyama, Hirobumi Watanabe

Electronic Devices Company, Ricoh Co. Ltd., Japan

Stress-induced parametric changes during the resin-molded packaging of a small-scale integrated circuit (IC), which is smaller than 1.0mm^2, have been evaluated by a specially designed test chip. Multiple test chips with different resistor locations have been fabricated, measured by die-to-die correspondence and one contour plot was reproduced from the measurement results. This paper shows the distribution of parametric change for the small scale IC. In addition, a new method for evaluating the circuit performance change due to stress-induced parametric changes is presented.

09:20

5.2 – Test Structures for the Measurement and Optimisation of Bond Strength for Anodic Bonding of Glass to Dielectric Thin Films

G. Cummins, H. Lin and A.J. Walton

The University of Edinburgh, UK

This paper presents results of the use of test structures to characterize and optimize parameters for anodic bonding of thin dielectric films (rather than silicon) to glass. These test structures consist of a single titanium layer, rather than the aluminium/silicon nitride layers previously reported, which is stepped regularly across the film surface. These structures have been optically analysed to provide non-destructive information about the bond strength obtained through the different process steps.

09:40

5.3 – Test Structures For The Evaluation Of 3D Chip Interconnection Schemes

A. Mathewson[1], J. Brun[1], G. Ponthenier[1], R. Franiatte[1], A. Nowodzinski[1], N. Sillon[1], F. Depoutot[2] and B. Dubois-Bonvalot[2]

[1]*CEA-Leti-Minatec, Grenoble,* [2]*Hardware Research Group, Gemalto, Grenoble, France*

In this paper a test structure is described which facilitates the evaluation of interconnection schemes for chip on wafer attachment and interconnection. Microinsert technology is described

and some of the characterization that the test structure permits is discussed. Thermal cycling experiments were performed on this test structure and although the resistance of the contact chain seemed not to change as a function of number of cycles, detailed investigation revealed that the metal resistance was reducing while contact resistance was increasing and the two effects were trading off against each other. Possible explanations for this behavior have been provided.

10:00

5.4 – An Evaluation of Test Structures for Measuring the Contact Resistance of 3-D Bonded Interconnects

H. Lin, S. Smith, J.T.M. Stevenson, A.M. Gundlach, C.C. Dunare, and A.J. Walton

The University of Edinburgh, UK

This paper evaluates test structures designed to characterise electrical contacts between interconnect on bonded wafers. Both simulation and experimental measurements are used to explore the capability of a stacked Greek cross type test structure to extract the contact resistivity between two bonded conductive layers. It is concluded from the simulations and actual electrical measurements of the benchmark Kelvin structures that the stacked Greek cross can only be used where there is a relatively high specific contact resistivity. For the structures evaluated in this study, this was found to be greater than $\rho_c \geq 2.0 \times 10^{-8} \Omega.\text{cm}^2$.

10:20–10:50 **Break**

SESSION 6: Yield and Reliability II

10:50–12:10

Co-Chairs: Kiyoshi Takeuchi, *NEC Corp., Japan*
Alan Mathewson, *Tyndall National Institute, Ireland*

10:50

6.1 – High Density Test Structure Array for Accurate Detection and Localization of Soft Fails

Christopher Hess[1], Michele Squcciarini[1], Shia Yu[1], Jianjun Cheng[2], Ron Lindley[2], Andrew Swimmer[2], Steven Winters[2]

[1]*PDF Solutions Inc., San Jose, CA 95110, USA,* [2]*PDF Solutions Inc., San Diego, CA 92128, USA*

To resolve performance yield issues it is required to detect and localize soft fails such as a contacts having 500ohms instead of its nominal 50ohms. Soft fails can only be detected within very small test structures, which requires an array design to efficiently use the area of test chips. Here we present a novel High Density Test Structure Array, which will enable accurate 4 terminal measurements of 1000 or more very small devices under test (DUT) within each array. On average, only 2 selection devices are required per DUT, which will provide outstanding utilization of the test chip area.

11:10

6.2 – New method for non destructive snap-back characterization in multifinger power MOSFETs

Frangois Dieudonné, Aurore Constant, Julien Rosa, Benoit Gautheron

STMicroelectronics, Crolles, France

In this paper, we have implemented a non destructive conductance based electrical characterization method of the snap-back phenomenon on dedicated multi-finger power MOSFETs. The context of the study is firstly presented, and then the specific test structures along with the measurement methodology are shown. The robustness and repeatability of our approach is demonstrated on a variety of power N- & P-MOSFETs regarding to some technological parameters. Comparisons between our results and the ones provided by a destructive characterization are also drawn. The temperature's influence on snap-back will be demonstrated in the final paper as well as repeatability in terms of contact sensitivity and potential hot-carrier induced stress during measurements.

11:30

6.3 – Test Circuit for Measuring Pulse Widths of Single-Event Transients Causing Soft Errors

Balaji Narasimham, Matthew J. Gadlage, Bharat L. Bhuva, Ronald D. Schrimpf, Lloyd W. Massengill, W. Timothy Holman, and Arthur F. Witulski

Vanderbilt University, Nashville, TN 37235, USA

A novel on-chip test circuit to measure single event transient (SET) pulse widths has been developed and implemented in IBM 130-nm and 90-nm processes for characterizing logic soft errors. Test measurements with energetic ions show transient widths ranging from 100 ps to over 1 ns, comparable to legitimate logic signals in such technologies. Certain layout techniques for logic circuits are shown to help limit the SET pulse width and hence mitigate soft errors.

11:50

6.4 – CMOS Latch Metastability Characterization at the 65-nm-Technology Node

Manjul Bhushan[1], Koushik K. Das[2] and Mark B. Ketchen[2]

[1]*IBM Systems and Technology Group, NY, USA,* [2]*IBM Research, T.J. Watson Research Center, NY, USA*

A new test structure for measuring CMOS latch metastability with sub-ps time resolution is described. The latch delay and error count in the metastability region are measured as a function of data-to-clock edge delay. This compact test structure can be placed in the scribe line for characterizing different latch designs and correlating their behavior to model predictions.

12:10–13:30 **Lunch**

13:30–13:40 **ICMTS 2009 Presentation**

SESSION 7: MOS Modeling and Characterisation

13:40–14:40

Co-Chairs: Kevin McCarthy, *University College Cork, Ireland*
Bill Verzi, *Agilent Technologies, USA*

13:40

7.1 – Characterization of MOSFETs Intrinsic Performance using the In-Wafer Advanced Kelvin-Contact Device Structure for High Performance CMOS LSIs

R. Kuroda[1,3], A. Teramoto[2], T. Komuro[4], W. Cheng[2], S. Watabe[1], C. Tye[1], S. Sugawa[1] and T. Ohmi[2]

[1]*Graduate School of Engineering, Tohoku University,* [2]*New Industry Creation Hatchery Center, Tohoku University,* [3]*Japan Society for the Promotion of Science Research Fellowship,* [4]*Agilent Technologies International Japan Ltd.*

The in-wafer Advanced Kelvin-Contact device structure is newly developed. The developed structure allows us to eliminate the series resistances in MOSFETs by the use of the current and potential lines physically implemented in the MOSFETs and we can characterize the MOSFETs intrinsic I-V characteristics as well as the quantitative effects of the series resistance to the device performance, very stably and accurately. It is very useful for the characterization and parameter extractions of fabricated MOSFETs for device/process development of ultra-thin gate insulator short channel CMOS LSIs for higher performance.

14:00

7.2 – New Y-function-based methodology for accurate extraction of electrical parameters on nano-scaled MOSFETs

Dominique Fleury[1,2], Antoine Cros[1], Hugues Brut[1], Gérard Ghibaudo[2],

[1]*STMicroelectronics, Crolles,* [2]*IMEP, Grenoble, France*

Accurate and reliable extraction of electrical parameters is becoming more and more difficult to perform on nanoscaled MOSFETs. Thus, we developed a new Y-function-based extraction methodology laying on a robust recursive algorithm. This new technique does not require any input parameter and vanishes any possible impact from the measurement noise, allowing to perform fast parameters extractions as needed by the industrial context. Automatic extractions have been performed, providing accurate and reliable results for standard and breakthrough architectures.

14:20

7.3 – A Novel Biasing Technique for Addressable Parametric Arrays

Brad Smith[1], Uma Annamalai[2], Alexandre Arriordaz[1], Venkat Kolagunta[1], Jeff Schmidt[1] and Mehul Shroff[1]

[1]*Freescale Semiconductor, Austin, TX,* [2]*University of Arkansas, AR, USA*

Addressable arrays are limited in size and utility by the parasitic leakage caused by the switches used to isolated the devices not being tested. A new biasing technique that removes the

drain-source bias from these switches has been studied to address this problem. Simulations performed in both 90 nm and 45 nm technologies predicted more than a two-decade drop in parasitic leakage of the array. Experiment data performed on a 90 nm technology confirmed this improvement.

14:40–15:10 **Break**

SESSION 8: RF

15:10–16:30

Co-Chairs: Franz Sischka, *Agilent Technologies, Germany*
Ulrich Schaper, *Infineon, Germany*

15:10

8.1 – 2.6GHz RF Inductive Power Delivery for Contactless On-Wafer Characterization

Jonathan Tompson, Adam Dolin, and Peter Kinget
Department of Electrical Engineering, Columbia University, NY, USA

This paper presents the critical components of a contactless IC testing infrastructure to overcome the shortfalls of more traditional IO approaches in nanoscale technologies. This includes the modeling, simulation and testing of an inductively-coupled, power injection system through 150×150μm on-chip and on-chip spiral inductors, low loss rectification and voltage regulation to supply a constant 1V, 8.5mW DC source to power on-chip characterization circuits. This system presents a means to power test circuitry without physical contact, with applications in process variation and fault analysis, in early stages of the fabrication cycle, after only completing a part of the back end interconnect steps, without damage to the wafers and without the need for ESD circuits.

15:30

8.2 – Advanced Test Structure Design for Dielectric Characterisation of Novel High-K Materials

John A. O'Sullivan, Kevin G. McCarthy and Gabriel M. Crean
Department of Electrical and Electronic Engineering, University College Cork, Ireland

The extremely high level of integration currently required within the wireless industry poses significant challenges at all technology steps from materials through processing to packaging. Capacitor design is a very important element of this technology integration challenge. Recently there has been strong interest in the use of PMNT (Pb(Mg,Nb)TiO^3) as a thin-film layer in semiconductor processes [1]. The high dielectric constant of PMNT makes it an attractive material for the fabrication of MIM (Metal/Insulator/Metal) decoupling capacitors. Before PMNT can be used in conjunction with a modern Si process for capacitor design the PMNT layer must be accurately characterised. This paper addresses the issue of thin-film characterisation through wafer-probe measurements and electromagnetic simulation (EM) of coplanar waveguides. Based on the results obtained a design methodology for optimum test structure layout is presented.

15:50

8.3 – Characterization of T-Shape Terminal Impedances of Differential Short Stubs in Advanced CMOS Technology

Chiaki Inui and Minoru Fujishima
University of Tokyo, Japan

For short stubs in advanced CMOS technology, it is known that small terminal impedances are achieved by employing differential transmission lines and by making virtual ground. However, no quantitative evaluation method of the terminal impedances of a differential short stub was reported. To characterize the terminal impedance accurately, we propose a T-shape terminal impedance model of differential short stubs, where the impedances are evaluated by applying differential-mode and common-mode signals. In this paper, we describe the T-shape terminal impedance model and the characterization procedure of the terminal impedances. From measured data, it is shown that the T-shape impedances in the differential short stubs are successfully evaluated.

16:10

8.4 – Identifying dielectric and resistive electrode losses in high-density capacitors at radio frequencies

M.P.J. Tiggelman[1], K. Reimann[2], M. Klee[3], R. Mauczock[3], W. Keur[3], J. Liu[2], Y. Furukawa[2], J. Schmitz[1] and R.J.E. Hueting[1]
[1]*MESA+ Research Institute for Nanotechnology, University of Twente,* [2]*NXP Semiconductors,* [3]*Philips Research, The Netherlands*

A regression-based technique is presented which distinguishes the intrinsic dielectric loss from the resistive loss of high density planar capacitors in a very wide bandwidth of 0.1 8GHz. Moreover, the procedure yields useful results if the capacitor deviates from a lumped element model and shows when the used approximations break down or whether size-dependent loss mechanisms exist.

16:30 **End of Session 8**

19:00 **Banquet in Playfair Library Hall, Old College**

Thursday 27th March

Location: Appleton Tower

08:30–17.00 Registration

SESSION 9: Interconnect

09:00–10:20

Co-Chairs: Hi-Deok Lee, *Chungnam National Univ., Korea*
Larg H. Weiland, *PDF Solutions, USA*

09:00

9.1 – A Study of Cross-Bridge Kelvin Resistor Structures for Reliable Measurement of Low Contact Resistances

N. Stavitski[1], J.H. Klootwijk[2], H.W. van Zeijl[3], A.Y. Kovalgin[1] and R.A.M. Wolters[1,4]

[1]*MESA+ Institute for Nanotechnology, University of Twente,* [2]*Philips Research,* [3]*DIMES, Delft University of Technology,* [4]*NXP Research, The Netherlands*

The parasitic factors that strongly affect the measurements accuracy of Cross-Bridge Kelvin Resistor (CBKR) structures for low specific contact resistances (ρ_c) have been extensively discussed during last few decades and the minimum of the ρ_c to be accurately extracted was estimated. We fabricated a set of various metal-to-metal CBKR structures with different geometries, i.e., shapes and dimensions, to confirm this limit experimentally. As a result, a model was developed to account for the actual current flow, to create a method for reliable ρ_c extraction. It was found that in our case of shallow metal-to-metal contacts, the measured CBKR contact resistance was determined by dimensions of the two-metal stack in the area of contact and sheet resistances of the metals used.

09:20

9.2 – Comb Capacitor Structures for Measurement of a Post-processed Layer

D. Roy[1], J.H. Klootwijk[2], N.A.M. Verhaegh[1], H.H.A.J. Roosen[2], and R.A.M. Wolters[1]

[1]*NXP Semiconductors,* [2]*Philips Research, The Netherlands*

Measurements of post-processed layers have been successfully done using simple comb capacitor structures. The structures were fabricated in a single step in the last metallization layer of a standard IC process. A coating is applied over different comb structures by spray coating. Changes in capacitance values of these comb structures are measured and analysed in terms of the properties of this coating layer.

09:40

9.3 – Test structure for characterizing metal thickness in damascene CMP technology

Alain Toffoli, Sylvain Maitrejean, Jean Duport de Pontcharra, Francois de Crecy, David Bouchu, Lucile Arnaud, Fabien Boulanger

CEA-LETI, Grenoble Cedex, France

The purpose of this work is to introduce a new test structure.

When it is coupled with TCR (Temperature Coefficient of Resistance) method, it is helpful for the electrical extraction, of the metal thickness unambiguously in Damascene interconnects process. In this case, others parameters as sheet resistance and resistivity, are also produced.

10:00

9.4 – Test Structure Definition for Dummy Metal Filling Strategy Dedicated to Advanced Integrated RF Inductors

C. Pastore[1,2], F. Gianesello[1], D. Gloria[1], E. Serret[1], P. Benech[2]

[1]*STMicroelectronics, Crolles,* [2]*IMEP, Grenoble Cedex, France*

A complete and relevant strategy to manage dummy fills inside a large spectrum of integrated RF inductors realized in a 0.13 5m CMOS technology using a Damascene Copper Back End is presented here. The main motivation of this paper relies on specific test structure definition and their RF characterization in order to evaluate the effect of metal dummy fills on the high frequency behaviour of integrated inductors used in main RF applications. Thanks to the developed test structures and Design Of Experiment modelling analysis, it has been possible to determine the right metal fill density to insert inside inductor without degrading its electrical performances. Thus, this work appears as a promising way to reduce the number of specific design rules applied to RF integrated inductors required to assure metal density uniformity and device performances. The proposed results would actually enable integrated RF inductors to be compliant with Advanced Digital Back End Of Line (BEOL) design rules.

10:20–10:50 **Break**

SESSION 10: Matching II – Mechanisms

10:50–12:10

Co-Chairs: Mark Poulter, *National Semiconductor, USA*
Hugues Brut, *STMicroelectronics, France*

10:50

10.1 – Fully considered layout variation analysis and compact modeling of MOSFETs and its application to circuit simulation

Takuji Tanaka[1], Akira Satoh[2], Mitsuru Yamaji[1], Osamu Yamasaki[1], Hiroshi Suzuki[2], Tsuyoshi Sakata[1], Yoshio Inoue[3], Masaru Ito[1], Seiichiro Yamaguchi[1] and Hiroshi Arimoto[1]

[1]*FUJITSU Ltd.,* [2]*FUJITSU Laboratories Ltd.,* [3]*FUJITSU VSLI Ltd. Tokyo, Japan,*

We have developed a total systems of circuit design to treat dependency of MOSFET electric characteristics of layout patterns. Our new methodology with two-step multivariate analysis realizes highly reliable compact modeling and its application to SPICE simulation significantly improves accuracy of circuit modeling. Our systems is a powerful tool of design for manufacturing in 65nm technology node and beyond.

11:10

10.2 – On-Mask Mismatch Resistor Structures for the Characterisation of Maskmaking Capability

S. Smith[1], A. Tsiamis[1], M. McCallum[2], A.C. Hourd[3], J.T.M. Stevenson[1], A.J. Walton[1] and S. Enderling[1]

[1] *The University of Edinburgh,* [2] *Nikon Precision Europe GmbH,* [3] *Compugraphics International Ltd., UK*

This paper presents results of the use of electrical measurements to investigate dimensional mismatch in an advanced photomask process. Test structures consisting of matched pairs of Kelvin resistor structures have been measured and the results analysed to obtain information about the capability of the mask making process. Comparisons between this mask and a previous plate have shown a significant change, which is consistent with the recalibration of the mask writing tool's correction parameters.

11:30

10.3 – Physics and Modeling of Transistor Matching Degradation under Matched External Stress

Xiaoju Wu, Zhenwu Chen

Mixed Signal Technology Development, Texas Instruments, TX, USA

In this paper, we report detailed studies on transistor matching reliability under external stresses such as NBTI. Transistor threshold voltage VT mismatching as a function of stress voltage, ambient temperature as well as stress time has been established based on device physics and statistics. A closed form equation for current mismatching under stress has also been obtained using a correlated mobility-shift and VT-shift model. Methods to extract relevant parameters in the models have been established. The models have been validated experimentally and been used to predict the transistor matching shift under normal operating conditions for a 40V high performance precision analog technology. It has been found that transistor matching degrades 10% during the 10 years lifetime of products when operating at VGS=15V and 100C. This suggests 10% over design for critical transistor matched transistors at time zero in order to achieve a 10 year reliability requirement.

11:50

10.4 – Influence of STI stress on drain current matching in advanced CMOS

Nicole Wils[1], Hans Tuinhout[1], Maurice Meijer[2]

[1] *NXP-TSMC Research Center,* [2] *NXP Semiconductor Research, The Netherlands*

Using a dedicated set of asymmetrically designed matched pair test structures and a novel data analysis technique based on so-called mismatch sweeps, we answer some important questions in the discussions on variability in advanced CMOS technologies.

12:10 **Best paper announcement and closing remarks**

12:30 **Lunch**

13:30 **Excursion**

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ICMTS 2008 CONDENSED PROGRAM

Monday, March 24

08:00	Registration
09:00	Introduction
09:05	Test Structure Fundamentals
09:55	MEMS Test Structures
10:45	Break
11:15	SPICE Modeling
12:05	Characterization of Mobility
12:55	Lunch
14:25	Pulsed IV Characterisation
15:15	Through Wafer Vias
16:05	Break
16:35	Efficient Usage of Test Structures
17:25	Dielectric Characterisation
18:15	Closing Remarks
18:30	Welcome Reception

Tuesday, March 25

08:00	Registration
09:00	Opening Remarks
09:10	Session 1 Matching I
10:30	Break
11:00	Session 2 Resistivity
12:00	Lunch
13:30	Session 3 Yield I
14:50	Break
15:20	Session 4 Poster Talks
16:00	Exhibitor Presentions
16:30	Poster Session
18:00	End of Poster Session

Wednesday, March 26

08:30	Registration
09:00	Session 5 3D Integration
10:20	Break
10:50	Session 6 Yield II
12:10	Lunch
13:30	ICMTS 2009
13:40	Session 7 MOS Modeling
14:40	Break
15:10	Session 8 RF
16:30	End of Session 8
19:00	Banquet

Thursday, March 27

08:30	Registration
09:00	Session 9 Interconnect
10:20	Break
10:50	Session 10 Matching II
12:10	Closing remarks
12:30	Lunch
13:30	Excursion