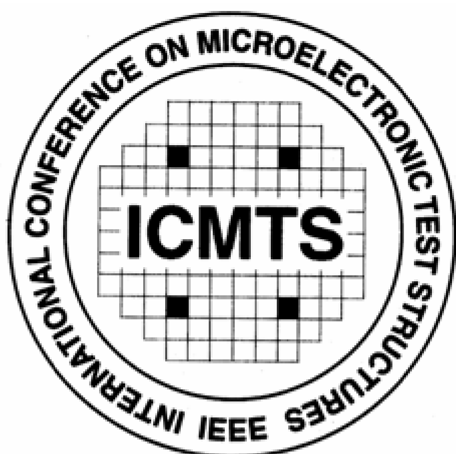
20th ICMTS

2007 IEEE
International Conference on
Microelectronic Test Structures



March 19-22
Takeda Hall,
The University of Tokyo
Tokyo, Japan

http://www.else.k.u-tokyo.ac.jp/ICMTS07/
icmts2007@vdec.u-tokyo.ac.jp

Sponsored by:
Association for Promotion of Electrical,
Electronic and Information Engineering
The IEEE Electron Devices Society

In cooperation with:
The Institute of Electronics, Information and
Communication Engineers
The Japan Society of Applied Physics
VLSI Design and Education Center

20th ICMTS
2007 IEEE International Conference on
Microelectronic Test Structures

Tutorial and Technical
Program

2007 March 19-22
Takeda Hall, the University of Tokyo
2-11-16, Yayoi, Bunkyo-ku, Tokyo 113-0032
Japan

http://www.else.k.u-tokyo.ac.jp/ICMTS07/
http://www.see.ed.ac.uk/ICMTS/

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ICMTS 2007 CHAIRMAN'S LETTER

Dear Colleagues,

On behalf of the committee, I welcome you to the 2007 International Conference on Microelectronic Test Structures (ICMTS 2007) in Tokyo, Japan. This is the 20th anniversary of the ICMTS and the 6th conference to be held in Japan. The conference is technically sponsored by the IEEE Electron Devices Society and sponsored by the Association for Promotion of Electrical, Electronic and Information Engineering in cooperation with the Institute of Electronics, Information and Communication Engineers, the Japan Society of Applied Physics, and the VLSI Design and Education Center, the University of Tokyo.

The ICMTS has been advanced with the progress of the semiconductor integrated circuits. Test structure is the key for research and development of new integrated circuits. Those for new process, device and circuit developments become more important as the feature size is scaled down into sub-100 nanometer. Furthermore, they can provide the rapid technology transfer and quick yield improvements of new LSIs. Topics of the ICMTS have been increasing steadily, from the fundamental fields to the new fields: Low-k and high-k materials for high-performance LSIs, MEMS devices for sensors and RF ICs, etc.

The purpose of the conference is to bring together designers and users of test structures to discuss recent developments and future directions. This year's conference consists of 54 papers in 9 oral sessions and 1 poster session. Session topics will include: “CD Metrology”, “Process Characterization”, “Device Characterization”, “Matching”, “Capacitance”, “Yield and Variation”, “RF”, and “Parameter Extraction and Modeling”. Oral presentations are 15 minutes long with 5 minutes for questions. The poster session is preceded by a three-minute oral presentation by the author.

The one-day Tutorial Short Course will be held on March 19. The course is intended to provide the participants with guidelines and information that will be helpful for good design, test and analysis. The instructors have many years of experience in their fields. The Tutorial will cover Test Structure Fundamentals, Efficient Usage of Test Structures, Strained-Si CMOS, MEMS Reliability, Low-k1 Lithography, BEOL design, RF Measurement, and SPICE Modeling.

There will be an equipment exhibition relating to the latest test structure measurements: measurement instruments, wafer probing equipment, computer software for data analysis, parameter extraction and measurement control.

The 2007 ICMTS will be held in the University of Tokyo, and this is the first time the conference is being held at a university campus in Japan. The University of Tokyo was founded in 1877 and celebrating its' 130th anniversary in 2007. The location of the conference was formerly the mansion of an old ‘samurai’ leader. There are many historical buildings on campus: the “*Akamon*”, the red gate, which was built about 300 years ago, is an important cultural property in Japan; Yasuda hall and the general library were built about 100 years ago; and there is also a natural garden with Sanshiro-ike pond. The ICMTS will be held in the Takeda hall. In the Takeda building, which was built three years ago, we have a federal class 1 super clean room with good equipments for making fine Si test devices. The VLSI design and education center (namely VDEC) is working here, and fabrication of various devices including MEMS and material research are being performed actively.

Just near the university, there is Ueno Park, a large cultural park with various museums and zoo. Also nearby is the famous electric town, Akihabara, with many electronic parts shops and big discount stores offering all sorts of consumer electronic products. The official conference hotel, Juraku at Ochanomizu, is located between Akihabara and the University.

For further information, please visit the ICMTS web site at
http://www.see.ed.ac.uk/ICMTS/ or
http://www.else.k.u-tokyo.ac.jp/ICMTS07/.
We are looking forward to seeing you in Tokyo.

Sincerely,

Yoichi Tamaki
General Chairman

GENERAL INFORMATION

Conference Information

The 2007 International Conference on Microelectronic Test Structures is technically sponsored by the IEEE Electron Devices Society and sponsored by the Association for Promotion of Electrical, Electronic and Information Engineering in cooperation with the Institute of Electronics, Information and Communication Engineers (IEICE), the Japan Society of Applied Physics (JSAP), and the VLSI Design and Education Center, the University of Tokyo (VDEC). The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The Conference will be preceded by a one-day Tutorial Short Course covering a variety of technical areas related to Microelectronic Test Structures.

ICMTS 2007 homepage :
http://www.else.k.u-tokyo.ac.jp/ICMTS07/

ICMTS homepage :
http//:www.see.ed.ac.uk/ICMTS/

Presentation

The official language of the conference is English.

The ICMTS considers both oral and poster presentations to be of equal value and importance to the Conference. Oral presentation time is 15 minutes plus 5 minutes for discussion. All poster presenters are requested to make a brief, three-minute oral presentation describing their research to the Conference during a session prior to the poster session. This presentation is limited to three slides. For presentation, Windows laptop PC installed with Microsoft Powerpoint 2003 and Adobe Acrobat 7 will be available in the conference hall. It is highly recommended to use this PC so as to remove time loss in PC switching. Before March 12, send all presentation materials to icmts2007@vdec.u-tokyo.ac.jp. Also remember to bring original files as backup. There will be no slide projector available. All speakers are requested to report to registration desk located in front of the conference room before the session begins. Poster board for A0 size will be available for poster session.

Best Paper Award

Both Oral and Poster papers will be judged by the same criteria in determining the best paper award for the Conference. The best paper will be announced at the end of the conference. Presentation of the award will be made at the ICMTS 2008.

Conference Proceedings

The IEEE ICMTS 2007 will publish proceedings and CD-ROM. One copy of the proceedings and one CD-ROM are included in the registration fee. Additional copies will be available at the Conference for 5,000 yen per copy for members of the IEEE or IEICE or JSAP, 7,000 yen per copy for non-members, or from the IEEE after the conference.

Equipment Exhibition

An equipment exhibition will be held besides the conference room during the Conference to display equipment closely paralleling the nature of this meeting. This equipment exhibition will permit one-on-one discussions between exhibitors and conference attendees on the latest test equipment. Exhibits will be open as follows.

March 19	13:00 – 17:00
March 20, 21	9:00 – 17:00
March 22	9:00 – 12:00

The exhibitors list will be distributed on the day of the conference.

On-Line Conference Registration

JTB Global Marketing & Travel Inc. (JTB GMT) has been appointed as the official registration office for the conference and will handle registration. Please visit the ICMTS website (http://www.else.k.u-tokyo.ac.jp/ICMTS07/) to make on-site registration.

Conference registration fees

Below are the conference fees for early, late, and on-site registrants.

Early Registration: (Registered by January 31, 2007)

	Member*	Non Member	Student**
Tutorial	￥18,000	￥21,000	￥ 8,000
Technical Sessions	￥35,000	￥43,000	￥25,000

Late Registration: (Registered after February 1, 2007)

	Member*	Non Member	Student**
Tutorial	￥25,000	￥28,000	￥10,000
Technical Sessions	￥38,000	￥46,000	￥26,000

On-site Registration: (Registration at the Conference)

	Member*	Non Member	Student**
Tutorial	￥31,000	￥34,000	￥13,000
Technical Sessions	￥40,000	￥48,000	￥28,000

* Must be a member of the IEEE or IEICE or JSAP.

**To qualify for reduced conference rates, you must be a Student Member, a full time student, not be self-employed, nor working part or full time at a facility or corporation.

Registration fees include admittance to technical sessions, equipment exhibits, morning and afternoon coffee breaks, reception, conference banquet, one copy of the proceedings and CD-ROM.

On-site registration schedule

On-site registration for the conference will be conducted at the Registration Counter (5th floor) at Takeda Hall of the University of Tokyo as follows:

Monday,	March 19	8:00 – 19:00
Tuesday,	March 20	8:00 – 17:00
Wednesday,	March 21	8:30 – 16:00
Thursday,	March 22	8:30 – 11:00

Payment of the registration fees

Registration fees should be payable to the IEEE ICMTS 2007 and must be in Japanese Yen only.

(1) A bank transfer to JTB Global Marketing & Travel Inc.
(Message: CD101923-718)
Account at The Bank of Tokyo-Mitsubishi UFJ, Ltd.
Shin-Marunouchi Branch (swift code: BOTKJPJT)
1-4-2 Marunouchi, Chiyoda-ku, Tokyo 100-0005 Japan
Account number: 4760343

(2) Bank Check in Yen payable to the order of IEEE ICMTS 2007. Personal Checks are not acceptable.

(3) Credit Card in Yen: Master Card, VISA, Diners Club, American Express are available.

(4) Cash in Yen at the conference registration desk.

Cancellation

Due to advance financial commitments, refunds of registration fees requested after March 1, 2007, cannot be guaranteed. 5,000 yen processing fee will be withheld from all refunds. Requests for refunds of registrations cancelled after March 1 will be considered after the conference.

On or before February 28, 2007 ---------JPY5,000 of processing fee
On and after March 1, 2007 -------------100% of the registration fee

Messages

If you need to be contacted during the Conference Sessions, a message can be left at the Registration Counter (5th floor) at Takeda Hall of the University of Tokyo between the hours of 9:00am and 5:00pm, March 19, 20, 21, and from 9:00 to 12:00pm on March 22. Messages will be placed on a Message Board beside the registration desk.

Banquet

The conference banquet will be held on Wednesday evening, March 21 at Tokyo's Japanese Garden Restaurant (Chinzan-so). Bus will depart at 18:30 from Takeda Building. Conference registration fees include one banquet ticket. Guest ticket will be available for sale at the registration desk.

During the banquet, a “*koto* (Japanese harp)” concert is programmed. The players are licensed specialists conducted by

Ms. Miho Todoroki. Ms. Todoroki got her bachelor and master's degrees from Traditional Japanese Music Course of the Tokyo National University of Fine Arts and Music, and she is a *dai-shihan*, a superior master, of *Nippon Todokai* school.

Tea-ceremony

During the conference break, a Japanese traditional tea-ceremony is planned. Details will be available at registration desk.

Excursion – *Tokyo Afternoon*

We have arranged Excursion on Wednesday, March 22.
Visit Asakusa, Nakamise and the Imperial Palace (Tokyo afternoon tour), where allows you to enjoy cruising on Sumidagawa river, shopping at Nakamise and sight of the castle of Edo and the Imperial Palace at evening.

Time: 13:00 – 17:20
Fare: 6,000 yen/person (Admission tickets and Lunch box are included)

Tokyo Information

Tokyo is a capital city of Japan for 400 years since the Tokugawa shogunate installed his headquarters in 1603. The characteristic of Tokyo is the co-existence of history such as *Sensoji* Temple (*Asakusa area*) and *Ueno* Park, daily life such as small villages of two-level houses in wood, and modern life such as Akihabara Electric Market Town, Roppongi Hills Skyscraper, and Tokyo Disneyland.

Climate and Clothing

The temperature in Tokyo during the conference period will range between 8ºC (46ºF) at night and 16ºC (64ºF) during the day. The weather is, however, often unpredictable during this season. The average humidity is 76%, so light clothing and a sweater or light coat is recommended. Takeda Hall is fully air-conditioned.

Hotel Accommodations

JTB Global Marketing & Travel Inc. (JTB GMT) will handle registration all related travel arrangements including hotel accommodation. Fill in the on-line application form linked from the ICMTS website (http://www.else.k.u-tokyo.ac.jp/ICMTS07/). Inquiries and applications concerning arrangements should be addressed to:

JTB Global Marketing & Travel Inc.
Convention Center (CD101923-718)
Fax+81-3-5495-0685
2-3-11 Higashi-Shinagawa, Shinagawa-ku,
Tokyo 140-8604 Japan
Phone+81-3-5796-5445
E-mail: icmts2007@jtb.jp

ICMTS has reserved a sufficient number of rooms at the following hotels for Conference participants at special discount rates. Those persons who wish to apply for hotel reservation are requested to apply online to reach JTB GMT no later than February 16th. Please note that **room availability is guaranteed until February 16th**. For reservation later than February 16th, rooms may still be available but not for sure. If hotel is already fully occupied, we will reserve for you another hotel instead, with possibly more elevated rate. It is therefore highly recommended to make your reservation **as soon as possible**

Daily room charges are as follows:

Name of Hotel	Rate	
	Single	Double
Ochanomizu Hotel Juraku	¥7,500	¥13,000 (for 2 persons)

Hotel Location

2-9 Kanda-Awajicho, Chiyoda-ku, Tokyo
+81-3-3251-7222
5 min. walk to JR Akihabara or Ochanomizu Stations.
15min. to conference site with using metro for 2 stations.

1) Above rate includes service charge, tax and full buffet-style breakfast.
2) It should be noted that it is practically impossible to find elsewhere such a nice accommodation in such an inexpensive rate.

Hotel Cancellation:

If a cancellation notice is received by JTB GMT on or before or after

One day before the day ----------------------20% of the charge
On the day -------------------------------------80% of the charge
On day after the day --------------------------100% of the charge

Transportation

Detailed access instruction is available at the ICMTS 2007 official WEB page.

Nearest Airport is Narita Tokyo International Airport (NRT). From Narita, you can conveniently use railway services into downtown of Tokyo. Two major carriers run trains from Narita: Keisei railway and Japan Railway (JR). For those who are interested in visiting other historical cities such as *Kyoto* and *Nara*, it is recommended to purchase *before* leaving your country the "JR Rail Pass", with which you can take unlimited number of JR trains including "Hikari" bullet trains.

Once you are in the downtown, the most convenient way to access Takeda Hall is to take a metro Chiyoda-line and get out at "Nezu (C-14)" station. Nezu is two stations from "Shin-Ochanomizu (C-12)", which is the nearest station of Hotel Juraku. From Exit #1, turn right and across the street, then again turn right and climb up the hill. In 600 meters, at the next traffic signal, you will see Takeda Building on your left.

TUTORIAL SHORT COURSE

Monday, March 19

8:00 – 17:00 Registration
9:00 Introduction – Kiyoshi Takeuchi, *NEC Corp.*

9:05
1. Test Structure Fundamentals – Anthony J. Walton, *The University of Edinburgh*

This presentation will begin with a review of test structures detailing their history and hot topics over the past 20 years. The presentation will include the development of test structures for measuring sheet resistance, line width and contact resistance. Measurement and equipment developments will also be addressed focusing on procedures for obtaining accurate and repeatable measurements.

9:55
2. Efficient Usage of Test Structures – Christopher Hess, *PDF Solutions*

Test Structures are used for an ever increasing set of applications. Thus, more and more test structures have to be designed, manufactured, tested and analyzed. Focusing on Yield and Variability, the Tutorial will give an overview how to balance and manage the following challenges:
- Increase the Number of Experiments
- Decrease Mask Cost
- Decrease Test Time
- Faster Data Feedback

10:45 Break

11:00
3. Physics and Technology of Strained-Si CMOS – Shinichi Takagi, *The University of Tokyo*

A strained-Si channel has been recognized as mandatory for sub-100 nm CMOS devices. This talk will review the current status of strained-Si CMOS including both global and local techniques with an emphasis on the underlying device physics. The physical mechanisms of the mobility enhancements due to uni-axial and bi-axial strain will be explained from the viewpoint of the MOS subband structures. Also, a variety of global strain substrates and local strain techniques and the combined technologies will be introduced with comparing the pros and cons.

11:50

4. MEMS Reliability – Toshiyuki Tsuchiya, *Kyoto University*

Reliability of microelectromechanical systems (MEMS) is one of the most important issues when devices come into market. Much research on MEMS reliability has been done both in research institutes and product developers. However, there are few standard test methods and little common knowledge in MEMS reliability, which prevents rapid product development and causes higher development cost. In this tutorial, test methods and current knowledge in MEMS reliability are presented, especially about silicon material and device, which is most widely investigated but still being discussed today.

12:40 Lunch

13:40

5. Approaches to Ultra low-k1 Lithography – Kohji Hashimoto, *Toshiba Corporation*

The accelerating shift toward much smaller geometries in semiconductor devices poses difficulties concerning lithography for mass production. In regard to optical lithography, the manufacturability is roughly defined by the k1 factor from the Rayleigh equation (k1=Half pitch*NA/λ). Below 45nm CMOS technology node, even using a high-end optical exposure system such as immersion lithography with higher NA, k1 factor is lower than 0.35. The primary risk posed by lower k1 is the likelihood of degradation of patterning fidelity on LSI circuits. This tutorial describes our approaches to ultra low-k1 lithography on high-end semiconductor devices with brief summaries on state-of-art lithography status.

14:30

6. Global Interconnect Characterization, Testchip, Structures, Modeling, and Statistics for BEOL – Akis Doganis, *TSMC*

The tutorial will cover all aspects from design of a specialized set of BEOL test structures, to the generation of RC statistical worst-case models for circuit simulation, and intelligent dummy metal insertion methodology to minimize the circuit delay variations. The discussion will touch as well, some advanced nonlinear optimization techniques using PCA, and RSM which are used for a 3D solver calibration, statistical intra-, inter-die modeling, with dependencies on metal density, dummy metal insertion, and conductor orientation. Briefly, the SPICE RC model verification and validation will be given. Additionally, an overview of the circuit design flow and the necessity of the BEOL parasitic RC models for timing accuracy will be preceded.

15:20 Break

15:50
7. On-wafer evaluation for high-frequency CMOS devices – Minoru Fujishima, *The University of Tokyo*

In this presentation, on-wafer evaluation for CMOS devices with high-frequency operation will be reviewed. The presentation will include brief introduction of high-frequency measurement procedures and parameter extraction for CMOS active and passive devices. Also issues on measurement accuracy and reproducibility in ultra-high frequency, such as millimeter-wave band will be addressed.

16:40
8. SPICE Modeling – Colin McAndrew, *Freescale Semiconductor*

This tutorial will review topics in compact modeling ("SPICE" modeling) for circuit simulation. Recently, there has been a fundamental shift in MOSFET models, from being based on threshold voltage to being based on the surface potential formulation. This is a very major change, and was not undertaken lightly but was forced by weaknesses and inabilities of threshold voltage based MOSFET models to simulate some key circuit performance measures, especially for RF CMOS. Details of these issues, which were the primary motivation behind the selection, by the Compact Model Council, of PSP as the new standard MOSFET model, will be reviewed. The fundamental physical operation of MOSFETs will be detailed, and this will be translated into the basic equations and structure of surface potential based models in general, and PSP in particular. The geometric dependence of parameters, and the separation into local and global parameters, will be covered; this has caused some confusion among characterization engineers but is in essence no different from what has been the standard practice for some time.

17:30 Wrap-Up and Conclusion

18:00 Welcome Reception at Foyer

ICMTS 2007 Tutorial Lecturer Biography

Anthony J. Walton

Anthony J. Walton is professor of Microelectronic Manufacturing in the School of Engineering and Electronics at the University of Edinburgh. He has been actively involved with the semiconductor industry in a number of areas associated with silicon IC technology and micro-systems. Over the past 25 years he has had a direct interest in the design, fabrication and measurement of microelectronic test structures and has taken an active role in the organization of ICMTS. He played a key role in setting up the Scottish Microelectronics Centre (SMC) which is a purpose built facility for R&D and company incubation consisting of approximately 300 m^2 of class 10 cleanrooms. Companies that have successfully incubated in the Centre include MED, Memsstar and Oligon. He has published widely on test structures and is an associate editor of the IEEE Transactions on Semiconductor Manufacturing.

Christopher Hess

Christopher Hess received the diploma degree in electrical engineering from the University of Karlsruhe, Germany in 1992, and the Dr.-Ing. (Ph.D.) degree in computer science from the University of Karlsruhe, Germany in 1998. In 1992 he was a founding member of the Defect Diagnosis Group at the University of Karlsruhe. In 1998 he joined PDF Solutions in San Jose, CA. As a Fellow he is currently responsible for Yield & Performance Characterization. Since 1992, he has been involved in the design of more than 100 test chips for the microelectronics industry over numerous technologies. For years, his main R&D focus is on efficient merging of experiments by minimizing chip area usage and manufacturing cycle time. His activities also include developing new architectures of testing equipment providing several orders of magnitude more data from high density test chips compared to testing traditional stand alone experiments. Most recently he is working on high density test chips for scribe line applications. Dr. Hess has published about 40 conference and journal papers and he holds 10 patents. He is a member of the IEEE and the Electron Device Society as well as a technical committee member of several semiconductor manufacturing related conferences. He has served as Technical Chairman of the 2000 International Conference on Microelectronic Test Structures (ICMTS) and General Chairman of ICMTS in 2003.

Shinichi Takagi

Shinichi Takagi received the B.S., M.S. and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1982, 1984 and 1987, respectively. He joined the Toshiba Research and Development Center, Kawasaki, Japan, in 1987, where he had been engaged in the research on the device physics of Si MOSFETs. From 1993 to 1995, he was a Visiting Scholar at Stanford University, where he studied the Si/SiGe hetero-structure devices. Since 2001, he has been working for MIRAI Project, as the leader of New Transistor Structures and Measurement/Analysis Technology Group. In 2003, he moved to the University of Tokyo, where he is currently working as a professor in the department of Frontier Informatics, Graduate School of Frontier Science.

Toshiyuki Tsuchiya

Toshiyuki Tsuchiya received the M.S. degree from the University of Tokyo and the Ph.D. degree from Nagoya University in 1993 and 2004, respectively. He worked with Toyota Central Research and Development Laboratories form 1993 to 2004. In 2004, he joined Kyoto University as an associate professor and now he is in the Department of Micro Engineering. He is currently engaged in the research of silicon surface micromachining, its sensor application, and mechanical property evaluation of MEMS materials.

Kohji Hashimoto

Kohji Hashimoto received M.S. degree in electric engineering from the Kyusyu University, Fukuoka, Japan in 1988. After joining the Toshiba ULSI Research Center, Toshiba Corporation, Kawasaki, Japan in 1988, he worked for the development of megabit DRAM device technology. From 1991 to 1993, he worked for phase shift mask development for sub-half micron lithography. From 1993 to 1996, he joined to the quarter micron DRAM development project with IBM and Siemens at IBM East Fishkill, NY, USA, and worked for lithography integration there. From 1996 to now, he has been engaged in the development of lithography technology to apply Flash, DRAM, High-end CMOS, SRAM and CMOS sensor at Process and Manufacturing Engineering Center, Toshiba Corporation, Yokohama, Japan. He is member of the SPIE and the Japan Society of Applied Physics (JSAP).

Akis Doganis

Akis Doganis, Technical Director in TSMC, Taiwan. He holds a Stanford Univ. Dgr. in E.E. and M.Sc. in Systems Control and he is the author of "OPSIM™" circuit optimizer, "SUXES™" and "SUP-OPT™" device and process modeling and optimization programs, which distributed worldwide by Stanford University. As VP of R&D of Meta-Software Inc. he setup the Meta-Labs for device parameter extraction, circuit optimization and testchip design. He founded and co-founded 3 EDA companies, and he served as President, CTO, VP of R&D, or Chief Scientist, and has developed many EDA packages. His current interests include, BEOL testchip design, interconnect RC characterization and modeling, Statistical Worst-case corners, advanced eDFM, and maximization of eDFY.

Minoru Fujishima

Minoru Fujishima received BE, ME, and PhD degrees from the University of Tokyo in 1998, 1990, and 1993, respectively. In 1993, he joined the University of Tokyo as a research associate and is currently an associate professor. His research interests are design and modeling of high-frequency CMOS, in particular millimeter-wave CMOS. He has served on a TPC member of Symposium on VLSI Circuits and Solid-State Devices and Materials (SSDM). He is currently a TPC member of A-SSCC and an editor of Japanese Journal of Applied Physics (JJAP).

Colin McAndrew

Colin McAndrew received the Ph.D. and M.A.Sc. in Systems Design Engineering from the University of Waterloo, Ontario, Canada, and the B.E. (Hons) from Monash University, Melbourne, Australia. He was with AT&T Bell Laboratories for 7 years, ending up as a Distinguished Member of Technical Staff, and since 1995 has been with Freescale Semiconductor (formerly Motorola) in Tempe AZ. He is a Fellow of the IEEE, the Vice-Chairman of the Compact Model Council, an editor of the IEEE Transactions on Electron Devices, and is or has been on the technical program committees for the IEEE BCTM, ICMTS, CICC, and BMAS conferences.

TECHNICAL PROGRAM SCHEDULE

Tuesday, March 20

8:00 – 17:00 Registration

9:00 Opening Remarks

Yoichi Tamaki, General Chairman

Yoshio Mita, Technical Program Chairman

SESSION 1: CD Metrology

9:10 – 10:30

Co-Chairs: Michael W. Cresswell, *NIST, USA*

Loren W. Linholm, *USA*

9:10 1.1 Electrical Measurement of On-Mask Mismatch Resistor Structures,

S. Smith[1], A. Tsiamis[1], M. McCallum[2], A.C. Hourd[3], J.T.M. Stevenson[1], and A.J. Walton[1],

[1]The University of Edinburgh, [2]Nikon Precision Europe, [3]Compugraphics International Ltd., UK

This paper describes the design and measurement of electrically measured test structures for the characterisation of dimensional mismatch in an advanced photomask making process. Test structures consisting of pairs of Kelvin connected bridge resistors have been fabricated on a chrome-on-quartz photomask plate. These have been electrically measured on mask and the results used to obtain information about dimensional mismatch in the mask making process.

9:30 1.2 A Systematic Approach to Accurate Evaluation of CD-Metrology Tools,

N. G. Orji, B. D. Bunday, R. G. Dixson, and J.A. Allgair,

National Institute of Standards and Technology, USA

We present a procedure for evaluating the accuracy and performance of critical dimension metrology tools used in monitoring the semiconductor manufacturing process. Our method involves the use of a reference measurement instrument and SI traceable reference material to evaluate the accuracy and resolution CD metrology tools. The achievable accuracy and intrinsic linearity of the tools under test are evaluated with respect to the reference system.

9:50 1.3 Extraction of Sheet Resistance and Linewidth from All Copper ECD Structures Fabricated from Silicon Preforms,

B.J.R. Shulver[1], A.S. Bunting[1], L.I. Haworth[1], A.M.

Gundlach[1], A.W.S. Ross[1], S. Smith[1], A.J. Snell[1], J.T.M. Stevenson[1], A.J. Walton[1], R.A. Allen[2], and M.W. Cresswell[2],
[1]*University of Edinburgh, UK,*
[2]*National Institute of Standards and Technology, USA*

Structures have been fabricated to allow electrical Critical Dimensions (ECD) to be extracted from copper interconnect features. The implementation of these structures is such that no conductive barrier metal has been used. This permits electrical measurements to be taken from copper test structures without interference from other materials. The advantage of this approach is that the electrical measurements provide a non-destructive and efficient method for determining CD values. This paper reports on the results of various tests which have been conducted to fully evaluate the current design.

10:10 1.4 Study of Test Structures for Application as Reference Material for Optical Critical Dimension Application,

Richard A. Allen[1], Heather J. Patrick[1], Michael Bishop[3], Thomas A. Germer[2], and Michael W. Cresswell[1],
[1]*National Institute of Standards and Technology, USA,*
[2]*KT Consulting, Inc., USA,*
[3]*International SEMATECH Manufacturing Initiative, USA*

Optical Critical Dimension (OCD) metrology has rapidly become a critical tool of the worldwide semiconductor industry. OCD relies on a combination of measurement and modeling to extract the average dimensions of an array of identical features, typically parallel line. In this paper, initial work into the development of reference materials at NIST is reported. These reference materials include features with vertical sidewalls defined by the silicon lattice.

10:30 – 10:40 Exhibition Presentations
10:40 – 11:00 Break

SESSION 2: Process Characterization

11:00 – 12:20

Co-Chairs: Junko Komori, *Renesas Technology, Japan*
Emilio Lora-Tamayo,
Universitat Autonoma de Barcelona, Spain

11:00 2.1 A New Test Structure for Shallow Trench Isolation (STI) Depth Monitor,

Qingfeng Wang, Sameer Pendharkar, Binghua Hu, Bill Russell, and Pam Jones-Williams, *Texas Instruments, USA*

A non-destructive electrical process monitor has been developed for shallow trench isolation (STI) depth control

in an advanced high voltage analog process. An implanted p-body (LDMOS back gate) pinch resistor has been demonstrated to accurately measure the depth of the shallow trench isolation. STI depth can be further correlated to critical LDMOS parameters such as Rdson (on resistance) and BVdss (off-state device breakdown). This technique can be easily implemented in the scribe line to monitor STI trench depth as well as to characterize high voltage component variations.

11:20 FUSI Specific Yield Monitoring Enabling Improved
2.2 Circuit Performance and Fast Feedback to Production,

T. Chiarella[1], M. Rosmeulen[1], H. Tigelaar[2], C. Kerner[1], A. Nackaerts[1], J. Ramos[1], A. Lauwers[1], A. Veloso[1], M. Jurczak[1], A. Rothschild[1], L. Witters[1], H. Yu[1], J. A. Kittl [2], R. Verbeeck[1], M. de Potter[1], I. Debusschere[1], P. Absil[1], S. Biesemans[1], and T. Hoffmann[1],
[1]IMEC, [2]Texas Instruments, Belgium

The integration of fully silicided gates on a high-k dielectric in a standard process flow offers a solid alternative to the conventional Poly/SiON devices. In this work, we provide an extensive analysis of the module yield extracted for such devices highlighting the need for specific additional alarm flags without which some integration problems might be overlooked. The impact at the circuit level is studied and supported by modeling work on simple ring-oscillators.

11:40 Test Circuit for Study of CMOS Process Variation by
2.3 Measurement of Analog Characteristics,

Karen M. González-Valentín Gettings, and Duane S. Boning,
Massachusetts Institute of Technology, USA

This paper presents a test chip for extraction of spatial and layout dependent variations in both transistor and interconnect structures. A scan chain approach is combined with low-leakage and low-variation switches, providing access to detailed analog characteristics in large arrays of test devices. Compared to digital (ring oscillator) test structures, the test circuit enables flexible extraction and analysis of variation in any device model parameters based on current/voltage measurement.

12:00 Ring Oscillator Based Test Structure for NBTI
2.4 Analysis,

Mark B. Ketchen, Manjul Bhushan, and Ronald Bolam,
IBM Corp., USA

We have developed a new NBTI test structure comprising differential pairs of ring oscillators with stages

of various circuit types. For stages consisting of inverters driving p-FET passgates, the gates of which are set at an adjustable potential, this structure allows high resolution absolute measurement of the average Vt shift of a large number (~ 100) product representative p-FETs in response to a pure AC or DC NBTI voltage stress as short as 30 sec as well as traditional long duration pure NBTI AC or DC voltage/temperature stresses.

12:20 – 13:50 Lunch

SESSION 3: Device Characterization I

13:50 - 15:10

Co-Chairs: Kiyoshi Takeuchi, *NEC, Japan*
Greg Yeric, *Synopsys, USA*

13:50 3.1 A Precise Resistance Tracing Technique for a Toggle Mode MRAM Evaluation,

Y. Katoh, K. Tsuji, H. Hada, and N. Kasai, *NEC, Japan*

A precise evaluation technique was created for developing magnetic random access memory (MRAM), especially such memory that is operated in a toggle writing mode. This technique allows us to observe a detailed resistance transition of a magnetic tunneling junction (MTJ) cell during a complicated write operation. It was used to analyze failed cells, and it revealed that the MTJ characteristics in the third quadrant are significantly related to the disturb robustness with 4 Mbit MRAM. We found our technique to be a powerful method for failure analysis and essential for accelerating MRAM development.

14:10 3.2 Electrical Failure Analysis Methodology for DRAM of 80nm era and beyond using Nanoprober Technique,

Hyunho Park, Sang-Yeon Han, Won-Seok Lee, Satoru Yamada, Chang-Hoon Jeon, Siok Sohn, Kyosuk Chae, Wouns Yang, and Donggun Park,
Samsung Electronics Co., Korea

In this paper, the electrical failure analysis for DRAM of design rule as 80nm and beyond by using nanoprober technique was described. We have successfully measured and evaluated electrical characteristics of periphery and cell array transistors of 80nm DRAM using nanoprober. Measurements for Metal Contact (MC), Bit Line (BL) and Bit Line Contact (BLC) probing were proceeded and compared with Test Element Group (TEG) probing results. Interconnect Characterization Environment (ICE) simulation was also carried out to verify the current decrease of BLC probing results. Measurement for characteristics of memory cell array transistors, which had

150nm pitch, of 80nm DRAM was possible. It is concluded that a direct probing method using the nanoprober technique was very useful tool of the electrical failure analysis for 80nm DRAM and beyond generations.

14:30 3.3 New Methodology for the Characterization of EEPROM Extrinsic Behaviors,

Djafer Medjahed[1], Thierry Yao[1], Michael Yameogo[2], Pierre Gassot[1], and Dominique Wojciechowski[1],
[1]AMI Semiconductor Belgium BVBA, Belgium,
[2]University of Bordeaux, France

In medical and automotive applications, device reliability needs to be assessed with great precision. It is therefore mandatory to investigate deeply extrinsic behaviors of the devices to optimize their operating specifications in order to obtain the best endurance and retention characteristics. In this paper, we describe a new methodology to characterize the extrinsic behaviors of EEPROM devices that can be extended to other type of devices. We fully describe the architecture of the test structure that we have developed. Finally, we present results that validate this new methodology.

14:50 3.4 A 1 Mbit SRAM Test Structure to Analyze Local Mismatch beyond 5 Sigma Variation,

Thomas Fischer[1,2], Ettore Amirante[1], Alexander Olbrich[1], Peter Huber[1], Martin Ostermaier[1], Thomas Nirschl[1,2], Christopher Otte[2], Jan Einfeld[1], and Doris Schmitt-Landsiedel[2],
[1]Infineon Technologies AG, [2]Technical University of Munich, Chair for Technical Electronics, Germany

We present an area efficient test structure that allows a measurement of the statistical distribution of SRAM cell currents beyond 5 sigma variation. The test structure was fabricated in a 90nm and a 65nm CMOS technology. The measured data show that the device variations are Gaussian distributed for more than 1 million devices, covering more than 5 sigma of variation. Monte Carlo simulations are used to validate the measurements.

15:10 – 15:40 Break

SESSION 4: Matching

15:40 – 17:00

Co-Chairs: Mark Poulter, *National Semiconductor, USA*
Ulrich Schaper, *Infineon Technology, Germany*

15:40 4.1 Impact of Sinter Process and Metal Coverage on Transistor Mismatching and Parameter Variations in Analog CMOS Technology,

Xiaoju Wu, Joe Trogolo, Flex Inoue, Zhenwu Chen, Steve Burich, and Pam Jones-Williams, *Texas Instruments, USA*

In this paper, we report detailed studies on the impacts of sinter process and metal coverage on CMOS transistor matching and parameter variability in an analog CMOS technology. Transistor matching and parameter variations with different metal slotting sizes processed at different sinter temperatures have also been studied. It has been found that the both metal plating and sinter temperature play critical rules in transistor matching and parameter variation. Metal plating degrades VT and current matching (VT offset ~14-24mV, ΔI/I~18% at moderate inversion and ΔI/I~3% at strong inversion) significantly at low sinter temperature. Transistor matching improves at higher sinter temperature. Calculated current variations agree well with experimental results.

16:00 4.2 Rapid Characterization of Threshold Voltage Fluctuation in MOS Devices,

Kanak Agarwal, Sani Nassif, Frank Liu, Jerry Hayes, and Kevin Nowka, *IBM, Corp., USA*

We present a technique for fast characterization of random threshold voltage variation ins MOS devices and report results of VT scatter measurement from a test chip in a 65 nm SOI CMOS process. The magnitude of local device current mismatch caused by VT fluctuation is also measured and reported.

16:20 4.3 Impact of Transistor Matching on Features of Digital Circuit Blocks,

Ulrich Schaper, T. Kodytek, W. Kamp, and R. Künemund, *Infineon Technologies AG, Germany*

Digital circuit blocks are extracted from full custom digital circuits as units for test structures. The test structures are suited for a statistical evaluation of circuit features like the pre-charge of node voltages of fast decision circuits. A statistical evaluation is needed to account for process variations. The circuit characterization results allow a comparison with statistical device models. The constant margin procedure for the circuit performance can be replaced by realistic margins applying the characterization results.

16:40 Understanding the Carbon Impact on Si/SiGe:C HBT
4.4 Base Current Mismatch,

Stéphane Danaie[1,2], Mathieu Marin[1], Gérard Ghibaudo[2], Jean-Charles Vildeuil[1], Stéphanie Chouteau[1], Isabelle Sicard[1], and Augustin Monroy[1],
[1]STMicroelectronics, [2]IMEP/CNRS, France

In this paper, we have investigated the impact of carbon concentration on bipolar transistor matching at medium current region. Original base current matching results, obtained from the characterization of two carbon concentration splits in a SiGe:C BiCMOS technology, are first discussed and well interpreted by a new base current mismatch physical model. Our assumptions are also confirmed by a matching characterization of bipolar transistors subjected to a hot carrier injection (HCI) stress.

<u>**Wednesday, March 21**</u>

8:30 – 16:00 registration

<u>SESSION 5: Device Characterization II</u>

9:00 – 10:20

Co-Chairs: Bill Verzi, *Agilent Technologies, USA*
Yoshiaki Hagiwara, *Sony, Japan*

9:00 Automatic Extraction Methodology for Accurate
5.1 Measurement of Effective Channel Length on 65nm MOSFET Technology and Below,

Dominique Fleury[1], Antoine Cros[1,2], Krunoslav Romanjek[3], David Roy[1], Frank Perrier[3], Benjamin Dumont[1], and Hugues Brut[1], *[1]STMicroelectronics, [2]IMEP, [3]NXP Semiconductors, France*

Constant downscaling of transistors leads to increase the relative difference between L_{mask} and L_{Eff}. Effective length (L_{Eff}) extractions are now crucial to avoid calculations errors on parameters such as the mobility, which can exceed 100% for shorter devices. We propose an industrially-adapted method to extract L_{Eff} by using an enhanced "split C–V" method. Accurate and consistent values have been extracted (±1nm) and then correlated to mobility and HCI lifetime studies, as a function of L_{Eff}.

9:20 Faster ESD Device Characterization with Wafer-level
5.2 HBM,

M. Scholz[1], D. Trémouilles[1], D. Linten[1,2], Yves Rolain[2], Rik Pintelon[2], M. Sawada[3], T. Nakaei[3], T. Hasebe[3], and G. Groeseneken[4], *[1]IMEC, Belgium, [2]Vrije Universiteit Brussels, Belgium, [3]Hanwa Electronics Ind. Co. Ltd., Japan, [4]IMEC, also at Katholieke Universiteit, Leuven, Belgium*

HBM testers are tools for product qualification whereas TLP testers are used for device characterization. The ability to extract TLP-like IV curves from an HBM system is demonstrated in this paper. Together with measurement results on wafer-level the full methodology is presented and compared to standard 100ns TLP. The advantage of this methodology is that the quasistatic data of a device can be obtained much faster with only one test procedure.

9:40 5.3 A New Mixed Solution for Write-Margin Extraction in Advanced SRAM Characterization,

Nicolas Gierczynski[1], Bertrand Borot[2], Nicolas Planes[2], and Hugues Brut[2],

[1]Philips Semiconductors, [2]STMicroelectronics, France

As SRAM integration scheme becomes more and more aggressive in term of development time, supply voltage and geometric dimension, parameter extraction techniques need to be continuously upgraded to ensure the best support for technology development. An innovative approach for write-margin extraction has recently been published at the ISSCC'2006 conference. This approach makes use of test structure giving access to internal node. Here, this approach is evaluated through our 65nm process and it is shown that the layout and probing of the proposed test structure induces a write delay. As a consequence an adaptation of this innovative methodology is proposed. The new mixed solution gives promising results, in terms of accuracy and spread, to better follow the process development of advanced SRAM.

10:00 5.4 Scalable Approach for External Collector Resistance Calculation,

C. Raya[1,2], N. Kauffmann[1], F. Pourchon[1], D. Celi[1], and T. Zimmer[2],

[1]ST Microelectronics, [2]Université Bordeaux I, France

For device modeling purposes, the geometry dependence of the external collector resistance has been investigated. Firstly, using specific test structures and dc measurements, a new method to determine the different components of this resistance is presented. The external collector resistance could be separated in a vertical resistance perfectly 1D and a 2D horizontal contribution. An analytical scalable formula based on Fourier techniques takes into account the current distribution in the horizontal layer. This method is applied to a double poly ST BiCMOS technology and results are discussed.

10:20 – 10:50 Break

SESSION 6: Capacitance

10:50 – 12:10

Co-Chairs: Hugues Brut, *STMicroelectronics, France*
Jurriaan Schmitz, *University of Twente, the Netherlands*

10:50 6.1 Analog characterization of dielectric relaxation of MIM capacitor using an improved recovery voltage technique,

Zhenqiu Ning[1], Herman Casier[1], Renaud Gillon[1], H-X Delecourt[1], Dimitri Tack[1], Erwin de Vylder[1], Patrick van Torre[2], and Dan Hegsted[1],
[1]AMI Semiconductor, [2]Hogeschool GENT, Belgium

Dielectric relaxation of capacitor plays an important role in determining the accuracy of analogue sampled data systems that are based on charge storage, e.g. charge-redistribution A/D converters. To perform an accurate characterization of the dielectric relaxation of MIM capacitor, a technique based on voltage recovery principle has been developed, in which the effects of parasitic capacitance, leakage and mismatch on the characterization have been well minimized or canceled. The technique is proven to be highly accurate and flexible, while maintaining low cost.

11:10 6.2 Modeling the Mismatch of High-κ MIM Capacitors,

Mathieu Marin, Sébastien Cremer, Jean-Christophe Giraudin, and Bertrand Martinet,
STMicroelectronics, France

In this contribution we investigate the matching properties of modern high-κ metalinsulator-metal capacitors. In particular, we derive a physics-based model, in order to explain the observed geometry dependence of mismatch. This model is applied successfully to MIM devices processed with Ta_2O_5 and Al_2O_3 as dielectrics.

11:30 6.3 Gate Oxide Leakage and Floating Gate Capacitor Matching Test

Weidong Tian, Joe Trogolo, Bob Todd, and Lou Hutter,
Texas Instruments Inc., USA

Capacitor matching is an important device parameter for precision analog applications. In the last ten years, the floating gate measurement technique has been widely used for its characterization. As technologies advance, however, new challenges emerge. In this paper we describe the impact of MOSFET thin gate oxide leakage on the technique. SPICE simulation, bench measurement, analytical model and numerical analyses are presented to illustrate the problem and key contributing factors. In addition, we propose a field MOSFET approach to solve the

problem. Thick gate oxide MOSFET and Field MOSFET data are compared.

11:50 6.4 **Test Structures for Accurate UHF C-V Measurements of Nano-Scale CMOSFETs with HfSiO and TiN Metal Gate,**

KyongTaek Lee[1,4], George A. Brown[2], Dawei Heh[2], Rino Choi[2], Rusty Harris[2], Seung-Chul Song[2], Byoung Hun Lee[2], Ook-Sang Yoo[3], Hi-Deok Lee[3,4], and Yoon-Ha Jeong[1], *[1]Pohang University of Science and Technology (POSTECH), Korea, [2]SEMATECH,USA, [3]Chungnam National University, Korea, [4]Microelectronics Research Center, University of Texas, USA*

Test structures for accurate UHF capacitance-voltage (C-V) measurements of high performance CMOSFETs with Hf-based high-k dielectric and TiN metal gate are analyzed. It is shown that series resistance or substrate resistance between the channel region and body contact plays a role in UHF C-V measurements. The substrate resistance beneath the gate region also impacts accurate UHF C-V measurements. Therefore, short gate lengths with a minimum distance between the source/drain and body contact are necessary for an accurate evaluation of gate dielectric thickness using UHF C-V measurements.

12:10 – 13:30 **Lunch**

13:30 – 13:40 **ICMTS 2008 Presentation**

SESSION 7: Yield and Variation

13:40 – 15:00

Co-Chairs: Satoshi Habu, *Agilent Technologies, Inc., Japan*
Christopher Hess, *PDF Solutions, Inc., USA*

13:40 7.1 **A Large Scale, Flip-Flop RAM imitating a logic LSI for fast development of process technology,**

Masako Fujii, *Renesas Technology Corp., Japan*

We propose a new, large-scale, logic TEG, which is called Flip-Flop (FF) RAM, to improve the total process quality before the beginning of the first commercial products. It is designed for analysis as easy as an SRAM and imitating a logic LSI. We implemented 10M-gates FF-RAM using our 65 nm CMOS process. The test result shows that it is easy to detect the failure locations and layers by Fail Bit Map. Owing to this TEG, we can shorten the development period for advanced CMOS technology.

14:00 7.2 Development and Use of Small Addressable Arrays for Process Window Monitoring in 65nm Manufacturing

Muthu Karthikeyan[1], Arthur Gasasira[1], Stephen Fox[1], Greg Yeric[2], Michael Hall[2], John Garcia[2], Barry Mitchell[2], and Eric Wolf[2],
[1]IBM Systems and Technology Group, [2]Synopsys, USA

In this paper, we report on the development and use of two scribe-line compatible addressable array test structures in 65nm technology for routine process window monitoring. One array was dedicated for front-end of line test structures, while a second consists exclusively of back-end structures. Fast testing allows large-scale sampling of wafer lots in a manufacturing environment. Customized software is used to automate data analysis and calculate figures of merit that enable process and equipment performance to be tracked by process module. Several examples of the successful application of these arrays in addressing systematic yield detractors are provided

14:20 7.3 Test Structure for Process and Product Evaluation,

Jean-Michel PORTAL, *Laboratoire Matériaux et Microélectronique de Provence , France*

The objective of this paper is to present a test structure introduce in the scribe lines designed to detect process drift and to characterize product performances, i.e. delay and V. A brief overview of the structure, designed in a ST-Microelectronics 130nm technology, is given. The main advantages of the structure are to be introduced in the scribe line and to have a complex architecture close to the product back-end configurations. A specific test flow is applied to the structure in order to extract relevant data (frequency, delay and bias). The monitoring efficiency of the structure is validated with measurement correlation performed on the structure data, parametric test data and full test chip data.

14:40 7.4 Device Array Scribe Characterization Vehicle Test Chip for Ultra Fast Product Wafer Variability Monitoring,

Christopher Hess[1], Sharad Saxena[1], Michele Quarantelli[1], Angelo Rossoni[1], Stefano Tonello[1], Sa Zhao1, and Dustin Slisher[2],
[1]PDF Solutions Inc., [2]IBM Microelectronics, USA

Lower supply voltages and aggressive OPC on 65nm and below technologies are causing larger variability of critical device parameters like Vt and Id. With ever increasing clock frequencies, more and more performance related yield loss can be observed even for purely digital circuits. To design more robust circuits it is required to

characterize device variability within die, within wafer, wafer to wafer as well as lot to lot. Large samples of device measurements are necessary for accurate variability characterization. A novel Characterization Vehicle (CV) has been developed, which achieves an extremely efficient placement of several hundred devices by arranging them underneath the probing pads. Placed next to product chips, those Scribe CV test chips are providing Vtlin, Idlin, Vtsat, Idsat, Gmlin, and Gmsat for more than 25000 devices per 300 mm wafer requiring less than 20 minutes for testing.

15:00 – 15:20 Break

SESSION 8: Poster

15:20 – 18:30

Co-Chairs: Anthony J. Walton, *University of Edinburgh*
Yoshio Mita, *The University of Tokyo*

15:20 8.1 A Test Structure for Analysis of Asymmetry and Orientation Dependence of MOSFETs,

T. Matsuda[1], Y. Sugiyama[1], K. Nohara[1], K.Morita[1], H. Iwata[1], T. Ohzone[2], T. Morishita[2], and K. Komoku[2],
[1]*Toyama Prefectural University,*
[2]*Okayama Prefectural University, Japan*

A test structure to analyze asymmetry and orientation dependence of MOSFETs is presented. N-MOSFETs with 8 different channel orientation and three kinds of process conditions were measured and symmetry of IDsat and IBmax with respect to the interchange of source and drain was examined. Although both IDsat and IBmax have similar channel orientation dependence, only IBmax in interchanged S/D measurements show asymmetrical characteristics, which can be applied to a sensitive method for device asymmetry detection.

15:23 8.2 Automated on-wafer characterization in micro-machined resonators: towards an integrated test vehicle or bulk acoustic wave resonators (FBAR),

Humberto Campanella[1], Pascal Nouet[2], Pedro de Paco[3], Arantxa Uranga[3], and Jaume Esteve[1],[1]*Centro Nacional de Microelectrónica de Barcelona, Spain,* [2]*LIRMM, France,* [3]*Universitat Autònoma de Barcelona, Spain*

Electrical on-wafer characterization in FBAR is automated by means of a wide-band parameter extraction algorithm, in order to define a complete characterization vehicle or FBAR and MEMS resonators. A model of FBAR-substrate losses is proposed and an automation algorithm implementing a multi-step least-squares strategy is presented. Extraction of the equivalent-circuit parameters is performed from experimental s-parameter

data acquired by a microwave network analyzer. The results of FBAR and substrate characterization are presented, and the basis of an integrated test vehicle is discussed.

15:26 8.3 Excess Base Curren Model for Gamma-Irradiated SiGe Bipolar Transisors,

M. Ullán[1], J. P. Alegre[2], S. Díez, G. P llegrini[1], F. Campabadal[1], M. Lozano[1], and E. Lora-Tamayo[1],
[1]Centro Nacional de Microelectrónica de Barcelona, Spain,
[2]Universidad de Zaragoza, Spain

The radiation hardness of advanced SiG BiCMOS technologies is being evaluated in order to check their applicability for the front-end readout electronics of the ATLAS Upgrade in the framework of the Super-LHC at CERN. A model that describes the effect of ionizing radiation on bipolar transistors as an exponential term is widely accepted. Nevertheless, this model is not very precise in the bias ranges of interest for these applications. We propose a new empirical model that, by the inclusion of one extra parameter to the classical exponential model, describes more accurately the ionization radiation effects on SiGe bipolar transistors in the range of interest.

15:29 8.4 Array Based Test Structure for Optical-Electrical Overlay Calibration,

B.J.R. Shulver[1], A.S. Bunting[1], C. Dunare[1], L.I. Haworth[1], A.M. Gundlach[1], A.W.S. Ross[1], S. Smith[1], A.J. Snell[1], J.T.M. Stevenson[1], A.J. Walton[1], R.A. Allen[2], and M.W. Cresswell[2], *[1]The University of Edinburgh, UK, [2]National Institute of Standards and Technology, USA*

This paper describes the fabrication and electrical characterisation of a test structure for measuring overlay in interconnect systems. Such a structure provides the necessary measurements to calibrate optical overlay measurement tools. The design incorporates a large array of features with the potential to determine the overlay to within 10nm accuracy. Electrical measurements have been taken as a primary means of determining overlay and compared favorably with SEM measurements.

15:32 8.5 Development of Electrical On-Mask CD Test Structures Based On Optical Metrology Features,

A. Tsiamis[1], S. Smith[1], M. McCallum[2], A.C. Hourd[3], O. Toublan[4], J.T.M. Stevenson[1], and A.J. Walton[1],
[1]The University of Edinburgh, [2]Nikon Precision Europe, [3]Compugraphics International Ltd, [4]Mentor Graphics, UK

The standard approach to generate the data required for automated proximity correction is to measure a set of patterned features using an optical tool or a critical

dimension scanning electron microscope (CD-SEM). This paper describes the design of a set of on-mask electrical test structures to perform the same task which has a number of attractions. The electrical test structures are based on the Kelvin bridge resistor to measure the widths of isolated and densely packed lines and spaces. The results from these measurements can be used to extract information about proximity effects in the mask making process and to generate rules or models for the correction of mask designs. Electrical results from a test mask, fabricated without any correction for e-beam proximity effects, are presented and compared with optical measurements of the same structures made with an industry standard mask metrology tool.

15:35 8.6 Methodology for Performing RF Reliability Experiments on a generic Test Structure,

G.T. Sasse, R.J. de Vries, and J. Schmitz,
University of Twente, the Netherlands

This paper discusses a new technique developed for generating well defined RF large voltage swing signals for on wafer experiments. This technique can be employed for performing a broad range of different RF Reliability experiments on one generic test structure.

15:38 8.7 On-wafer RF Figure-of-Merit Circuit Block Design for Technology. Development, Process Control and PDK Validation,

S. Minehane[1], J. Cheng[1], T. Nakatani[2], S. Moriyama[1], B. Aghdaie[1], M. Sengupta[1], S. Saxena[1], S. Winters[1], H. Karbasi[1], M. Quarantelli[1], S. Tonello[1], and M. Redford[1],
[1]PDF Solutions, USA,
[2]Matsushita Electric Industrial, Japan

The inclusion of circuit-level blocks, such as ring oscillators, operational amplifiers and A/D or D/A converters, in technology characterization test chips is now a well-established practice. Such Figure-of-Merit (FoM) circuit blocks provide a means of judging technology performance and variability on-wafer during the technology development phase. In addition, FoM blocks are used to validate the ability of a PDK in capturing process behavior. This paper describes an extension of this concept to the RF domain, for a high-performance 0.18 µm SiGe:C-BiCMOS technology. The design of six different RF-FoM blocks, typically found in a transceiver, is presented. Test structure design considerations, including layout, pad-frame choice and probe-card design, are described. Finally, measured statistical results are presented. These designs enabled PDK verification and high-volume yield product samples.

15:41 8.8 Differential P+/Nwell varactor High Frequency Characterization

Yvan Morandini[1,2], Dario Rapisarda[1], Jean-Francois Larchanche[1], and Christophe Gaquière[2],
[1]STMicroelectronics, France, [2]IEMN, France

Here we report, the evaluation of two differential integrated diode varactor layouts. In a first time, differential structures connected to an integrated BalUn are characterized with a two ports vector network analyzer (VNA). Limitations of this method lead us to use four ports measurements. Results reveal the best layout for differential implementation and the sensitivity to common mode.

15:44 8.9 High-Q Slow-Wave Transmission Line for Chip Area Reduction on Advanced CMOS Processes,

Ivan Lai and Minoru Fujishima,
The University of Tokyo, Japan

A transmission line structure is presented in this work for advanced CMOS processes. This structure has a high quality factor and low attenuation. It allows slow-waves to propagate which results in a short wavelength for chip area-reduction. It is also designed to satisfy the stringent density requirements of advanced CMOS processes. Test structures were fabricated using CMOS 90nm process technology with measurements made up to 110 GHz.

15:47 8.10 Test Structure on SCR Device in Waffle Layout for RF ESD Protection,

Ming-Dou Ker and Chun-Yu Lin,
National Chiao-Tung University, Taiwan

With the highest ESD level in a smallest layout area, SCR device was used as effective on-chip ESD protection device in CMOS technology. In this paper, a waffle layout test structure of SCR is proposed to investigate the current spreading efficiency for ESD protection. The SCR in waffle layout structure has smaller parasitic capacitance under the same ESD robustness. With smaller parasitic capacitance, the degradation on RF circuit performance due to on-chip ESD protection device can be reduced. The proposed waffle SCR is suitable for on-chip ESD protection in RF applications.

15:50 8.11 Reducing measurement errors caused by a DC voltage dependence of kHz-GHz range bias-tees,

M.P.J. Tiggelman[1], K. Reimann[2], J. Schmitz[1], and R.J.E. Hueting[1], *[1]University of Twente,*
[2]Philips Research Laboratories, The Netherlands

To characterize tunable ferroelectric capacitors using a VNA, from the kHz-range up to the GHz-range, accuracy

can be lost using a wide-band bias-tee. A subtraction technique can significantly improve the measurement accuracy. Additionally, a new wide-band bias-tee has been developed with a NP0 capacitor which shows excellent performance in the complete frequency range of interest.

15:53 8.12 **The rectangular bipolar transistor tetrode structure and its application,**

M. Schroter[1,2] and S. Lehmann[2],
[1]*University of California San Diego, USA,*
[2]*Dresden University of Technology, Germany*

The operation of rectangular-shaped bipolar tetrode structures as well as the proper evaluation of measured data from such structures are discussed. Based on device simulation, which also serves for verification purposes, guidelines for the layout and measurement data correction are presented. The application to experimental data is demonstrated.

15:56 8.13 **Evaluation of 300 mm High Resistivity SOI Unibond material for RF applications up to millimeter wave using 65 nm CMOS SOI technology**

F. Gianesello[1], C. Raynaud[1, 2], D. Gloria1, S. Boret[1], and B. Gyselen[3]
[1]*STMicroelectronics,* [2]*CEA-LETI,* [3]*SOITEC, France*

In this paper, 300 mm High Resistivity (HR) SOI Unibond material is evaluated using RF component and millimeter wave (MMW) function realized in advanced 65 nm HR SOI CMOS technology. The goal is to investigate the insulating behavior, in term of resistivity homogeneity all over the wafer, of 300 mm wafer provided by SOITEC and to offer a benchmarking with well known 200 mm material in order to answer to the question of the maturity of advanced 300 mm HR SOI material. For this purpose a methodology based on high frequency measurement is proposed.

15:59 8.14 **Dynamic Analyses of Membranes and Thin Films on Wafer Level,**

Ronny Gerbach[1], Falk Naumann[1], Matthias Ebert[1], Joerg Bagdahn[1], Jens Klattenhoff[2], and Christian Rembe[2],
[1] *Fraunhofer Institute for Mechanics of Materials,*
[2]*Polytec GmbH, Germany*

A new approach is presented to monitor geometrical and material parameters of membranes and thin films for MEMS applications at wafer level. The method is based on the use of a combination of measurements via Laser-Doppler-Vibrometry and numerical simulations. The approach allows the characterization of devices during an

early fabrication stage. Experimental examples are given for the detection of geometrical parameters of silicon membranes in a production-related situation.

16:02 8.15 Quantitative analysis of Joule heating in suspended Greek cross test structures,

Stefan Enderling, J.T.M. Stevenson, and A.J. Walton,
University of Edinburgh, UK

This paper quantitatively analyses the Joule heating in suspended Greek cross test structures. The analysis was performed using Finite Element (FE) simulations, which indicated that most Joule heating occur sinfully suspended (undercut) test structures. The analysis has shown that the Joule heating effect can be dramatically reduced as along as test structures undercut by no more than 75% of its arm width. Using this design guideline, one can significantly reduce the sheet resistance measurement error, which is associated with the amount of Joule heating.

16:05 8.16 Improved Test Structure for Thermal Resistance Scaling Study in Power Devices,

Anna Canepari[1,2], Guillaume Bertrand[1], Alexandre Giry[1], Michel Minondo[1], Sylvie Ortolland[1], Herv. Jaouen[1], Bertrand Szelag[1], Jocelyne Mourier[1], and Jean-Pierre Chante[2], *[1]STMicroelectronics, [2]INSA Lyon, France*

Power MOSFETs suffer from a strong self-heating effect currently modeled with a thermal resistance Rth. Understanding the evolution of Rth with device scaling is today an important issue. This paper presents an improved test structure for temperature measurements in multiTnger LDMOS power devices. This structure allows accessing the temperature of every device Tnger. With this approach, impact of boundary effects and thermal coupling on Rth could be investigated. Measurements results are presented and a basic distributed model is used to reproduce Rth behavior.

16:08 8.17 A Continuous Model for MOSFET VT Matching Considering Additional Length Effects,

Samuel Bordez[1], Augustin Cathignol[1], Krysten Rochereau[2],
[1] STMicroelectronics, [2] NXP Semiconductors, France

MOS transistor threshold voltage matching is usually modeled proportionally to reverse square root of gate area. Yet this model is not satisfactory when discontinuities are observed. In this paper, a continuous matching model with only two parameters is given. It is obtained by analyzing impact of Short Channel Effects on matching degradation.

16:11 8.18 From Matching Test Structures to Matching Data Utilization: Not An Ordinary Task.

Augustin Cathignol[1,2], Samuel Bordez[1], and Krysten Rochereau[3], Gerard Ghibaudo[2], [1]*STMicroelectronics,* [2]*IMEP, Minatec, INPG,* [3]*NXP semiconductors, France*

Delivering mismatch data that reflect design reality is a real challenge. Indeed, from test structures to final data, many steps can be the source of distortion. The first possible source of distortion is linked to the differences in terms of environment and spacing that might exist between test structure transistors and circuit transistors. The second potential source of distortion is related to the measurements and extraction that can both add extra mismatch. Finally, the data treatment and utilization can constitute other error sources. In this paper, thanks to results from various test structures and device types, the main sources of distortion are pointed out in order to help to set up a reliable chain from matching test structures to matching data utilization.

18:30 Banquet Bus Departure from Takeda to *Chinzanso*

19:00 – Conference Dinner including "*koto*" concert.

Thursday, March 22

8:30 – 11:00 Registration

SESSION 9: RF

9:00 – 10:30

Co-Chairs: Tatsuya Ohguro, *Toshiba Corp., Japan*
Willy Sansen, *IMEC, Belgium*

9:00 9.1. A Scalable Transmission-Line Based Technique for De-Embedding Noise Parameters,

Kenneth H.K. Yau[1], Alain M. Mangan[1], Pascal Chevalier[2], Peter Schvan[3], and Sorin P. Voinigescu[1],
[1]*University of Toronto, Canada,*
[2]*STMicroelectronics, France,* [3]*NORTEL, Canada*

A transmission line-based de-embedding technique for on-wafer S parameter measurements is extended to the noise parameters of MOSFETs and HBTs. Since it accounts for the distributed effects of interconnects and for the pad-interconnect discontinuity, it is expected to yield more accurate results at high frequencies than existing approaches. Experimental validation is provided on 90 nm and 130 nm n-MOSFETs and SiGe HBTs and its accuracy is compared with other lumped or distributed de-embedding techniques.

9:20 9.2 A Novel RF-WAT Test Structure for Advanced Process Monitoring in SOC Applications,

David C. Chen, Ryan Lee, C. Liu, Mao Chyuan Tang, Annie Kuo, C. S. Yeh, S. C. Chien, and S. W. Sun
United Microelectronics Corporation, Taiwan

We propose a novel test structure for radio frequency wafer acceptance test at the scribe line area to monitor the RF device performance data and extract an accurate device parameter of the advanced processes especially for the SOC applications. Three different layout styles with scribe line S-GSG, GSSG or GSGSG are investigated. Excellent agreement of 65nm NMOS RF-CV mapping data among S-GSG, GSSG and GSGSG in a 12” wafer is demonstrated.

9:40 9.3 Accurate Inductance De-embedding Technique for Scalable Inductor Models,

Volker Blaschke and James Victory,
Jazz Semiconductor, USA

We present a semi-analytical de-embedding technique that accounts for the magnetic coupling between test structure feed-lines and device under test (DUT) to achieve scalable and physical based model. The method significantly improves the result of extracted inductance and enables broadband frequency characterization of square and octagonal inductors in single-ended and differential configuration over a large space of geometries.

10:00 9.4 Coupling on-wafer measurement errors and their impact on calibration and de-embedding up to 110 GHz for CMOS millimeter wave characterizations,

C. Andrei, D. Gloria, F. Danneville, P. Scheer, and G. Dambrine, *IEMN, France*

An investigation of parasitic coupling that occurs when making on-wafer measurement at millimeter wave range is described. Several passive structures dedicated to de-embedding of MOSFETs are experimentally studied and compared to HFSS electromagnetic simulations in order to highlight parasitic coupling and identify causes of measurement errors. Suggestions on coupling between adjacent test structures and/or probe to back-end environment are also discussed.

10:20 – 10:40 Break

SESSION 10: Parameter Extraction and modeling

10:40 – 12:00

Co-Chairs: Stewart Smith, *The University of Edinburgh, UK*
Colin McAndrew, *Freescale Semiconductor, USA*

10:40 10.1 Benchmarking PSP Compact Model of MOS Transistors,

Xin Li[1], Weimin Wu[1], Amit Jha[1], Gennady Gildenblat[1], Ronald van Langevelde[2], Geert D.J. Smit[3], Andries J. Scholten[3], Dirk B.M. Klaassen[3], Colin C. McAndrew[5], Josef Watts[5], Michael Olsen[6], Geoffrey Coram[7], Samir haudhry[8], and James Victory[8],
[1]Arizona State University, USA, [2]Philips Research Laboratories, The Netherlands, [3]NXP Corporate Research, The Netherlands, [4]Freescale Semiconductor, USA, [5]IBM Semiconductor Research and Development Center, System and Technology Group, USA, [6]IBM Semiconductor Research and Development Center , USA, [7]Analog Devices, Inc. ,USA, [8]Jazz Semiconductor ,USA

Recently PSP model was selected as the first surface-potential-based industry standard compact MOSFET model. This work presents the results of several qualitative “benchmark” tests that over the last two years were used to verify the physical behavior of the new model and its usefulness in the future generations of CMOS IC design. These include newly developed tests and previously unavailable experimental data stemming from the low-power, RF, mixed and analog applications of MOSFETs.

11:00 10.2 Novel parameter extraction method for low field drain current of nano-scaled MOSFETs,

Takuji Tanaka, *Fujitsu Ltd., Japan*

We developed parameter extraction method based on a BSIM3-like compact model to analyze low field drain current with size dependent mobility in nano-scaled MOSFETs. Our new straightforward algorithm has made it possible to automatically extract model parameters with high accuracy and robustness. It is applicable to wide variation of device sizes, structures and materials.

11:20 10.3 Unified model for integrated resistors in CMOS technologies,

C. Codegoni, I. Aureli, D. Ventrice, and P. Fantini, *STMicroelectronics, Italy*

We have presented a flexible compact model for resistors including bias-induced narrow width effects, head resistance modeling, velocity saturation contribution at high longitudinal field and the temperature resistance

dependence accounting for self-heating effect too. The completeness and robustness of our model are supported by considering a wide fan of experimental data on various kinds of integrated resistors in CMOS technologies.

11:40 10.4 **Extraction of Self-Heating Free I-V Curves Including the Substrate Current of PD SOI MOSFETs,**

Qiang Chen, Zhi-Yuan Wu, Richard Y.K. Su, Jung-Suk Goo, Ciby Thuruthiyil, Martin Radwin, Niraj Subba, Sushant Suryagandh, Tran Ly, Vineet Wason, Judy X. An, and Ali B. Icel, *Advanced Micro Devices, USA*

A new methodology is proposed to extract self-heating free I-V curves, including the substrate current, of SOI MOSFETs based on triple-temperature, regular DC measurement. It is verified to be accurate with Hspice simulations and suitable for SPICE model parameter extraction. It is also demonstrated that extraction of self-heating free I-V curves is not only desired for efficient SPICE model generation, but also required to accurately capture the true temperature dependence in the models.

12:00 **End of Exhibition**

12:00 **Best Paper Announcement**

Closing Remarks

12:05 **End of Conference**

12:05 **Optional Excursion "*Tokyo afternoon*"**

(Lunch is offered for Excursion participants)

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ICMTS2007 Condensed Program

Monday March 19

- 9:00 Introduction
- 9:05 Test Structure Fundamentals
- 9:55 Efficient Usage of Test Structures
- 10:45 Break
- 11:00 Physics and Technology of Strained-Si CMOS
- 11:50 MEMS Reliability
- 12:40 Lunch
- 13:40 Approaches to Ultra low-k1 Lithography
- 14:30 Global Interconnect Characterization, Testchip, Structures, Modeling, and Statistics for BEOL
- 15:20 Break
- 15:50 On-wafer evaluation for high-frequency CMOS devices
- 16:40 SPICE Modeling
- 17:30 Wrap-Up and Conclusion
- 18:00 Welcome Reception at foyer

Tuesday March 20

- 8:00 Registration
- 9:00 Opening Remarks
- 9:10 Session1: CD Metrology
- 10:30 Exhibition and Break
- 11:00 Session2: Process Characterization
- 12:20 Lunch
- 13:50 Session3: Device Characterization I
- 15:10 Break
- 15:40 Session 4: Matching

Wednesday March 21

- 8:30 Registration
- 9:00 Session5: Device Characterization II
- 10:20 Break
- 10:50 Session6: Capacitance
- 11:00 Session2: Process Characterization
- 12:10 Lunch
- 13:30 Session7: Yield and Variation
- 15:00 Break
- 15:40 Session 8: Poster
- 18:30 Bus departure for Banquet@Chinzanso

Thursday March 22

- 8:30 Registration
- 9:00 Session9: RF
- 10:20 Break
- 10:40 Session10: Parameter Extraction and Modeling
- Best Paper Announcement
- Closing Remarks and End of Conference
- Lunch (For excursion attendee only)
- Excursion “*Tokyo Afternoon*”