ICMTS 2005
International Conference on Microelectronic Test Structures

Tutorial and Technical Program

April 4-7, 2005
De Valk, Tiensestraat 41, Leuven
Belgium

ICMTS2005
http://www.see.ed.ac.uk/ICMTS/

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GENERAL INFORMATION

Conference Information

The IEEE Electron Devices Society is sponsoring the 2005 International Conference on Microelectronic Test Structures.

The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The Conference will be preceded by a one-day Tutorial Short Course on Microelectronic Test Structures.

ICMTS 2005

http://www.see.ed.ac.uk/ICMTS/

Presentation

The official language of the conference is English and it will be used for all presentations and printed materials. Only a data projector connected to a laptop PC will be available for your presentation of ICMTS 2005. We prefer the usage of the data projector connected to a PC for a seamless presentation flow. We will prepare a laptop PC and accept presentations as PDF files or MS Power Point files only. These files have to be sent to the Technical Chairman and the ICMTS secretariat until March,18, 2005 by e-mail. Please bring a backup file on USB memory stick, CD-ROM or floppy disk of your presentation, in case something accidentally does not work on the data projector as expected. There will be no slide projector available. All speakers are requested to report to the speakers registration desk located in front of the conference room before their presentation.

Best Paper Award

One paper presented will be selected for the Best Paper Award. Presentation of the award will be made at the ICMTS 2006.

Conference Proceedings

The IEEE ICMTS 2005 will publish proceedings. One copy of the proceedings is included in the registration fee. Additional copies will be available at the Conference for 100 Euro per copy for members of the IEEE, or 130 Euro per copy for non-members, or from the IEEE after the conference.

Registration

Please visit the ICMTS website (http://www.see.ed.ac.uk/ICMTS/) to download the registration form, fill in the form and send it to ICMTS 2005 conference services AIMS by FAX or email.

AIMS International Congres Services

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Conference registration fees in Euro

Herewith you can find the conference fees for early, late, and on-site registrants.

Early Registration:(Registered by February 28, 2005)

	Member*	Non Member	Student**
Tutorial	220	280	120
Technical Sessions	400	480	200

Late Registration:(Registered after March 1,2005)

Tutorial	270	330	150
Technical Sessions	450	530	250

On-site Registration:(Registration at the Conference)

Tutorial	320	380	180
Technical Sessions	500	580	300

* Must be a member of the IEEE or IEICE or JSAP

** To qualify for reduced conference rates, you must be a Student Member, a full time student, not be self-employed, nor working part or full time at a facility or corporation.

Registration fees include admittance to technical sessions, equipment exhibits, morning and afternoon coffee breaks, reception, conference banquet, one copy of the proceedings.

On-site registration schedule

On-site registration for the conference will be conducted at the Registration Counter AIMS, De Valk, Tiensestraat 41, 3000 Leuven

Monday, April 4	8:00-17:00
Tuesday, April 5	8:00-17:00
Wednesday,April6	8:30-17:00
Thursday,April 7	8:30-11:00

Payment of the registration fees

Payment for registration fee, hotel and transport has to be made in EURO.
Please transfer the amount to the conference account :
ING 310-1264125-10 IBAN BE41 3101 2641 2510 – BIC.BBRUBEBB

Do not forget to indicate your name and the purpose of your payment: "ICMTS 2005".
Please enclose a copy of the bank transfer with your registration form.
Banking fees have to be settled by the remitter.

Credit Cards are accepted in Euro: Master Card, VISA, American Express as indicated on registration form. Cash in Euro will be accepted only at the conference registration desk.

Cancellation

Due to advance financial commitments, refunds of registration fees requested after March 1, 2005, cannot be guaranteed. 40 Euro processing fee will be withheld from all refunds. Requests for refunds of registrations cancelled after March 1 will be considered after the conference.

Messages
Messages will be placed on a Message Board beside the registration desk.
A number of PC's will be available to read and send e-mails.

Banquet
The conference banquet will be held on Wednesday evening, April, 6 at 19:00 at Faculty Club, Groot Begijnhof, Leuven. Conference registration fees include one banquet ticket. Guest ticket will be available for sale at the registration desk at the price of 85 Euro.

Excursion
We have arranged an excursion on Thursday, April 7.
Visit of Leuven and Brussels.
Time: 14:00-19:00
Fare: 60 Euro/person

Information about Leuven
The town Leuven covers an area of 14,371 acres and consists of the following boroughs: Heverlee, Leuven, Kessel-Lo, Wilsele and part of the former municipalities: Wijgmaal, Korbeek-Lo and Haasrode. Since 1 January 2001 Leuven has 88.564 inhabitants.

The history of Stella Artois is closely connected with the history of Leuven. The foundation of the university of Leuven in 1425, the digging of the canal Leuven-Rupel in the 18th century, two industrial revolutions and two world wars; all were events that played a fundamental part in the development of this beer town and... of the brewery Artois.

The University of Leuven is famous not just within the borders of Belgium, but far beyond as well. Being a very lively city of and for students, Leuven aspires to maintain that reputation. In contrast to most university cities, Leuven does not have a closed campus. The University buildings are spread throughout the city and were originally built for completely different purposes.

The conference site is the College of the Falcon ' De Valk' , located at: Tiensestraat 41. This is the former college of the Arts Faculty, which was founded around 1434 and moved to this site in 1543. The classical buildings were built on this site in 1783 and renewed at the end of the previous century. The Faculty of Law is based here. In 1966 a new complex was added next to the old college.

Climate and clothing

The temperature in Leuven during the conference period will range between 6 °C and 14 °C. The average humidity is 81 %. The weather, during spring is often very unpredictable, so a sweater or coat is recommended.

Hotel Accommodations

AIMS has been appointed as Destination Management and registration desk for the Conference and will handle all hotel accommodation. Fill in the application form on the ICMTS website (http://www.see.ed.ac.uk/ICMTS/). Inquiries and applications concerning arrangements should be addressed to:

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Equipment Exhibition

An equipment exhibition will be held besides the conference room during the conference to display equipment closely paralleling the nature of this meeting. This equipment exhibition will permit one-on-one discussions between exhibitors and conference attendees on the latest test equipment. Exhibits will be open as follows.

April 4 13:00 - 17:00
April 5, 6 9:00 - 17:00
April 7 9:00 - 12:00

The exhibitors list will be distributed on the day of the conference.

Route description to Leuven

By air

In the Zaventem - Brussels Airport, take the train to Brussel Noord (about 15 minutes), and change for Leuven (about 20 minutes). Direction Liège or Hasselt or …

By car coming from Brussels or Liege

- take the highway E40 (Brussels - Liege)
- take the exit E314 / Leuven (no. 15)

By car coming from Hasselt / Eindhoven / Aachen

- take the highway E314 (Aachen - Leuven).
- take the exit "Leuven" (no. 15). This is the last exit before the E40.

By train and bus

Please pay attention to the fact that you have to take the train to Leuven and not to Louvain-la-neuve (Louvain-la-neuve is situated near Wavres and houses the French speaking campus of the Katholieke Universiteit), which was created in 1972.

ICMTS 2005
CHAIRMAN'S LETTER

Dear colleague,

On behalf of the steering and technical program committees, I take pleasure in welcoming you to the 2005 International Conference on Microelectronic Test Structures (ICMTS-2005) in Leuven, Belgium on April 4 - 7, 2005. It is the 18th ICMTS as an international conference and the very first one in Belgium. The conference is sponsored by the IEEE Electron Devices Society.

The purpose of this conference is to bring together designers and users of test structures to discuss recent developments and future directions. This ICMTS-2005 conference brings 3 invited talks, 45 oral papers and several poster papers.

The first invited talk is on the Technology characterization of 90 nm CMOS towards high yield. It will be delivered by Ann Kelleher of Intel, Kildare, Ireland. The second invited talk is on Reliability Assessment of Advanced CMOS Technologies by Guido Groeseneken, of IMEC, Leuven, Belgium. The third invited talk is by George Brown of Sematech, USA. He will discuss the Intimate relationship between test structure design, equivalent circuit and measurement technology by use of capacitance characterization.

There is no doubt that test structures will play an ever more important role for new process, device and circuit developments once deep submicron or nano CMOS technologies become mainstream. Indeed test structures have become essential for accurate modeling and for the prediction of mismatch, 1/f-noise and high-frequency behavior. Moreover test structures have played an essential role for improvements in yield, both within factories as between factories.

On the Monday before the conference, on April 4th, a single-day Tutorial Short-Course will be held. This course is intended to provide the participants with instructions on test structure design, measurement and analysis. The instructors have many years of experience in this field. They will cover topics such as Test Structure Fundamentals (A. Walton, University Edinburgh), Introduction to MEMS test structures (M.McNie, QinetiQ), Stress-induced leakage paths in thin-gate oxides (R.Degraeve, IMEC), Test structures and methodologies for the assessment of back-end-of-line reliability (C.Bruynseraede, IMEC), Low-frequency noise as a diagnostic tool (C.Claeys, IMEC), RF Characterization of Silicon Devices (F. Sischka, Agilent), Modeling of RF CMOS (K.McCarthy, University Cork) and MOSFET matching (J. Croon, IMEC).

During the conference, an equipment exhibit is set up as well, to illustrate the latest measurement techniques on test structures. Wafer probing, data analysis, parameter extraction are among the techniques demonstrated.

The conference will be held in the College, "De Valk", in the center of Leuven, which is situated about 25 km East of the center of Brussels.

The program of this conference has been put together by the Program Committee, chaired by Ulrich Schaper (Infineon, Munich), whom I want to thank. I also want to thank A. Walton (University Edinburgh) for his guidance, and all members of the

steering committee.

I hope that ICMTS-2005 conference will bring you the technical expertise that you are looking for, but in addition, the opportunity to learn about the interests and the cultural background of your colleagues engineers. Also I hope you will enjoy your stay in Leuven, which is the oldest university town in the North of Europe. It hosts the largest university in Belgium and IMEC, the largest independent semiconductor laboratory in Europe.

We are looking forward to meeting you all in Leuven !

Willy Sansen
General Chairman

Tutorial Short Course

Monday, April 4

Tutorial Program

9:05

1. Test Structure Fundamentals
Anthony J. Walton (The University of Edinburgh)

This presentation will begin with a review of test chips briefly detailing their history and their application. The presentation will include a brief review of test structures for measuring sheet resistance, line width and contact resistance. Measurement and equipment issues will be addressed focusing on procedures for obtaining accurate and repeatable measurements.

9:55

2. Introduction to MEMS test structures
Mark McNie (QinetiQ)

When developing MEMS processes, the mechanical properties of a material must be considered in addition to the electrical properties. This lecture will introduce the use and limitations of test structures and techniques used to characterize the mechanical properties of layers used in a MEMS process. Test structures enable a stable process window to be developed and maintained, enabling the use of CAD to design practical devices. Examples will be given based on the INTEGRAM MPW processes - metal-nitride surface micromachining, polysilicon surface micromachining and SOI micromachining.

10:25 Coffee Break

10:55

3. Stress-induced leakage paths in thin gate oxides: from hard breakdown to micro breakdown
Robin Degraeve (IMEC)

Hard breakdown, analog and digital soft breakdown, micro breakdown, progressive breakdown, stress-induced leakage current, anomalous stress-induced leakage current, etc... When a constant voltage stress is applied to a thin (<10 nm) oxide layer many degradation phenomena are observed. All of these have in common that they are localized stress-induced leakage paths involving electrical trap centers in the bulk of the oxide, but different names are in use depending on the magnitude of the leakage current or on the application where they are typically measured. Some of these stress-induced leakage paths can be negligible artifacts for one application while they are showstoppers for another

application. This tutorial aims at presenting a comprehensive overview of all these dielectric breakdown phenomena, explaining their origin and showing what test methods and structures are needed to observe and study them.

11:35

4. Test structures and methodologies for the assessment of back-end-of-line (BEOL) reliability
Christophe Bruynseraede and Zsolt Tõkei (IMEC)

Back-End-of-Line reliability, comprising barrier, dielectric and current-carrying metal reliability, is a major challenge for future IC generations. It is generally reported that the reliability margin of the dielectric/barrier/copper system is shrinking. Material selection, integration schemes, test structure design and virtually all fabrication steps affect the BEOL performance and reliability. Appropriate test methodologies and test structures that are capable of assessing these complex relationships are a must. In this tutorial the impact of test structures on the assessment of quasi-intrinsic and integration performance will be outlined and illustrated by recent experimental reliability data. Interconnect reliability issues to be covered deal with the barrier and dielectric part, as well as with the Cu or Al part of the BEOL stack (electromigration and stress-induced-voiding).

12:15 Lunch

13:40

5. Low Frequency Noise as a Diagnostic Tool for Advanced Semiconductor Material and Device Characterization
Cor Claeys (IMEC)

This tutorial focuses on the different types of noise occurring in deep submicron silicon MOSFETs and their use as an analytical tool. The noise sources comprise white noise, Generation-Recombination (GR) noise, Random Telegraph Signal (RTS) fluctuations and 1/f or flicker noise. The fundamental basis of each noise type will be briefly described and illustrated by some practical examples. In a second part, the impact of the properties of the silicon substrate (orientation, crystallization technique, SOI, SiGe) on the noise performance is discussed. Finally, the impact on the low-frequency (LF) noise behavior of different advanced process modules, such as gate stack (thermal SiO_2, nitrided oxides, high-k materials, metal gates), device isolation (LOCOS and STI based), silicidation, and gate engineering is illustrated. Some state of the art processing such as e.g. FUSI and strained SiGe layers will also be discussed.

14:30

6. RF Characterization of Silicon Devices (including non-linear network measurements)
Franz Sischka (Agilent)

Characterizing silicon devices has become more challenging due to the improved speed performance of modern technologies. This implies to pay more attention to accurate RF measurements and especially to reliable verification procedures. Besides verifying the network analyzer calibration quality, special attention has to be given to accurate de-embedding results. And for nonlinear devices like transistors and diodes, the additional challenge is to combine that with consistent DC measurements. While S-parameter cover the linear range of RF performance, Spectrum Analyzers and even Nonlinear Network Analyzers are applied to characterize the device behavior in the real application conditions and not only in the linear micro-watt RF range. The tutorial will give an overview about methods and actual trends.

15:20 Coffee Break

15:50

7. Modeling of RF CMOS
Kevin McCarthy (University College Cork

RF circuit design based on advanced deep-submicron CMOS is now a reality with both products and research papers appearing regularly on this topic. This dramatic increase in the use of CMOS for RF applications has created a need for improved MOSFET modelling at RF that in turn has led to significant model developments in recent years. This tutorial begins by looking at the core building blocks and equations of a MOS model and then discusses how modern RF models are built from this basic framework by considering the modelling of parasitics, non-quasi-static effects, distortion, noise and other effects. The most important recent developments are reviewed and measured and simulated data is shown to provide insight into the new models and to illustrate the high accuracy that can be achieved. Finally, the tutorial concludes with a review of the remaining MOS modelling challenges for RF that provide the seed for future research and developments.

16.40

8. MOSFET matching: Modeling, characterization, and physical aspects
Jeroen Croon (IMEC)

No two MOSFETs are identical at the nanoscale level. Small differences cause inaccuracies in analog circuits, and, because of the downscaling of transistor dimensions, also the yield of digital designs is affected. Spatial fluctuations of MOSFET parameters are analyzed by matching two supposedly identical transistors, and by investigating the stochastic properties of the measured

difference.
After an introduction, this tutorial firstly compares several modeling approaches for describing the differences between transistors. In literature, no clear consensus exists on how this should be done, and it is tried to list the merits and difficulties associated with different methodologies. Secondly, some common measurement pitfalls are presented and several test structures are compared. This tutorial concludes by briefly explaining some of the physical aspects of matching theory, which allows us to identify future issues related to the characterization of MOSFET mismatch.

17:30 Wrap-Up and Conclusion

18:00 Welcome Reception in the Valk

ICMTS 2005 Tutorial Lecturer Biography

Anthony J. Walton

Anthony J. Walton is professor of Microelectronic Manufacturing in the School of Engineering and Electronics at the University of Edinburgh. He has been actively involved with the semiconductor industry in a number of areas associated with silicon processing which includes both IC technology and micro-systems. For the 20 years he has had a direct interest in the design, fabrication and measurement of microelectronic test structures and has taken an active role in the organization of ICMTS. He played a key role in setting up the Scottish Microelectronics Centre (SMC) which is a purpose built facility for R&D and company incubation consisting of approximately 300m2 of class 10 clean rooms. He has published widely on test structures and is an associate editor of the IEEE Transactions on Semiconductor Manufacturing.

Mark McNie

After graduating in Physics (Imperial College, UK) in 1990, Mark McNie completed a MSc in Electronics (Nottingham, UK) in 1991. He worked on high temperature superconductors and III-V HBT devices before joining QinetiQ (formerly DERA) in 1995 to work on silicon-based MEMS. His areas of interest include microinertial sensors, optical MEMS and associated process technologies. He is technical prime for the INTEGRAM manufacturing cluster - part of the EUROPRACTICE foundry access programme. He has recently led the integration chapter of MANCEF/SEMI international roadmap on "The Commercialisation of MEMS", is co-chair of the MRS symposium on Micro- and Nanosystems, is a member of the IoP and IEE, and has published many papers and patents in the field.

Robin Degraeve

Robin Degraeve received the M.Sc. degree in electrical engineering from the University of Gent, Belgium, in 1992, and the Ph.D. degree from the Catholic University of Leuven, Belgium, in 1998.
He joined the Interuniversity Microelectronics Center (IMEC), Leuven, in 1992 in the CMOS Reliability group, where he is currently working as a Senior Researcher. His work has been focussing on reliability aspects of thin insulating layers under electrical stress. His current interests and activities include hot-carrier related reliability issues in MOSFETs, the study of the physics of degradation and breakdown phenomena in gate oxide films, the reliability of flash memory devices, the reliability of ultrathin oxide and oxynitride layers for VLSI technologies, and the reliability of high-k materials as MOSFET gate insulators for future CMOS generations

Christophe Bruynseraede

Christophe Bruynseraede received the M.S. degree in electrical engineering in 1993 and the Ph.D. degree in 2000, both from the Katholieke Universiteit Leuven, Leuven,

Belgium. He is currently continuing his research at the Interuniversity Microelectronics Center (IMEC), whereby his main research interests are focused on reliability issues (electro-and stressmigration) in advanced Cu/low-k interconnects. He has authored and coauthored 35 papers and conference contributions in the fields of opto-electronics, magneto-electronics and BEOL reliability

Zsolt Tõkei

In the framework of a co-directed thesis between the Hungarian university of Debrecen and the French university Aix-Marseille-III, Zsolt T_kei received his PhD degree in materials science in 1997. His work concentrated on diffusion studies of metals in Cu-alloys and intermetallic compounds. After finishing his PhD, he worked for 20 months at the Max-Planck Institute of Düsseldorf as a Post Doctorate researcher in the field of high temperature oxidation/corrosion processes. In 1999 he joined the Interuniversity Microelectronics Center (IMEC) as a researcher in the field of Cu-low-k interconnects. His current interest is focusing on the reliability of copper low-k interconnects. He has authored and coauthored more than 30 papers and over 40 conference contributions.

Cor Claeys

Cor Claeys received the electrical-mechanical engineering degree in 1974 and the Ph.D. degree in 1979, both from the Katholieke Universiteit Leuven (KU Leuven), Belgium.
From 1974 to 1984 he was a Research Assistant and Staff Member, respectively, of the ESAT Laboratory of the KU Leuven and since 1990, a Professor. In 1984, he joined IMEC as Head of Silicon Processing Group. Since 1990 he is Head of the research group on Radiation Effects, Cryogenic Electronics and Noise Studies. He is also responsible for Technology Business Development. His main interests are in general silicon technology for ULSI, device physics, including low-temperature operation, low frequency noise phenomena and radiation effects, and defect engineering and material characterization. He coedited a book "*Low Temperature Electronics*" and wrote a book "*Radiation Effects in Advanced Semiconductor Materials and Devices*". He also authored and co-authored six book chapters and more than 600 technical papers and conference contributions related to the above fields. He is an associated Editor for the *Journal of the Electrochemical Society.*
Dr. Claeys is a member of the European Material Research Society, a Senior Member of IEEE and a Fellow of the Electrochemical Society. He was the founder of the IEEE Electron Devices Benelux Chapter and is presently elected AdCom member of the Electron Devices Society and Vice-President for Chapters and Regions. He also received the IEEE Third Millennium Medal. In 1999 he was elected as Academician and Professor of the International Information Academy. In 2004 he received the Electronics Division Award of the Electrochemical Society.

Franz Sischka

Franz Sischka studied Electronic Communication Engineering at the University of Stuttgart, Germany, where he received his Diplom-Ingenieur and Ph.D. degrees in 1979 and 1984. After joining Hewlett-Packard in Germany, he worked for 5 years in R&D in

the fiber optics group at HP Boeblingen. Since 1989, he is consultant for Agilent-EEsof's simulation and modeling software.
He has given invited device modeling tutorials at the VLSI 1999 (Lisbon) and also at the ICMTS 1999 (Gothenburg) and ICMTS 2000 (Monterey) as well as at the MIXDES 2001 (Zakopane) and Wireless Design Conference 2002 (London) conference. Also, he is the author of Agilent's IC-CAP Modeling Reference book.

Kevin G. McCarthy

Kevin G. McCarthy (MIEI, MIEEE) obtained the B.E., M.Eng.Sc. and Ph.D. degrees from University College Cork (UCC), Ireland in 1982, 1986 and 1992 respectively. He is a lecturer in the Department of Electrical and Electronic Engineering, UCC, where his main teaching and research interests are communications and microelectronic devices and circuits for communications, especially in the RF and mixed-signal area. Previously, he was a senior research scientist at the National Microelectronics Research Centre, Ireland (NMRC) where he worked on the simulation of advanced MOSFET and bipolar devices for digital and analog applications with emphasis on parameter extraction and statistical analysis methodologies. Before joining UCC/NMRC he worked with Analog Devices in product engineering and CAD engineering roles. He has authored or co-authored 35 publications and is a member of the 2005 technical program committees of ICMTS, ESSDERC and the RFIC Symposium.

Jeroen Croon

Jeroen Croon was born in Delft, The Netherlands, on March 18, 1975. In 1998 he received a Master's degree in applied physics from the Delft University of Technology. His thesis involved the optimization of the receiving coil and pre-amplifier of an Overhauser MRI system at 77 K and at room temperature. After this he started working in IMEC, Belgium, and in 2004 he obtained a Ph.D. degree in electrical engineering from the Katholieke Universiteit of Leuven, also in Belgium, for his study of the matching properties of deep submicron MOSFETs. His current research in IMEC involves the characterization of MOSFETs fabricated on germanium substrates, and the study of variability in advanced CMOS processes.

ICMTS 2005 Invited Speakers Biography

George A. Brown

George A. Brown is a Fellow, Technical Staff at SEMATECH, assigned to the Front End Processes division. At SEMATECH, he is involved in the electrical and reliability characterization of high-k gate stack and gate electrode materials.
He received the B.S.E.E. degree from the University of Pennsylvania in 1959 and the M.S.E. from Princeton University in 1961. Prior to joining SEMATECH, he retired from Texas Instruments, Inc., as a Distinguished Member, Technical Staff with 37 years of service. Early in his career he was with RCA Laboratories, Princeton, NJ,

where he was involved in the development of the MOS transistor device. He is a Life Senior Member of the IEEE and a member of the Electrochemical Society.

Guido Groeseneken

Dr. Guido Groeseneken received the M.Sc. degree in electrical and mechanical engineering (1980) and the Ph.D degree in applied sciences (1986), both from the Katholieke Universiteit Leuven, Belgium. In 1987 he joined the R&D Laboratory of IMEC (Interuniversity Microelectronics Center) in Leuven, Belgium, where he is responsible for research in reliability physics for deep submicron CMOS technologies. Since 2001 he is also Professor at the KU Leuven.
He has made contributions to the fields of non-volatile semiconductor memory devices and technology, reliability physics of VLSI-technology, hot carrier effects in MOSFET's, time-dependent dielectric breakdown of oxides, ESD-protection and –testing, plasma processing induced damage, electrical characterization of semiconductors and characterization and reliability of high k dielectrics.
He has served as a technical program committee member of several international scientific conferences, among which the IEEE International Electron Device Meeting (IEDM), the International Reliability Physics Symposium (IRPS), the IEEE Semiconductor Interface Specialists Conference (SISC) and the EOS/ESD Symposium. From 2000 until 2002 he also acted as European Arrangements Chair of IEDM.
He has authored or co-authored more than 300 publications in international scientific journals and in international conference proceedings, 3 book chapters and 7 patents in his fields of expertise. Dr. Groeseneken is a senior member of IEEE.

Ann Kelleher

Ann Kelleher obtained the B.E., M.Eng.Sc. and Ph.D. degrees from University College Cork (UCC), Ireland in 1987, 1989 and 1993 respectively. She is an Engineering Manager in Intel Ireland where she has held a number of different engineering positions. For the 90nm technology transfer, Ann was Yield Manager with a primary focus on the technology start-up in the 300mm facility. Since June she has moved to manage the Process engineering Thin Films department. Previously, she was a senior research scientist at the National Microelectronics Research Centre, Ireland (NMRC) where she led a process development group working on a wide variety of technologies (MOS, sensors, power devices etc). Before joining NMRC she worked with IMEC in Belgium, and as part of the Ultra clean processing group she concentrated on ultra thin gate oxides. She has authored or co-authored 19 publications.

Technical Program Schedule

Tuesday, April 5

8:00 - 17:00 **Registration**
9:00 – 17:00 **Exhibition**

9:00 **Welcome to ICMTS 2005**
Willy Sansen, General Chairman
Ulrich Schaper, Technical Chairman

Session 1: CD Metrology

9:20 – 10:40
Co-Chairs: Michael Cresswell (Natl. Inst. Stds & Tech.)
Emilio Lora-Tamayo (University of Barcelona)

9:20 **Suspended Greek Cross Test Structures for Measuring the Sheet Resistance of Non-Standard Cleanroom Materials**
1.1 *S. Enderling, M.H. Dicks, J.T.M. Stevenson, A.W.S. Ross, S. Smith and A.J. Walton, Scottish Microelectronics Centre, University of Edinburgh*

A novel method is reported to measure the sheet resistance of CMOS incompatible layers using a suspended polysilicon Greek cross test structures. To demonstrate the technique, gold (Au) was blanket evaporated onto the test structures and the sheet resistance extracted. A sheet resistance of 0.266W/sq was determined for a 0.1μm thick deposited Au film on Greek cross structures with arm widths ranging between 5 and 20μm demonstrating that the structures are full capable of measuring sheet resistance of blanket deposited films.

9:40 **Extraction of Critical Dimension Reference Feature CDs from New Test Structure Using HRTEM Imaging**
1.2 *Richard A. Allen, Amy Hunt, Christine E. Murabito, Brandon Park, William F. Guthrie, and Michael W. Cresswell, National Institute of Standards and Technology, Gaithersburg; Accurel Systems International Corp, Sunnyvale;*

NIST has an ongoing effort to provide the semiconductor industry with critical dimension CD reference materials, using the silicon (111) lattice spacing as the ruler to establish the linewidth. Recent developments include both a new test structure design as well as changes to the HRTEM sample preparation and fringe counting procedures. These changes are expected to contribute to an improvement over earlier work in which overall uncertainties of 10 nm - 15 nm were observed for approximately 100 nm wide features.

10:00 **Comparison of CD-Measurements Extracted from Test-Structure Features Having Linewidths in the Range 40 nm to 240 nm by Use of SEM and HRTEM Imaging**

1.3 *Brandon Park,1 Richard A. Allen, William F. Guthrie, Ronald G. Dixson, Christine E. Murabito, Michael W. Cresswell, National Institute of Standards and Technology, Gaithersburg, Maryland*

A comparison of CD measurements extracted from SEM and HRTEM images of each of the same set of mono-crystalline silicon features having linewidths between 40 and 200 nm has been made. The silicon features are incorporated into a new test structure which has been designed to facilitate this type of CD-metrology comparison. The original purpose of the work was to investigate of the absolute accuracy of SEM imaging.

10:20 **Improved Test Structures for the Electrical Measurement of Feature Size on an Alternating Aperture Phase-Shifting Mask**

1.4 *S. Smith, A.J. Walton, M. McCallum, A.C. Hourd, J.T.M. Stevenson, A.W.S. Ross and L. Jiang, Scottish Microelectronics Centre, The University of Edinburgh*

Electrical test structures have been designed that are compatible with a standard alternating phase shift mask manufacturing process. Measurements indicate that these have superior performance to previous designs with FA < 10% for Greek crosses. As a result the test structures extract a consistent sheet resistance and the measurements on linewidth structures have demonstrated an improved capability with the offset variability being halved.

10:40 – 11.00 **Exhibition Presentations**

11:00 – 11:30 Break

Session 2: Process Characterization

11:30 – 13:00

Co-Chairs: **Christopher Hess** (PDF Solutions)
Kelvin Yih-Yuh Doong (TSMC Co. Ltd)

11:30 **90nm CMOS Technology Characterization at Transfer and Ramp**
- invited talk -

2.1 *A. Kelleher, D. Gourley, A.M Holmes, T. Hepburn, C. Farrell, R. Groves, T. Taskin, J. McMillan, Intel Ireland, Leixlip, Co. Kildare, Ireland*

This paper will give an overview of the characterization requirements during the successful transfer and ramp of a high yielding 90nm CMOS technology. In particular, the different characterization phases will be examined and key aspects of achieving a high yielding technology during both transfer and ramp will be discussed.

12:00 **Test Structures for the Characterization of Deep Trench Isolation**

2.2 *Stefan Hausser, Remus Albu, Holger Schligtenhorst, Philips Semiconductors GmbH, Boeblingen*

Test structures are presented that allow the characterization of deep isolation trenches for their depth and for parasitic transistors that can occur in adjacent NMOS and PMOS devices. The trench depth can be correlated to the magnitude of reverse junction currents. Design options are explored that help to minimize the onset of currents in parasitic transistors.

12:20 **Design and characterization of a post-processed copper heat sink for smart power drivers**

2.3 *G. Van den Bosch[1], T. Webers[1], E. Driessens[1], B. Elattari[1], D. Wojciechowski[2], P. Gassot[2],P. Moens[2], G. Groeseneken[1]*
[1]: IMEC, Leuven, [2]: AMI Semiconductor Belgium

Heat sinks of various geometries have been post-processed by copper electroplating on top of large area power drivers to improve thermal management. The efficiency of the heat sink was quantified by energy capability (*EC*) measurements. Thermal as well as electro-thermal simulations backed up experimental results. A 25 mm thick copper layer improved *EC* with approx. 25%, translating into a driver area reduction by the same amount for *EC* critical applications.

12:40 **High Speed Test Structures for In-Line Process Monitoring and Model Calibration**

2.4 *Mark Ketchen, Manjul Bhushan, and Dale Pearson, IBM Research Division, Yorktown Heights*

The use of in-line test structures for routinely monitoring various high frequency aspects of the performance of CMOS gates is described. These compact test structures use dc I/O's and are compatible with standard parametric testers. The specific examples described are ring oscillators for a wide range of self-consistent parameter extraction ranging from circuit delays to gate length and leakage components; and self-timed/calibrated measurements of SOI switching history effects utilizing ~ 100ps self-generated pulses.

13:00 – 14:20 Lunch

Session 3: Device Characterization

14:20 – 16:00
Co-Chairs: **Yoshiaki Hagiwara** (Sony Corp.)
Kevin McCarthy (University College Cork)

14:20 **Study of 90nm MOSFET Subthreshold Hump Characteristics Using Newly Developed MOSFET Array Test Structure**
3.1 *Mizumura, T.Ohishi, N.Yokoyama*, M.Nonaka*, S.Tanaka*, and H.Ammo, Sony Corp.*

90nm MOSFET subthreshold hump characteristics are reported for the first time by using a newly developed MOSFET array test structure, which is a new layout pattern, in order to eliminate the contribution of gate leakage on measured MOSFET parameter data such as Vth, Ioff, subthreshold-slope et al. A single MOSFET has low sensitivity in monitoring subthreshold hump distribution in a wafer. It is confirmed that subthreshold hump occurs at random in an array. By extracting the hump variation, it is possible to estimate accurately and reduce the standby-current in logic LSI chips.

14:40 **Impact of Mask Alignment on the Tunneling Field Effect Transistor (TFET)**
3.2 *Th. Nirschl[1, 2], U. Schaper[2], J. Einfeld[2], St. Henzler[1, 2], M. Sterkel[1], J. Singer[2], M. Fulde[1], W. Hansch[1], G. Georgakos[2], D. Schmitt-Landsiedel[1],*
[1]: Techn. Univ. Munich, [2]: Infineon Technologies AG

The Tunneling Field Effect Transistor (TFET) is a quantum-mechanical device which is fabricated using the standard CMOS process flow. The tunneling junction is built by shifting the p-implant mask over the source region. To guarantee the complete doping of the source extension the p-implant mask is shifted over the gate. The channel region is protected by the gate stack. To investigate the impact of the alignment of the p-implant mask on the TFET performance a new test structure is presented. The test macro is fabricated using the 130nm technology.

15:00 **A Test Structure for spatial analysis of Hot-Carrier-Induced Photoemission in n-MOSFETs**
3.3 *T. Matsuda[1], T. Tanaka[1], H. Iwata[1], T. Ohzone[2], K. Yamashita[3], N. Koike[3] and K. Tatsuuma[3]; [1]: Toyama Prefectural Univ., [2]: Okayama Prefectural Univ., [3]: ULSI Center, Matsushita*

As the channel length of MOSFETs has been scaled down to deep submicron level, hot-carrier effects have become one of the most important problems affecting reliability. Since the hot carriers emit photons, measurements and analyses using a photoemission microscope become useful to study the high electric fields in MOSFETs[1-5]. Two-dimensional photoemission analyses are useful to study the emission mechanism as well as detailed high-electric-field

effects in MOSFETs. A test structure to determine the location of photoemission peak more precisely has been reported[2] In this paper, a spatial analysis of hot-carrier-induced photoemission is discussed. A method to measure the precise peak position of photoemission intensity from the center of MOSFET.s gate is presented as well as the photoemission profiles along the gate width direction.

15:20 **A self heating test structure using poly resistors and P+/N diodes to characterize anomalous charge transfers in embedded flash memories.**

3.4 *Pascal Mora, Patrice Waltz, Sophie Renard, Philippe Candelier, STMicroelectronics*

We report on the characterization of a self heating test structure which allows the monitoring of charge loss or gain of embedded flash memories with a high level of time accuracy. A calibration of the test structure has been successfully performed between 25°C and 300°C. Furthermore, voltage and current operating points were determined in order to obtain the self heating structure temperature profile needed for charge transfer studies.

15:40 **Test Structure for Performance Evaluation of 3 Dimensional FinFETs**

3.5 *Young Joon Ahn, Hye Jin Cho, Hee Soo Kang, Choong-ho Lee, Chul Lee, Jae-man Yoon, Tae Yong Kim, Eun Suk Cho, Suk-Kang Sung, Donggun Park, Kinam Kim and Byung-Il Ryu, Samsung*

The 3D MOSFETs have been recognized as the main technology to substitute planar MOSFET beyond 50nm. The development of various test structures is required to evaluate the characteristics of the new dimension. The FinFETs having 0, 45° rotated active directions from flat zone were evaluated, because those are critical for Si orientation of surface channel on the fin. In this paper, the performance and the reliability evaluation of 3D FinFET were performed by using two different test structures. The body tied FinFETs [1] having two different rotation angles _=0, 45° were designed. The "_" indicates the rotation angle of channel direction of the FinFET to the <110> flat zone. The electrical characteristics and reliability of the FinFET _(45°) were measured and compared to those of the FinFET _(0°).

16:00 – 16:30 Break

Session 4: Parameter Extraction

16:30 – 17:30

Co-Chairs: Colin McAndrew (Freescale Semiconductor Inc.)
Ulrich Schaper (Infineon Technologies AG)

16:30 **A Test Structure to Measure Sheet Resistances of Highly-Doped-Drain and Lightly-Doped-Drain in CMOSFET**

4.1 *T. Ohzone[1], K. Okada[1], T. Morishita[1], K. Komoku[1], T. Matsuda[2] and H. Iwata[2]; [1]: Okayama Prefectural Univ., [2]: Toyama Prefectural Univ.*

A test structure to separately measure sheet resistances R of highly-doped-drain (HDD) and lightly-doped-drain (LDD) in LDD-type CMOSFETs with various source/drain widths W having sub 100 nm spacer was proposed. The measured gate bias dependences of R-1 versus W characteristics depart from those expected for the ideal fabrication process, which suggests that the micro-loading effects on LDD spacer in the narrower W regions seriously affect on the R increase.

16:50 **New extraction method for gate bias dependent series resistance in nanometric double gate transistors**

4.2 *Antoine Cros, Samuel Harrison, Robin Cerutti, Philippe Coronel, Gerard Ghibaudo, Hugues Brut, STMicroelectronics*

Double gate type devices are needed for the ultimate integration on silicon, and thus extraction techniques have to be adapted. In this paper, the influence of the series resistance on the extrinsic mobility reduction parameters is analysed, in case of resistance varying with gate bias. It is evidenced that both the low field and high field parameters are impacted. Then, a new approach is proposed for the extraction of the series resistance, and applied to the analysis of gate-all-around transistors series resistance, with doped and undoped body.

17:10 **An Improved LDMOS Transistor Model That Accurately Predicts Capacitance for all Bias Conditions**

4.3 *S.F. Frère[1, 2], P. Moens[1], B. Desoete[1], D. Wojciechowski[1], A.J. Walton[2]*
[1]: AMI Semiconductor Belgium, [2]: University of Edinburgh

This paper proposes a significantly improved SPICE macro model for the LDMOS device. It performs significantly better than existing models in both DC and AC regimes and because it has been implemented using standard elements and Verilog-A modules, it is also simulator independent.

Wednesday, April 6

8:30 - 17:00 **Registration**
9:00 – 17:00 **Exhibition**

Session 5: Reliability

9:00 – 10:30
Co-Chairs: Robert Ashton (White Mountain Labs)
Yoshio Mita (University of Tokyo)

9:00 **Recent trends in reliability assessment of advanced CMOS technologies - invited talk -**
5.1 *Guido Groeseneken, IMEC – KU Leuven*

With the ultimate scaling of CMOS technologies, the reliability assessment of these technologies becomes more and more difficult due to a number of factors. First of all, the failures, such as electromigration failures or oxide breakdown failures, do not manifest themselves any longer as a sudden or abrupt change in a certain monitor parameter, such as line resistance or gate leakage current. Instead the failures become more and more gradual by which it becomes difficult to define an exact failure criterion. Moreover, the statistics of the failures are also changing dramatically, especially in the case of oxide breakdown, which has tremendous impact on the lifetime predictions. In the past the reliability specifications were based on a number of accelerated tests on isolated teststructures, from which a prediction of the lifetime was based using statistical extrapolations and accelerated stress models. In this approach it was always assumed that the first failure will cause the full circuit to fail. When applying this methodology to the most advanced technologies, the lifetime of the devices for some failure mechanisms, such as e.g. oxide breakdown, can no longer be guaranteed and the reliability margin is reduced to zero. As a result, research is going on to find new reliability margin by taking into account the gradual degradation of the devices, by investigating the impact of a failure on both the device characteristics and the circuit operation and by adopting new assumptions concerning the conditions of circuit failure.
Based on a case study carried out for oxide breakdown, it will be demonstrated that future reliability assessment and assurance will have to rely on interaction between designers and technology engineers.

9:30 **Assessment of a 90nm PMOS NBTI in the form of Products Failure Rate**
5.2 *Hiroo Masuda, Donald G. Pierce*, and Kazunori Nishitsuru** STARC, *Sandia Technologies, **Agilent Technologies*

Critical assessment of PMOS NBTI in a 90nm process is presented. NBTI will be the most critical MOS reliability issue for ppb-level product failures in Giga-transistor integrated systems. The product level failure rate is estimated at about

100 FIT @ worst case environmental conditions of 150C and +10% Vdd. However, 1 FIT level can be achieved at a limited temperature range of < 80C. Degradation during Burn-in Test is less important since the failure-rate saturates for long stress times.

9:50 **Multi-purpose EM test structure with electrical verification of the failure spot demonstrated using SWEAT for fast Wafer Level Reliability Monitoring**
5.3 *Andreas Pietsch, Andreas Martin, Josef Fazekas, Infineon Technologies*

A multipurpose electromigration test structure designed for advanced fast Wafer Level Reliability tests is described in this work. It is shown that different failure location and failure modes can be detected electrically by this test structures which is beneficial for early technology development. Furthermore, the ability to test different electromigration test modes (upstream, downstream) is possible using one test structure. The presented experimental data focuses on the investigation of different process splits.

10:10 **Accelerated life time estimation of electrostatic microactuators**
5.4 *B. Caillard, Y. Mita, Y. Fukuta, T. Shibata, H. Fujita, University Tokyo*

There is an absolute need of accelerated life time measurement for MEMS actuators. In this paper, a simple method is proposed. It relies on very low frequency electrical detection of the failures and on high voltage testing, since a relationship between mean time before failure and driving voltage is proved. A time gain factor of 10 is reached with test structures used in real applications.

10:30 – 11:00 Break

Session 6: RF test structures

11: 00 – 12:40
Co-Chairs: Juriaan Schmitz (University of Twente)
Franz Sischka (Agilent Technologies Germany)

11:00 **On-wafer radiation pattern measurements of integrated antennas on standard BiCMOS and Glass processes for 40-80 GHz applications**
6.1 *Noel Segura, Sebastien Montusclat, Christian Person, Smail Tedjini, Daniel Gloria, STMicroelectronics, Crolles*

Integrated antennas on-wafer measurements achieved on standard STMicro-electronics BiCMOS and Glass processes are presented for applications between 40 and 80 GHz. Radiation pattern and S-parameter measurements of a dipole and a patch antenna are described. For the first time, measure- ments of integrated millimeterwave antennas are shown at these frequencies. A complete test bench has been realized. In addition, associated wideband High Frequency model is described.

11:20 **Simple Expressions for Substrate Network of Accurate On-Chip Inductor Model**

6.2 *Ivan C. H. Lai, Minoru Fujishima, University of Tokyo*

This paper provides a practical implementation of an improved, yet simple inductor model that includes a substrate network. This implementation involves using simple, accurate expressions to determine this network. The accuracy of the model with these equations had been verified with standard CMOS 0.35μm and SOI 0.15μm processes. It is also demonstrated how this approach is superior in a circuit design example.

11:40 **Verification of Layout Efficient Shield-Based De-Embedding Techniques for On-Wafer HBT Characterisation up to 30 GHz**

6.3 *John A. O'Sullivan, Kevin G. McCarthy and Patrick J. Murphy, University College Cork, Aidan C. Murphy, Freescale Semiconductor, Cork*

On-wafer measurements play a vital role in device characterization and modelling for advanced high speed devices such as SiGe HBT's and submicron MOSFET's. Unfortunately, due to the lossy nature of Si substrates, extensive, area hungry, deembedding structures are necessary to separate out the intrinsic device characteristics from the extrinsic parasitics. It has been postulated, [1], that the use of shield-based structures may lead to a reduction in the layout-area requirements for de-embedding structures. In this work, we show for the first time that shielding techniques do indeed provide an area saving as high as 40% for the HBT process considered here.

12:00 **Characterization and Model of On-Chip Flicker Noise With Deep-Nwell (DNW) Isolation for 130nm and Beyond SOC**

6.4 *M. T. Yang, Darryl C. W. Kuo, C. W. Kuo, Y. J. Wang, Patricia P. C. Ho, T. J. Yeh, Sally Liu, TSMC, Hsinchu*

An investigation of the Flicker noise by exploring 0.13μm and beyond MS/RF CMOS technology was carried out for wireless system-on-a-chip (SOC) applications. On-chip flicker noise of various components are characterized and accurately modeled. Feasibility of deep N-well isolation to suppress substrate coupling of analog nodes from digital clock noise is also demonstrated.

12:20 **Substrate Isolation Study in 0.18um CMOS Technology**

6.5 *G. Ali Rezvani and Jon Tao, RF Micro Devices, San Jose*

Various methods of substrate Isolation in a typical 0.18um CMOS process technology with and without Deep Nwell (DNW) have been studied. Results are presented on the impact of guard ring, substrate contact size and proximity, DNW at various biases. |S21| is used as a measure of isolation. N+ to Psub junction diode is used as both the source of noise injected into the substrate and as the sensor for noise pick up. It is shown that isolation based on DNW works

well up to several Gigahertz, but at higher frequencies the impact of P+ guard ring and DNW are about the same in reducing the substrate coupling.

12:40 – 14:00 Lunch

14:00 **Announcement of ICMTS 2006**

Session 7: Matching

14:10 – 15:50
Co-Chairs: Hans P. Tuinhout (Philips Research, Eindhoven)
Mark Poulter (National Semiconductor Corp.)

14:10 **MOSFET matching improvement in 65nm technology providing gain on both analog and SRAM performances**
7.1 *R. Difrenza[1], K. Rochereau[2], T. Devoivre[1], B. Tavel[2], B. Duriez[2], D. Roy[1], S. Jullian[2], A. Dezzani[1], R. Boulestin[1], P.Stolk[2], M.Woo[3], F. Arnaud[1]*
[1]: STMicroelectronics, [2]: Philips Semiconductors, [3]: Freescale Semiconductor

The 65nm process has been optimized through thermal budget and implant of halo and LDD to reduce gate impact. It provides the best matching results ever reported to our knowledge, i.e. AVt of 2.1 and 1.9mV.μm for NMOS and PMOS respectively. We demonstrate that such results provide relevant circuit performance improvement. For SRAM, a gain of more than 50% has been achieved on cell read current going from 4 down to 2.1mV.μm. For analog applications significant improvement is pointed out in terms of linearity and resolution.

14:30 **Speed – Accuracy trade-off for measurement and characterization of the matching performance of SiGe:C HBTs, applied to a 200 GHz technology**
7.2 *L. J. Choi, R. Venegas and S. Decoutere, IMEC, Leuven*

In this paper, the trade-off between time and accuracy for measurement of the matching performance of bipolar transistors has been investigated. After determination of the limits of the hardware setup, the matching behavior of a 200 GHz SiGe:C HBT is characterized over a wide range of dimensions and biasing conditions. The focus is put on measurement in the low and high current region. It reveals the unique bias dependence of bipolar mismatch in the high current region.

14:50 **Design and implementation of an ultra high precision parametric mismatch measurement algorithm**
7.3 *T. Ewert[f], H.P. Tuinhout[ff], N.A.H. Wils[ff] and J. Olsson[f] ,*
[f]Uppsala University, [ff]Philips Research, Eindhoven

This paper describes a parametric mismatch characterisation approach that can assess statistical parametric mismatch fluctuation levels down to tens of ppm's.

This is almost two orders of magnitude better that any approach reported so far.

15:10 **Parameter Variation on Chip-Level**
7.4 *Ulrich Schaper, Jan Einfeld, Infineon Technologies AG, Munich*

Integrated MOSFET circuits fabricated in actual technologies are packed on several mm_ of chip area. Circuit building blocks distributed over a chip have to achieve the same specifications. The circuit features depend on device parameters which vary not only on a global scale (i.e. wafer scale) or on a local scale (i.e. close packed device pairs) but also on a chip level scale. A characterization concept for an intra-die-statistics is discussed which closes the gap between process control monitoring and matching characterization.

15:30 **A Simple and Accurate Capacitance Ratio Measurement Technique for Integrated Circuit Capacitor Arrays**
7.5 *Zhenqiu Ning, Luc De Schepper, Henri-Xavier Delecourt, Renaud Gillon, Marnix Tack, AMI Semiconductor Belgium*

The key performance of many analogue circuits is directly dependent on precise capacitance ratios. To perform an accurate characterization of non-unity capacitor ratios, a floating-gate AC nulling technique is proposed. A test-structure containing the floating-gate and a binary-weighted capacitor array has been designed, fabricated and tested in the AMIS C035 process. The technique is proven to be accurate, robust and easy to use.

15:50 – 16:20 Break

Session 8: Poster

16:20 – 18:00
Co-Chairs: Anthony J. Walton (University of Edinburgh)
Takashi Ohzone (Okayama Prefectural University)

16:20 **Short oral presentation**: 4 minutes (maximum) for each poster
17:00 **Poster Presentation**

8.1 **Physical Meaning of σ Value Estimated with V_{TH}-Mismatch Evaluation Circuit**
Kazuo Terada, Tomonari Yamauchi and Akihiko Ueki, Hiroshima City University

A new test chip is developed for clarifying the quantity corresponding to the standard deviation of the threshold voltage sigma which is extracted using the test circuit proposed in the previous ICMTS. Comparing sigma with the standard deviation calculated from the many data for the individual MOSFETs, it is considered that sigma is good approximation to the standard deviation of the threshold voltage.

8.2 **RF-ESD Design and Measurement of CMOS LNAs: a Comparison between Diode and Inductive Protection**
Paul Leroux and Michiel Steyaert, Katholieke Universiteit Leuven

This paper compares two types of ESD-protection suited for the protection of CMOS low-noise amplifiers. This comparison is illustrated with the design and measurement of two high performance LNA prototypes. The first amplifier with diode protection targets the GPS L1 band at 1.57 GHz. It features a very low noise figure of 1.3 dB and a gain of 16.5 dB. The second amplifier was designed for 5 GHz wireless LAN applications and uses inductive ESD-protection. This prototype has a power gain of 20 dB and a noise figure of 3.5 dB. Both amplifiers surpass the industrial 2 kV HBM specification.

8.3 **A novel test fixture with enhanced signal port isolation capability for on-wafer microwave measurements**
Tero Kaija and Eero O. Ristolainen, Tampere University

A novel test fixture for on-wafer microwave measurements is proposed in this study. It has an excellent isolation between signal ports. The proposed fixture has 15 dB and 30 dB lower forward coupling than commonly known shield-based and conventional fixture, respectively, at 20 GHz. This is validated by measurements. Reduction in the die space utilization and reliable open in-fixture performance in dummy de-embedding can be achieved by using the proposed test fixture. The fixtures were fabricated using four metal layer 0.35μm CMOS technology.

8.4 **Mismatch characterisation of chip interconnect resistance**
Jurgen Deveugele, Libin Yao, Michiel Steyaert, Willy Sansen,
Katholieke Universiteit Leuven

Many analog circuits use matched resistors on chip. The resistors have two components: the resistive elements and the interconnects. The resistive elements have good matching properties. The resistance of the interconnects – especially of the contacts and vias – however is only guaranteed to be within certain wide limits. If the matched resistors are low-ohmic then the interconnect dominates the mismatch equations. This is often solved by oversizing the interconnect or by avoiding structures with lots of interconnect. We prefer to characterize these interconnects or even to build resistors only using interconnects. The measurement results show that the interconnect resistance can match as good as poly resistors in the same 0.18 _m technology.

8.5 **Novel Realistic Short Structure Construction for Parasitic Resistance De-embedding and on-Wafer Inductor Characterization**
Jon Tao, Paul Findley and G. Ali Rezvani, RF Micro Devices, San Jose

A novel method of using measured S-parameters of a THROUGH structure to construct the Z-parameters of a realistic SHORT structure is presented. By using

this REALISTIC_SHORT structure for parasitic resistance de-embedding, an on-wafer inductor has been characterized, and inductor parameters (Q, L and R) have been accurately extracted.

8.6 **Experimental analysis of a Ge-HfO2-TaN gate stack with a large amount of interface states**

J.A. Croon, B. Kaczer, G.S. Lujan, S. Kubicek, G. Groeseneken, M. Meuris, IMEC, Leuven

We characterize and discuss the quality of the Ge-HfO2 interface of early MOS capacitors. Whereas PMOS capacitors exhibit well-behaved CV characteristics, the CV behavior of NMOS samples is strongly distorted. This makes the interpretation of measured data very difficult and it explains the need to go beyond standard CV-analysis. Low temperature CV, gated diode measurements and conductance analysis are carried out and suggest that Fermi-level pinning prevents inversion for p-type and accumulation for n-type Ge substrates.

8.7 **A New Method for Precise Evaluation of Dynamic Recovery of Negative Bias Temperature Instability**

S. Aota[1], S. Fujii[2], Z. W. Jin[1], Y. Ito[3], K. Utsumi[1], E. Morifuji[1], S. Yamada[1], F. Matsuoka[1], and T. Noguchi[1]
[1]: Toshiba Corporation, [2]: Agilent Technologies, [3]: Toshiba Microelectronics

Owing to the dynamic recovery of Negative Bias Temperature Instability (NBTI) after stress is removed, the precise time dependence of stress application and drain current (Id) measurement must be known beforehand for the instrument on which a NBTI experiment is conducted. This work presents a new characterization method to quantitate the dynamic recovery and, a general procedure for the evaluation of the NBTI degradation effects is proposed based on the results by the method.

8.8 **RF Monitoring test structure for Advanced RF Technologies working up to 100GHz with less than 80um width**

André Perrotin, Daniel Gloria, ST Microelectronics, Crolles

A new RF test structure for monitoring of Advanced Silicon Technologies and compatible with reduced scribe line dimensions (below 100um width) is presented. All DC and RF obtained results are compared with extraction on classical structures and are in good agreement up to 100GHz. This new layout approach can be extended to device RF matching parameters such as Ft mismatch monitoring.

8.9 **Measurement of Inner-chip Variation and Signal Integrity by a 90-nm Large-scale TEG**

Masaharu Yamamoto, Yayoi Hayasi† ,Hitoshi Endo†, and Hiroo Masuda, STARC, †Hitachi ULSI Systems

The evaluation of inner-chip variation and signal integrity (SI) in optimal design techniques for System on Chip (SoC) physical design is becoming increasingly important for shrinking feature dimensions, increasing scale, and improving precision. We here report on the development of new techniques for measuring and evaluating inner-chip variation and SI by the same test structure, i.e., the same pattern within a 90-nm large-scale test element group (TEG).

19:00 **Banquet** in Faculty Club, Groot Begijnhof, Leuven

Thursday, April 7

8:30 - 11:00 **Registration**
9:00 – 12:00 **Exhibition**

Session 9: Capacitance

9:00 – 10:50
Co-Chairs: **Satoshi Habu** (Agilent Technologies Japan Ltd)
Gregory Yeric (TestChip Technologies Inc.)

9:00 **Capacitance Characterization in Integrated Circuit Development: The Intimate Relationship of Test Structure Design, Equivalent Circuit, and Measurement Methodology**
- invited talk -
9.1 *George A. Brown, International SEMATECH, Inc.*

This paper, intended as an introduction to the capacitance test structure session, traces the historical and continuing relationship between integrated circuit device and material properties, capacitance test structure design, and measurement methodology. The key premise is that test structure design should provide a structure with an equivalent circuit matching that used for measurement and data analysis. Additional material introducing topics of papers accepted for the session will be included.

9:30
9.2 **A Novel Mobility-Variation-Free Extraction Technique of Capacitance Coupling Coefficient for Stacked Flash Memory Cell**
Okagaki Takeshi, Renesas

We propose a novel extraction technique of control gate capacitance coupling coefficient alpha g for stacked gate ash memory cell. Five novel test patterns are developed to directly measure all the capacitances connected to the floating gate. Comparison of extracted alpha g with TCAD result proves the validity of this technique. Moreover, we confirmed that conventional techniques, which use channel current characteristics, overestimate the alpha g variation due to channel

mobility variation. Therefore direct alpha g extraction using our proposed technique is necessary for precise process monitoring.

9:50 **EOT Measurements for Ultra-Thin Gate Dielectrics using LC Resonance Circuit**

9.3 *A. Teramoto, M. Komura, R. Kuroda, K. Watanabe, S. Sugawa, and T. Ohmi, Tohoku University, Sendai*

The EOT measurement method using by the LC Resonance Circuit (LC resonance method) for the thin gate dielectrics having large leakage current is demonstrated. In the LC resonance method, only an external inductance and a resistance and a simple equivalent electrical circuit of MOS devices are employed. The EOT value from thicker gate dielectrics (~10 nm) to thinner gate dielectrics (~1 nm) with large leakage current can be defined by the impedance – frequency characteristics at the resonance and be verified at other frequency region and DC gate current –gate voltage characteristics.

10:10 **Charge Pumping at Radio Frequencies**

9.4 *G.T. Sasse, J. Schmitz, University of Twente*

In this work for the first time charge pump measurements are obtained using gate signal frequencies in the GHz range. Measurement results show that the tunnelling component of the charge pump current on leaky oxides is minimized. A comparison of the obtained characteristics at low frequencies to the RF charge pump measurements indicate that the new method is indeed suitable for measuring the charge pump current in an accurate way.

10:30 **A Novel CBCM Method Free from Charge Injection Induced Errors: Investigation into the Impact of Floating Dummy-Fills on Interconnect Capacitance**

9.5 *Y.W. Chang, H.W. Chang, T.C. Lu, W. Ting, J. Ku and C.Y. Lu, Macronix, Hsinchu*

By CIEF CBCM, a novel CBCM method free from the errors induced by charge-injection, it is the first time to investigate into the impact of floating dummy-fills on interconnect capacitance in practice. The impact of floating dummy-fills is confirmed to play an important role on successful circuit design. Besides, a guideline to optimize the chip performance and minimize the crosstalk by dummy pattern design is also proposed in this paper.

10:50 – 11:20 Break

Session 10: Interconnect

11:20 – 12:40

Co-Chairs: **Bill Verzi** (Agilent Technologies, Austin)
Naoki Kasai (NEC Electronics Corporation)

11:20 **Extraction of Time Dependent Data from Time Domain Reflection Transmission Line Pulse Measurements**

10.1 *Robert A. Ashton, White Mountain Labs, Phoenix*

Transmission Line Pulse (TLP) measurements are an important tool in ESD protection design. The traditional TLP I-V curve only delivers part of the information available. This paper discusses the extraction of V(t) and I(t) data from each pulse in a Time Domain Reflection TLP system.

11:40 **A failure analysis test chip for deep sub-micron CMOS copper interconnect technologies**

10.2 *A. Cabrini[1], D. Cantarelli[2], P. Cappelletti[2], R. Casiraghi[2], D. Iezzi[2], A. Maurelli[2], M. Pasotti[2], P.L. Rolandi[2] and G. Torelli[1]*
[1]: Univ. of Pavia, [2]: STMicroelectronics

This paper presents a test chip that has been conceived to carry out all the measurements needed to evaluate the performance and the reliability of interconnects. In addition to allowing the simple fault detection (as in the case of conventional test structures such as interconnect chains), the proposed architecture makes it possible to identify the physical location of failed interconnects, as it is mandatory for a subsequent physical failure analysis and, moreover, to detect resistive C/V (that conventional test structures do not allow or, at least, allow without sufficient sensitivity).

12:00 **Test Chip for Inductance Characterization and Modeling for sub-100nm X Architecture and Manhattan Chip Design**

10.3 *N.D. Arora , L. Song, S. Shah, A. Sinha and V. Chang Cadence Design Systems , San Jose,TSMC, Hsin Chu*

This paper deals with the measurement and modeling of on-chip interconnect inductance in a VLSI chip fabricated using sub-100nm copper (Cu) CMOS process. A test chip was designed and fabricated in 90nm process node , to study the inductive effects, with various inductive return paths, including substrate, co-planar structures, power grids, and random structures. Inductive effects for Cu interconnects are then compared with previous studied on Aluminum (Al) interconnect at 130nm, followed by the discussion on the significance of inductance effect in sub-100nm X architecture chip design. Finally, inductance modeling and simulation results are presented are presented.

12:20 **New Applications of Cross-Talk -Based Capacitance Measurements**
10.4 *L. Vendrame, L. Bortesi, STMicroelectronics, A. Bogliolo, Università di Urbino*

Charge-based capacitance measurements (CBCMs) are widely used to estimate on-chip wiring capacitances because of their accuracy and simplicity. Enhanced CMOS transducers for CBCM have been recently proposed that exploit cross-talk to selectively measure cross-coupling capacitances. In this paper we propose two new applications of cross-talk-based capacitance measurements: mismatch measurement of stacked metal-metal capacitor pairs, and localization of wire interruptions. We present the measurement techniques, we discuss their implementation and we report preliminary experimental results.

12:00 **End of Exhibition**
12:40 **Best Paper Announcement**
12:50 **Closing Remarks**
13:00 **End of Conference**

14:00 -19:00 Excursion

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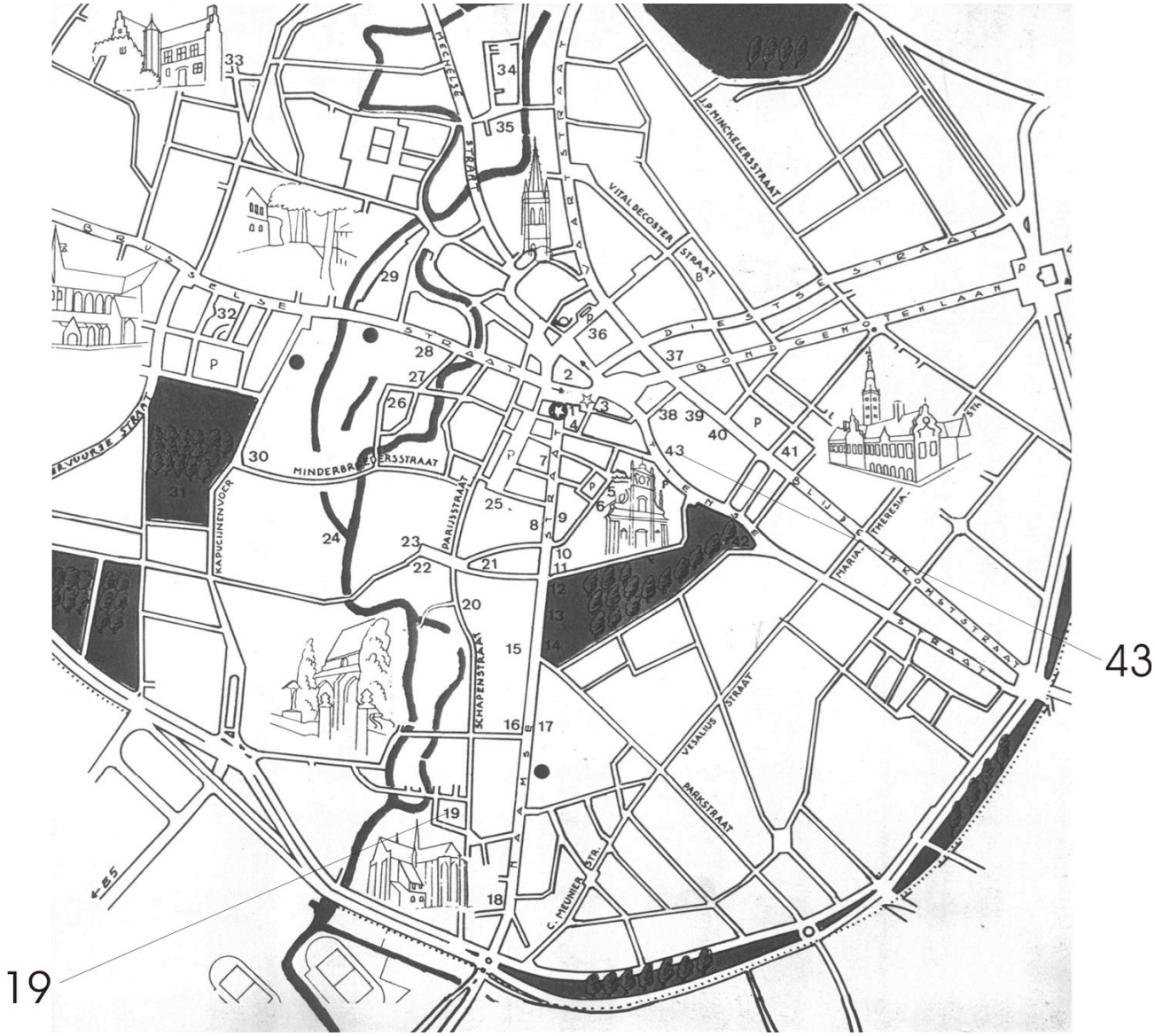
Map of Conference Site



no. 43 : De Valk : conference location (Falcon College)
no. 19 : Het Groot Begijnhof Leuven (Great Beguinage)
Banquet will be held in Faculty Club, Groot Begijnhof, Leuven.

ICMTS 2005 CONDENSED PROGRAM

Monday, April 4

8:00	Registration
9:00	Introduction
9:05	Fundamentals
9:55	Introduction to MEMs
10:25	Break
10:55	Oxide Breakdown
11:35	BEOL Reliability
12:15	Lunch
13:40	Low Frequency Noise
14:30	RF Characterization
15:20	Break
15.50	Modeling RF CMOS
16:40	MOSFET Matching
17:30	Wrap-Up, Conclusion
18:00	Reception

Tuesday, April 5

8:00	Registration
9:00	Conference Opening
9:20	Session 1
	CD Metrology
10:40	Exhibition Presentation
11:00	Break
11:30	Session 2
	Process Characterization
13:00	Lunch
14.20	Session 3
	Device Characterization
16:00	Break
16:30	Session 4
	Parameter Extraction

Wednesday, April 6

8:30	Registration
9:00	Session 5
	Reliability
10:30	Break
11:00	Session 6
	RF
12:40	Lunch
14.00	ICMTS 2006
14:10	Session 7
	Matching
15:50	Break
16:20	Session 8
16:20	Oral Introduction
16:40	Poster
19:00	Banquet

Thursday, April 7

8:30	Registration
9:00	Session 9
	Capacitance
10:50	Break
11:20	Session 10
	Interconnect
12:00	End of Exhibition
12:40	Best Paper Announcement
12:50	Closing Remarks
13:00	End of Conference
14:00	Excursion