ICMTS2004

http//:www.see.ed.ac.uk/ICMTS/

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ICMTS 2004 CONDENSED PROGRAM

GENERAL INFORMATION

Conference Information

The IEEE Electron Devices Society and Association for Promotion of Electrical, Electronic and Information Engineering are sponsoring the 2004 International Conference on Microelectronic Test Structures to be held in cooperation with The Institute of Electronics, Information and Communication Engineers (IEICE), and The Japan Society of Applied Physics (JSAP). The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The Conference will be preceded by a one-day Tutorial Short Course on Microelectronic Test Structures.

ICMTS 2004

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Presentation

The official language of the conference is English and it will be used for all presentations, printed materials. Only a data projector connected to a laptop PC will be available for your presentation of ICMTS 2004. We prefer the usage of the data projector and suggest using your own PC for the presentation to avoid some troubles. We will prepare a laptop PC and accept presentations as **PDF files or MS Power Point files** only, if you send it to the ICMTS secretariat until **March 12**, 2004 by e-mail. Please **bring backup file in CD-ROM, USB memory stick or floppy disk of your presentation**, in case something accidentally does not work on the data projector as expected. There will be no slide projector available. All speakers are requested to report to the speaker's registration desk located in front of the conference room before their presentation.

Best Paper Award

One paper presented will be selected for the Best Paper Award. Presentation of the award will be made at the ICMTS 2005.

Conference Proceedings

The IEEE ICMTS 2004 will publish proceedings. One copy of the proceedings is included in the registration fee. Additional copies will be available at the Conference for 5,000yen per copy for members of the IEEE or IEICE or JSAP, 7,000yen per copy for non-members, or from the IEEE after the conference.

Registration

Please visit the ICMTS website (http://www.see.ed.ac.uk/ICMTS/) to download the registration form, fill in the form and send it to ICMTS2004 Secretariat by FAX or postal-mail.

ICMTS 2004 Secretariat

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E-mail : icmts2004@bcasj.or.jp

Conference registration fees

Below are the conference fees for early, late, and on-site registrants.

	Member*	Non Member	Student**
Early Registration:(Registered by January 31, 2004)			
Tutorial	¥ 18,000	¥ 21,000	¥ 8,000
Technical Sessions	¥ 35,000	¥ 43,000	¥ 25,000
Late Registration:(Registered after February 1, 2004)			
Tutorial	¥ 25,000	¥ 28,000	¥ 10,000
Technical Sessions	¥ 38,000	¥ 46,000	¥ 26,000
On-site Registration:(Registration at the Conference)			
Tutorial	¥ 31,000	¥ 34,000	¥ 13,000
Technical Sessions	¥ 40,000	¥ 48,000	¥ 28,000

* Must be a member of the IEEE or IEICE or JSAP.

**To qualify for reduced conference rates, you must be a Student Member, a full time student, not be self-employed, nor working part or full time at a facility or corporation.

Registration fees include admittance to technical sessions, equipment exhibits, morning and afternoon coffee breaks, reception, conference banquet, one copy of the proceedings.

On-site registration schedule

On-site registration for the conference will be conducted at the Registration Counter (2nd floor) at Awaji Yumebutai International Conference Center as follows:

Monday,	March 22	8:00-19:00
Tuesday,	March 23	8:00-17:00
Wednesday,	March 24	8:30-16:00
Thursday,	March 25	8:30-11:00

Payment of the registration fees

Registration fees should be payable to the IEEE ICMTS 2004 and must be in **Japanese Yen only.**

(1) Bank Transfer in Yen to "IEEE ICMTS 2004". Account at the Tokyo Mitsubishi Bank. Esaka Branch A/C No. 1061511

(2) Bank Check in Yen payable to the order of "IEEE ICMTS 2004". Personal Checks are not acceptable.

(3) Credit Card in Yen: Master Card, VISA, Diner's Club, American Express*

(4) Cash in Yen at the conference regisrtation desk.

*For credit card payments of registration fees, add 5% to the registration fee for handling charges.

Cancellation

Due to advance financial commitments, refunds of registration fees requested after March 1, 2004, cannot be guaranteed. 5,000yen processing fee will be withheld from all refunds. Requests for refunds of registrations cancelled after March 1 will be considered after the conference.

Messages

If you need to be contacted during the Conference Sessions, a message can be left at +81-799-74-1020 (Ext. ICMTS Secretariat) between the hours of 9:00am and 5:00pm, March 22, 23, 24, and from 9:00 to 12:00pm on March 25. Messages will be placed on a Message Board beside the registration desk.

Banquet

The conference banquet will be held on Wednesday evening, March 24 at 18:30 at The Miracle Planet Museum of Plants (Awaji Yumebutai). Conference registration fees include one banquet ticket. Guest ticket will be available for sale at the registration desk.

Excursion

We have arranged Excursion on Thursday, 25 March.
Visit “Uzu-no-michi” (path of whirlpool) , where allows you to take a spectacular view of the whirlpools through the glassed floor above the sea, the Awaji Joruri Puppet Theater, and the Japanese Sake Brewery, “Sen-nen ichi”.

Time: 12:30-18:00
Fare: 4,000yen/person (Admission tickets and Lunch box are included)

Tea-ceremony

Awaji Yumebutai Internationl Conference Center has a modern, wonderful tea ceremony house, being in the bamboo grove in the midst of the deep forest, you feel as if you were in an isolated world.
Experience one of the most popular cultures of Japanese traditions.

Tuesday, March 23 12:30-14:30 / Tea-ceremony house Room A (4F)
* limited for the first 60 persons.

Awaji Information

Awaji Island is almost at the center of Japan’s archipelago, and is close to Kobe, Osaka and Kyoto. The largest island in the Inland Sea of Japan.
It is connected with the mainland (Honshu) by the Akashi Kaikyo Bridge, the largest suspension bridge in the world.
It is about 90 minutes from Kansai International Airport by the Hanshin Expressway Wangan Route and Akashi Kaikyo Bridge and 5 hours from Tokyo by Bullet Train and bus.

Climate and Clothing

The temperature in Awaji during the conference period will range between 8˚C(46˚F) at night and 16˚C (64˚F) during the day. The weather is, however, often unpredictable during this season. The average humidity is 76%, so light clothing and a sweater or light coat is recommended. Conference Center is fully air-conditioned.

Hotel Accommodations

JTB Corp. (JTB) has been appointed as the Official Travel Agent for the Conference and will handle all related travel arrangements including hotel accommodation. Fill in the application form on the ICMTS website (http://www.see.ed.ac.uk/ICMTS/) and fax to JTB. Inquiries and applications concerning arrangements should be addressed to:

JTB Corp (JTB)
Event & Convention Sales Dept, Western Japan
Regional Headquarters Sakaisuji-Hommachi Bldg.
2-1-6 Hommachi, Chuo-ku
Osaka 541-0053, Japan
Tel: +81-6-6260-5060 Fax: +81-6-6260-5090
Email: itdw_ec1@kns.jtb.co.jp

JTB has reserved a sufficient number of rooms at the following hotels for Conference participants at special discount rates. Those persons who wish to apply for hotel reservation are requested to complete the enclosed application form, and send it to JTB not later than March 5, 2004 with the necessary deposit (10,000 yen per room).
Hotel assignment will be made on a first-come, first-served basis.
Daily room charges are as follows:

Class	Name of Hotel	Rate (per person)		Location
		Single	Twin	
A	The Westin Awaji Island	¥12,390	¥10,185	on site
B	Hotel Ebisu (*1)	¥ 6,300	¥ 5,775	10 min. by bus

Note: 1) Above rate includes service charge, tax, and breakfast.
2) The deposit of ¥10,000 will be deducted when settling the bill with the hotel.
3) If your desired hotel is already fully occupied, we will reserve for you another hotel instead.
4) (*1): Above rate includes service charge and tax, but not breakfast.

Cancellation

If you want to cancel your hotel, a written notification should be sent directly to JTB.
The deposit will be refunded, but the following cancellation fees will be charged depending on when the notification is received by JTB.

At least 9 days before the first night of stay .... ¥1,000 per room
8-2 days before .... 20% of the daily room charge (minimum : ¥2,000)
One day before .... 50% of the daily room charge
The same day, or no notice given .... 100% of the daily room charge

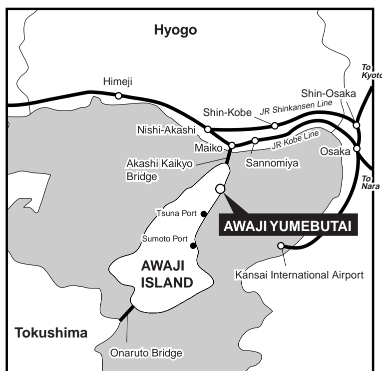
Equipment Exhibition

An equipment exhibition will be held besides the conference room during the Conference to display equipment closely paralleling the nature of this meeting. This equipment exhibition will permit one-on-one discussions between exhibitors and conference attendees on the latest test equipment. Exhibits will be open as follows.

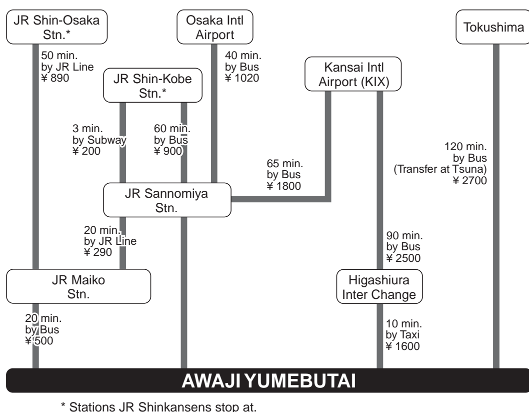
March 22	13:00 - 17:00
March 23, 24	9:00 - 17:00
March 25	9:00 - 12:00

The exhibitors list will be distributed on the day of the conference.

Where is Awaji Island



Access to Awaji Yumebutai International Conference Center



* Stations JR Shinkansens stop at.

From Kansai International Airport

By Limousine Bus:

Take a limousine bus for Higashiura I.C. (approx.90min.)
And take a taxi from Higashiura I.C. to Yumebutai (approx.10min.)
Services for Sannomiya Station are also available every 20 minutes from 6:30 to 23:30 (65min). At Sannomiya Station, take JR line to JR Maiko Station (20min) and a bus bound for Yumebutai (20min).

By train:

Take JR Line “Haruka” express to JR Shin-Osaka Station (45min). At Shin-Osaka station, transfer to JR “Kobe” line and get off at JR Maiko Station (50min). At JR Maiko Station, take a bus bound for Yumebutai (20min).

From JR Shin-Kobe Station

Take subway to JR Sannomiya Station (3min). At JR Sannomiya Station, take JR line to JR Maiko Station (20min) and a bus to Yumebutai(20min).
Also, limited number of buses direct to Yumebutai(via Sannomiya Station) are operated from JR Shin-Kobe Station.

CHAIRMAN'S LETTER

TUTORIAL and TECHNICAL PROGRAM

ICMTS 2004
CHAIRMAN'S LETTER

Dear Colleague,

On behalf of the committee, I welcome you to the 2004 International Conference on Microelectronic Test Structures (ICMTS 2004) in Awaji Yumebutai, Japan. This is the 17th ICMTS as an international conference and the 5th one to be held in Japan. The conference is sponsored by The IEEE Electron Devices Society, Association for Promotion of Electrical, Electronic and Information Engineering in cooperation with The Institute of Electronics, Information and Communication Engineers, and The Japan Society of Applied Physics.

The purpose of the conference is to bring together designers and users of test structures to discuss recent developments and future directions. This year's conference consists of 5 invited talks, and 53 papers in 9 oral sessions and 1 poster session.

Dr.Robert Ashton (White Mountain Lab, USA)'s invited talk will open Session 1 on "Reliability&System Integration", followed by Session 2 on "CD Measurement". Prof. Willy Sansen (KUL, Belgium)'s invited talk will open Session 3 on "RF", followed by Session4 "Interconnect". Prof. Steve Chung (NCTU,Taiwan)'s invited talk will open Session 5 on "Process Characterization", followed by Session 6 "Matching". Prof. Shinichi Takagi (Tokyo Univ.)'s invited talk will open Session 7 on "Device Characterization", followed by Session 8 with 23 Poster papers.

Prof.Mitiko Miura-Mattausch (Hiroshima Univ.)'s invited talk will open Session 9 on "Parameter Extraction", followed by Session 10 "Capacitance".

I am convinced that the test structures for new process, device and circuit developments become more and more important as the feature size is scaled down into deep submicron region. Test structures are essential for high frequency and precise digital/analog circuit design innovations. Furthermore, an advantage of test structures, which can provide the rapid transfer and quick yield improvements of new LSIs from R&D section to factories as well as between factories, becomes widely recognized. The well-designed test structures will also support the worldwide distribution of IP (Intellectual Properties) for SoC (System-on-a-Chip).

The one-day Tutorial Short Course will be held on March 22. The course is intended to provide the participants with a guideline on good design, test and analysis. The instructors have many years of experience in the field of test structures on CD-Measurements, TCAD, Parameter Extraction, SOI Devices, RF Measurements and Reliability Issues. Topics covered are:
Test Structure Fundamentals by Prof. A.J.Walton (Univ. of Edinburgh), Test Vehicle Design by Dr. K.Y.Doong (TSMC), Gate Capacitance Evaluation by Ms. M.Takayanagi (Toshiba), Yield&Variation by Dr. M.Aoki (STARC), Spice Modeling by Dr. C. McAndrew (Motorola), RF Modeling by Dr. K.McCarthy (Univ. of Cork), and Matching by Dr. H.Tuinhout (Philips Research).

There will be an equipment exhibition relating to the latest test structure measurements: measurement instruments, wafer probing equipment, computer software for data analysis, parameter extraction and measurement control.

The Conference will be held at the Awaji Yumebutai International Conference Center in Higashiura-cho, Tsuna-gun, Hyogo, Japan. The Awaji Island is directly connected to the city of Kobe by the Akashi Kaikyo Bridge.

I am sure that ICMTS 2004 in Awaji Yumebutai will give you excellent technical experience, cultivation of friendship with many engineers as well as understanding about Japanese cultures. We are looking forward to seeing you all in Awaji Yumebutai!

Sincerely,

Yoshiaki Hagiwara
General Chairman

TUTORIAL SHORT COURSE
Monday, March 22
Tutorial Program

8:00 Registration

9:00 **Introduction - Manabu Kojima, Fujitsu Ltd.**

9:05

1. Test Structure Fundamentals - Anthony J. Walton (University of Edinburgh)

This presentation will begin with a review of test chips briefly reviewing their history and their application. Measurement and equipment issues will be addressed focusing on procedures for obtaining accurate and repeatable measurements. The presentation will conclude with a brief review of test structures for measuring sheet resistance, line width and contact resistance.

9:55

2. Test Vehicle Design - Kelvin Yih-Yuh Doong (Taiwan Semiconductor Manufacturing Corp.)

As the requirement of functionality and application is getting complex, Logic-based technology could not only focus on a logic process but an application-oriented process such as embedded memory process. It changes the mask number of test vehicle from twenties, for using Al as interconnects, to fifties, for using Cu as interconnects. To fulfill the strict requirement of test vehicle design for process development, a test vehicle design methodology which is based on full-customized ASIC design flow is proposed. The tutorial will cover several parts of test vehicle design from

- The role of test vehicle in the process development and routine monitor cycle
- Front end of line (FEOL) test structure design
- Back end of line (BEOL) test structure design
- Design flow
- Floor planning of test vehicle
- Dummy feature insertion

In the 1st section, the role of test vehicle will be review at the various stages from the process development to the mass production. A brief introduction to the design of front and back end of line test structures will be presented. To accelerate the design cycle and maintain the consistency with a product design, a design flow and design tool will be review. To assemble the full chip of test vehicle, a practical case will be discussed to prevent the logistics error in the following mask process. Finally, in the sub wave-length process, a dummy feature insertion methodology will be presented.

10:45 Coffee Break

11:15

3. Characterization of Advanced Gate Dielectrics - Mariko Takayanagi (Toshiba Corp.)

Aggressive scaling of MOSFET devices result in the introduction of ultra-thin SiO_2 (SiON) or high-k materials, requiring new or improved techniques to characterize the properties of these gate dielectrics. This tutorial overview the issues of conventional measurements when applied to these advanced gate dielectrics and propose a new methods. It will cover C-V measurement, effective mobility extraction methods and measurements related to reliability issues and so on.

12:05 Lunch

13:30

4. Characterization of device variability in LSI chips - Masakazu Aoki (Tokyo University of Science), M. Yamamoto, H. Masuda (STARC)

Device variations in LSI chips have become one of the most serious issues in deep sub-micron LSI design and fabrication. Designers are faced with the degradation in timing margins in high-end processors, as well as the loss in voltage margins in low-power, low-voltage SoC's. Identification of defective failures in LSI products is also increasingly difficult. Thus, works are needed for characterizing the within-die variations, to provide appropriate guidelines to chip-designers and design tools, and also to identify major sources of yield loss efficiently. This tutorial explores test structures and methodologies to deal with the device variability in LSI chips.

14:20

5. Spice Modeling - Colin McAndrew (Motorola)

There are two major changes happening in SPICE models for present generation technologies, these are detailed in this Tutorial. First, the fundamental basis of MOSFET models is changing, from source-referenced threshold voltage based models, to inversion charge based models, to true surface potential based models. Details of these formulations will be presented, including the recent "symmetric linearization" technique, which is the most significant advance in MOSFET modeling in the past 20 years, as it results in an elegant, simple, and accurate model.

The continual decrease in device sizes has also led to a fundamental shift in the nature of statistical variations that affect device performance. The causes of this will be presented, and significant ramifications, such as the industry standard case file simulation approach no longer being reasonable, will be reviewed.

15:10 Coffee Break

15:40

6. RF CMOS Modelling - Kevin McCarthy (University College Cork), D.B.M. Klaassen, R. van Langevelde, A.J. Scholten and L.F. Tiemeijer (Philips Research)

As CMOS devices continue to scale the achievable cut-off frequencies have now reached over 100GHz for the most advanced devices indicating that CMOS technology has come of age for RF applications. One obstacle to the widespread use of CMOS technology for RF is that there hasn't yet been a widespread deployment of and familiarity with high-quality RF MOS models which are an essential design tool. This tutorial presents the background to modern high-quality RF models especially w.r.t. distortion and noise considerations. It begins by looking at the basic building blocks and equations of a MOS model and then shows how modern RF models are built from this basic framework. Measured data for advanced RF MOSFETs is shown together with model simulations to illustrate the high accuracy which can be achieved and to develop familiarity with the new generation of RF CMOS models.

16:30

7. Matching - Hans Tuinhout (Philips Research)

Parametric mismatch and fluctuations have received considerable attention in the recent parametric test literature and will no doubt continue to do so, as device scaling and mixed-signal requirements are increasing the demands for good understanding and control of parametric mismatch and fluctuations. This tutorial will discuss the main requirements and challenges of characterization of parametric mismatch fluctuations. After an introduction on terminology, mismatch effects, characterization techniques and test structure requirements, the two main test structure approaches will be discussed, namely the stand-alone matched pair and the addressable array. The merits of these two types will be compared in terms of test chip area and measurement time, versus accuracy, statistical uncertainty and characterization flexibility.

17:20 Wrap-Up and Conclusion

Welcome Reception

ICMTS 2004 Tutorial Lecturer Biography

Anthony J. Walton

Anthony J. Walton is professor of Microelectronic Manufacturing in the School of Engineering and Electronics at the University of Edinburgh. He has been actively involved with the semiconductor industry in a number of areas associated with silicon processing which includes both IC technology and micro-systems. For the 20 years he has had a direct interest in the design, fabrication and measurement of microelectronic test structures and has taken an active role in the organization of ICMTS.

He played a key role in setting up the Scottish Microelectronics Centre (SMC) which is a purpose built facility for R&D and company incubation consisting of approximately 300m^2 of class 10 clean rooms. He has published widely on test structures and is an associate editor of the IEEE Transactions on Semiconductor Manufacturing.

Kelvin Yih-Yuh Doong

Kelvin Yih-Yuh Doong was born in Kaoshiung, Taiwan, in 1968. He received B.S. degree from National Taiwan University, Taipei, Taiwan in 1990, and M.E. degree from Cornell University, Ithaca, New York in 1995, Ph.D. degree, National Tsing-Hua University in 2002, all in electrical engineering. He was a teaching assistant of the electrical engineering department of National Taiwan University from 1992 to 1993 and a research assistant of IAMS, Academia, Sinica from 1993 to 1994. He was a Rotary Ambassador Scholar from 1994 to 1995. He was an assistant manager of material analysis lab., quality engineering division of United Microelectronics Corp. (UMC) from 1995 to 1997. In 1998, he worked for a joint venture project between Toshiba Corp. and Worldwide Semiconductor Manufacturing Corp. (WSMC), where he was involved in developing test structure for process development and yield modeling. He jointed Alogic-1, Logic Technology Division, Taiwan Semiconductor Manufacturing Corp. (tsmc), Hsinchu, Taiwan, in July, 1999. He presently is a section manager, test vehicle project, R&D infrastructure program, and working on 65nm process test vehicle design and 90 nm yield improvement infrastructure program. He published more than 22 technical papers, holds 14 patents and 16 patents in pending. His research interests include sub-wave-length process integration, test vehicle design, and design for manufacturability.
He is a member of IEEE, EDS.

Mariko Takayanagi

Mariko Takayanagi received the B. A. degree in physics from International Christian University (ICU), Tokyo, Japan, in 1987.
She joined the Toshiba Research and Development Center, Kawasaki, Japan, in 1987, where she was engaged in the research on the characterization of the process and the electrical properties in Si MOS devices, including the carrier transport properties in doped poly-Si and the analysis of band-to-band tunneling current in MOSFET's. Since, 1991, she has been with SoC Research and Development Center, Semiconductor Company, Toshiba, in Yokohama, Japan, where she has been engaged in the research and development of advanced CMOSFET's. She is currently working on the physics and

technology of ultra-thin oxynitrides, high-k gate dielectrics, SiGe gate electrode and MOS (MIS) reliability issues.

Masakazu Aoki

Masakazu Aoki received the B.S. degree and the Ph.D. degree from the University of Tokyo, and the M.S. degree from the University of Michigan, Ann Arbor. From 1971 to 2000, he was with the Central Research Laboratory and later with the Semiconductor and IC Group, in Hitachi Ltd., where he was engaged in work on image sensors, high-density DRAM's and related low-voltage and low-power circuits. From 2001 to 2003, he was with Semiconductor Academic Research Center (STARC), Yokohama, where he worked on evaluation methodology for the within-die device variability. Currently, he is a professor of Electronic Systems Engineering at Tokyo University of Science, Suwa, in Nagano.

Colin McAndrew

Colin McAndrew received the Ph.D. and M.A.Sc. degrees in Systems Design Engineering from the University of Waterloo, Waterloo, Ontario, Canada, in 1984 and 1982 respectively, and the B.E. degree in Electrical Engineering from Monash University, Melbourne, Victoria, Australia, in 1978. Since 1995 he has been with Motorola, Tempe AZ, and is at present Director, Enabling Technology in the Analog-Mixed Signal Technology Center. From 1987 to 1995 he was at AT&T Bell Laboratories, Allentown PA. His work is primarily on compact and statistical modeling and characterization for circuit simulation.

Kevin McCarthy

Kevin McCarthy (MIEI, MIEEE) obtained the B.E., M.Eng.Sc. and Ph.D. degrees from University College Cork (UCC), Ireland in 1982, 1986 and 1992 respectively. He is a lecturer in the Department of Electrical and Electronic Engineering, UCC, where his main teaching and research interests are communications and microelectronic devices and circuits for communications, especially in the RF and mixed-signal area. Previously, he was a senior research scientist at the National Microelectronics Research Centre, Ireland (NMRC) where he worked on the simulation of advanced MOSFET and bipolar devices for digital and analog applications with emphasis on parameter extraction and statistical analysis methodologies. Before joining UCC/NMRC he worked with Analog Devices in product engineering and CAD engineering roles. Dr. McCarthy is a member of the ICMTS Technical Program Committee.

Hans Tuinhout

Hans Tuinhout received the M.Sc degree in electrical engineering from the Delft University of Technology (Delft, The Netherlands), in 1980. Since then he worked for the Philips Research Laboratories in Eindhoven, The Netherlands, on CMOS and BiCMOS process and device characterization. His current research activities, in the device modeling group at Philips Research, are focused on accurate DC parametric measurements for characterizing statistical differences between supposedly identical (matched) IC components and searching for techniques to interpret stochastic mismatch effects, to improve performance and yield of digital and mixed-signal integrated circuits.

TECHNICAL PROGRAM SCHEDULE

Tuesday, March 23

8:00 - 17:00 Registration

9:00 Opening Remarks
Yoshiaki Hagiwara, General Chairman
Naoki Kasai, Technical Program Chairman

SESSION 1: Reliability & System Integration

9:10 - 10:40
Co-Chairs: Junko Komori (Renesas Technology)
Akella Satya (KLA-TENCOR Corporation)

9:10 **Invited**
1.1 **Transmission Line Pulse Measurements: A Tool for Developing ESD Robust Integrated Circuits**
Robert Ashton (White Mountain Labs, USA)

Electrostatic discharge (ESD) is major reliability concern for semiconductors. The product qualification tests for ESD - human body model (HBM), machine model (MM), and charged device model (CDM) - are good predictors of susceptibility to ESD but they are not useful tools during the design of ESD protection circuits. Transmission line pulse (TLP) measurements have become an important tool in the design of on-chip protection. This paper will discuss ESD for semiconductor products, review the product qualification tests (HBM, MM, and CDM), and show how TLP measurements can be used to improve the design process for ESD on-chip protection.

9:40 **Characterization on ESD Devices with Test Structures in Silicon**
1.2 **Germanium RF BiCMOS Process**
*Ming-Dou Ker, Woei-Lin Wu, *Chyh-Yih Chang (National Chiao-Tung University, *Industrial Technology Research Institute, Taiwan)*

Different electrostatic discharge (ESD) devices in a 0.35-µm Silicon germanium (SiGe) RF BiCMOS process are characterized in high current regime by transmission line pulse (TLP) generator and ESD simulator for on-chip ESD protection design. The test structures of diodes with different p-n junctions and the silicon-germanium heterojunction bipolar transistors (HBTs) with different layout parameters have been drawn for investigating their ESD robustness. The human-body-model (HBM) ESD robustness of SiGe HBTs with low-voltage (LV), high-voltage (HV), and high-speed (HS) implantations has been measured and compared in details.

10:00 **Test Structures to Verify ESD Robustness of On-Glass Devices in**
1.3 **LTPS Technology**
*Ming-Dou Ker, Chih-Kang Deng, *Sheng-Chieh Yang and *Yaw-Ming Tasi (National Chiao-Tung University, * Toppoly Optoelectronics Corporation, Taiwan)*

Various types of test structures used to investigate the electrostatic discharge (ESD) robustness of on-glass devices in Low Temperature

Poly-Si (LTPS) process are proposed in this paper. The transmission line pulse generator (TLPG) is used to monitor the I-V behavior of on-glass devices in the high-current region during ESD stress condition, and to evaluate the ESD robustness of those LTPS devices. Finally, a successful ESD protection design with p-i-n diodes and VDD-to-VSS ESD clamp circuits integrated on a LCD panel have been demonstrated with a machine-model (MM) ESD level of up to 275V, whereas the traditional one can only sustain 100 V MM ESD stress.

10:20 **On-chip di/dt Detector Circuit for Power Supply Line**
1.4 *Toru Nakura, Makoto Ikeda and Kunihiro Asada (Univ. of Tokyo, Japan)*

This paper describes an on-chip *di/dt* detector circuit for power supply line. The *di/dt* detector consists of a spiral inductor under the power supply line and a noise-tolerant amplifier. The former induces *di/dt* proportional voltage by means of the mutual inductive coupling, and the latter amplifies the induced voltage linearly. Simulation results show that the detector can measure the *di/dt* with the accuracy of 1.52×10^7A/s. The current waveform can be obtained by integrating the *di/dt*, and the result shows 0.72mA accuracy at the average current of 50mA.

10:40 - 10:50 Exhibition Presentations

10:50 - 11:20 Break

SESSION 2: CD Metrology

11:20 - 12:20
Co-Chairs: Akio Kawamura (Sharp Corp.)
Loren Linholm

11:20 **Test structure for fixing OPC of 200 nm pitch via chain using inner**
2.1 **and outer dummy via array**
Takashi Nasuno, Yoshihisa Matsubara, Noboru Uchida, Hiromasa Kobayashi, Hisako Aoyama, Hiroshi Tsuda, Koichiro Tsujita, Wataru Wakamiya and Nobuyoshi Kobayashi (Selete Inc., Japan)

A new test structure for fixing OPC (Optical Proximity Correction) is proposed using inner and outer dummy patterns surrounding electrically connected 200nm pitch via chain array. Unconnected outer dummy via chain is designed as a protection dummy pattern for OPE (Optical Proximity Effect) and flare caused by scattered light of an exposure tool. Unconnected inner dummy via chain is designed to act as dummy arrays for failure analysis using a new failure analysis tool, OBIRCH (Optical Beam Induced Resistance CHange). This test structure can be used for both electrical OPC evaluation and process failure analysis in the 65nm node interconnect and beyond.

11:40 **Test Structures for CD and Overlay Metrology in Alternating**
2.2 **Aperture Phase-Shifting Masks**
*S. Smith, *M. McCallum, A.J. Walton, J.T.M. Stevenson and L. Jiang (The University of Edinburgh, *Nikon Precision Europe, U.K.)*

The ability to test and characterise advanced photomasks for verification

and process control is increasingly important and this paper builds on previous work in this area which left a number of unanswered questions. Atomic force microscope measurements are used to explain anomalies in previously presented electrical test results. In addition, a new test structure has been developed to measure an important parameter in alternating aperture phase shifting masks; the alignment between the chrome blocking features and the phase shifting regions etched into the quartz substrate. Simulation results are presented which demonstrate the capability of the test structure when used in a progressional offset array.

12:00 **Process for Reducing the Linewidths of Test-Structure Features for**
2.3 **Use as Critical D imension Reference Materials**
Ravi Patel, Michael W. Cresswell, Richard A. Allen, Christine E. Murabito, Brandon Park, Monica D. Edelstein and Loren W. Linholm (NIST, USA)

A process has been developed to reduce the linewidths of silicon features for use as Single-Crystal Critical-Dimension Reference Materials (SCCDRM). The new process employs a sequence of three wet etches to reduce the overall width of the replicated features while enabling them to retain their essential cross-section rectangularity and sidewall flatness. This paper will describe the new process and will present a selection of initial results.

12:20 - Lunch

SESSION 3: RF

13:50 - 15:40
Co-Chairs: Seiichi Banba (Sanyo Electric Co. Ltd.)
Sang-gug Lee (Information and Communication Unversity)

13:50 **Invited**
3.1 **From Analog to RF Design**
Willy Sansen (Katholieke University Leuven, Belgium)

The continuous reduction of the channel length of CMOS devices has given rise to fT frequencies in excess of 100 GHz. As a result the analog circuits have reached RF performance. They are now found in numerous applications such as RF frontends for integrated transceivers. The challenges and potential solutions will be discussed of specific transistor level realizations such as Low-noise ampifiers, Voltage-controlled oscillators, mixers and optical receiver preamplifiers.

14:20 **A Novel RFCMOS Process Monitoring Test Structure**
3.2 *C.B. Sia, *B.H. Ong, K.M. Lim, C.Q. Geng, *K.S. Yeo, *M.A. Do, *J.G. Ma and **T. Alam (Advanced RFIC (S) Pte Ltd., *Nanyang Technological University, Singapore, **Cascade Microtech, Inc., USA)*

A novel RFCMOS process monitoring test structure has been proposed for the first time in this paper. Excellent agreement in DC and RF characteristics has been observed between conventional test structure and the new process monitoring test structure for both n and p MOSFETs of different device dimensions. This new layout approach

can be extended to other devices such as MIM capacitors, diodes, mos varactors and interconnects.

14:40 **MOSFET Drain and Induced-gate Noise Modeling and**
3.3 **Experimental Verification for RF IC Design**

*Chih-Hung Chen, Feng Li and *Yuhua Cheng (McMaster University, Canada, *Skyworks Solutions, USA)*

This paper presents a new analytical model for the induced gate noise in MOSFETs including the channel-length modulation (CLM) effect. The implementation of the enhanced channel noise and the induced gate noise using subcircuits based on any compact MOSFET model for RF ICs is also demonstrated. Simulation and measurement results using a 0.18μm CMOS process are presented. The impact of the induced gate noise and the channel noise with the CLM effect on different transistors is also studied.

15:00 **A Novel Method to Obtain 3-port Network Parameters for a**
3.4 **MOSFET from 2-port Measurements**

*Anuranjan Jha, J.M. Vasi, *Subhash. C. Rustagi and Mahesh B. Patil (Indian Institute of Technology Bombay, India, *Institute of Microelectronics, Singapore)*

Two-port description of a four-terminal device like the MOSFET is incomplete. For complete analysis and at higher frequencies, four terminal characteristics have to be obtained. We describe a simple and novel measurement technique to obtain the complete description from two-port measurements on a single test structure. Such measurements are reported for the first time for a MOSFET.

15:20 **An accurate and scalable differential inductor design kit**
3.5 *C.B. Sia, K.W. Chen, C.Q. Geng, *K.S. Yeo, *M.A. Do, *J.G. Ma, W. Yang, **Sanford Chu and **K.W. Chew (Advanced RFIC (S) Pte Ltd., *Nanyang Technological University, **Chartered Semiconductor Manufactuaring Ltd., Singapore)*

An accurate and scalable RF differential inductor design kit is presented in this paper. The RF model in this design kit is accurate and continuous, capable of predicting all the differential inductors in the test element group. Coded into a smart and interactive foundry design kit, this scalable inductor model can be fully exploited to help cope with the increasing demands of new circuit design trends effectively and efficiently.

15:50 - 16:10 Break

SESSION 4: Interconnect

16:10 - 17:30

Co-Chairs: Yoshio Mita (University of Tokyo)
Michael Cresswell (Natl. Inst. Stds & Tech.)

16:10 **Test Chip for the Development and Evaluation of Test Structures**
4.1 **for Measuring Stress in Metal Interconnect**

*J.G Terry, A.J Walton, A.M Gundlach, J.T.M Stevenson, *A.B Horsfall, *K. Wang, *J.M.M dos Santos, *S.M Soare, *N.G Wright, *A.G O'Neill and *S.J. Bull (University of Edinburgh, *University of Newcastle, U.K.)*

Control of stress in deposited films is important in many processes involved in the manufacture of integrated circuits. This paper presents a test chip that examines both the design and process issues associated with the development of a novel MEMS based stress sensor. It consists of a range of devices that have been specifically designed to monitor the stress in metal films, in this case aluminium. Micromachined stress sensors have previously been reported for measuring stress in polysilicon and germanium films [1, 2] and the structures detailed in this paper are based on similar principles [3-6]. However, the devices published by other groups have not reported stress test structures for evaluating metallic films, which have slightly different properties, in particular plastic deformation. Aluminium is the interconnect film for which the stress sensors have been developed and this paper details some of the design, fabrication and measurement issues associated with the structure.

16:30 4.2 **Test Chip Characterization of X Architecture Diagonal Lines for SoC Design**

*N.D. Arora, *M. Smayling, L. Song, S. Shah and *T Nagata (Cadence Design Systems, *Applied Materials, USA)*

This paper addresses the manufacturability, yield and reliability concerns of an X Architecture (diagonal lines) Silicon-on-Chip (SOC) design that enables IC chips to become faster and smaller (area) compared to the same design in Manhattan structure. Test chips that consist of comb/serpentine, maze, via chain, as well as resistance and capacitance structures are designed and fabricated using both 130nm and 90nm copper processes. The measurements of the line resistance (Kelvin structures), capacitance (inter-digited structure) and SEM data show that 1:1 design rules (Manhattan vs. X Architecture) is manufacturable, and the uniformity and fidelity of the diagonal lines are as good as Manhattan lines. The current generation of mask, lithography, wafer processing techniques are applicable to X Architecture designs.

16:50 4.3 **A Novel Test-Structures for Detail Interconnect Fabric Diagnosis for 90nm Process**

*Shigekiyo Akutsu, *Noriyuki Ishihara and Hiroo Masuda (STARC, *Fuji Research Institute Co., Japan)*

We have developed a novel Test-structure and CAD-tool to strictly diagnose 100nm-level interconnects structure. Features are: (1) quantitative permittivity extraction of Low-K material formed in dense-interconnects fabric, (2) quick statistical inter- & intra-die data measurement of ILD and Metal dimensions from fabricated wafers. To achieve the accurate evaluation of Low-K material, two test-structures are devised; they are multi-metals ILDEx [1] and the one for on-wafer TEM. Also to enhance quick feedback of the interconnect structural-data, a new multi-layer ILDEx test-structure with CBCM circuit are developed. Based

on these new technologies, we have designed 90nm-TEG (Test Element Group) and fabricated it to validate effectiveness. It is noted that the Low-K permittivity, at dense-interconnects fabric, turns out to be 5-10% smaller than that estimated with wide area capacitance measurement. Statistical measurement (extraction) of ILD and Metal dimensions is successfully achieved within the extraction error of less than 5%.

17:10 **Electrical Characterization of Model-based Dummy Feature**
4.4 **Insertion in Cu Interconnects**
*Kelvin Y.Y. Doong, *C.-C. Chu, K.-C. Lin, T.-C. Tseng, Y.C. Lu, S.C. Lin, L.J. Hung, P.S. Ho, Sunnys Hsieh, K.L. Young and M.S. Liang (TSMC. Ltd., *Chang Gung University, Taiwan R.O.C)*

A methodology is proposed to characterize the electrical performance of model-based dummy feature insertion in Cu interconnect. Two types of test structures were designed to explore the electrical discrepancy of the rule-based and model-based dummy feature insertion. The sheet resistance of geometry dependencies is characterized under various density conditions and 2D field solver extracts the parasitic capacitance caused by dummy feature. A algorithm of model-based dummy feature insertion is proposed to assist the uniformity control of Cu CMP and MIT/SEMATECH 854 AZ test vehicle is used to demonstrate the feasibility of the proposed algorithm.

Wednesday, March 24

SESSION 5: Process Characterization

8:30 - 16:00 **registration**

9:00 - 10:30
Co-Chairs: Hidetsugu Uchida (Oki Electric Industry Co. Ltd)
Kelvin Yih-Yuh Doong (TSMC Co. Ltd)

9:00 **Invited**
5.1 **Process and Device Reliability Characterization Techniques for Advanced CMOS Technology: The Issues and Methodologies**
Steve Chung (National Chiao Tung University, Taiwan)

This paper will give an overview of more advanced charge pumping(CP) and Gated-Diode(GD) techniques for the process and reliability characterization of advanced CMOS devices. Its potential use for the device hot carrier reliability study, STI, plasma-induced oxide damage effect, and oxide quality monitoring will be discussed. More recent developments for 1nm range ultra-thin gate oxide CMOS device applications will also be demonstrated. Further development and the roadblocks of these techniques will be addressed.

9:30 **Development of a 90nm Large-scale TEG for Evaluation and**
5.2 **Analysis of Signal Integrity, Yield and Variation**
*Masaharu Yamamoto, *Yayoi Hayasi, *Hitoshi Endo and Hiroo Masuda (STARC, *Hitachi ULSI Systems Co. Ltd., Japan)*

We have developed the 90nm TEG (Test Element Group) that has large-scale patterns which compare well to those of an SoC and has 4-corner address decoders. This TEG is based on the design rules of pure processes that are independent of the products. We have successfully measured pure process yield, failure terms, and failure locations and evaluated characteristic variation in a chip. Stress tests and signal integrity evaluation were also implemented. With use of the electrical dimension measurement, charge-up damage, and analysis database software, this TEG will lead to a strategic 65nm technology.

9:50
5.3 **Gate-Last MISFET Structures and Process for High-k and Metal Gate MISFETs Characterization**

T. Matsuki, K. Torii, T. Maeda, H. Syoji, K. Kiyono, Y. Akasaka, K. Hayashi, N. Kasai and T. Arikado (Selete Inc., Japan)

We propose new test device structures, Gate-Last-Formed structures, for fundamental study of high-k and metal gate electrode MISFETs. The gate stack is formed after local interconnect pads for source/drain. And the gate stack formed in trench formed by dry and wet etching in a non-self-aligned to source/drain. The wet etching restricts damage formation on the exposed the trench bottom. This structure can provide fundamental performance of new gate materials with short TAT and avoiding contamination to a fab.

10:10
5.4 **A Novel Measurement Method of the Spatial Carrier Lifetime Profile Based on the OCVD Technique**

Salvatore Bellone, G. Domenico Licciardo and H.C. Neitzert (University of Salerno, Italia)

Using an original test structure we show by numerical simulations that the OCVD method can be improved to obtain the spatial profile of the τ_{PO}, τ_{NO} lifetime parameters along the epilayer of *n*-*n*+ wafers. The test structure consists of a surface diode including an additional n^+ region, where the diode is used to inject minority carriers within the epilayer, the sense region allows one to measure the diode voltage without the series resistance effect, and finally a positive voltage applied to the n^+ substrate is used to electrically control the epilayer volume where carriers recombine.

10:30 - 11:00 Break

SESSION 6: Matching

11:00 - 12:00

Co-Chairs: Yoichi Tamaki (Hitachi Ltd.)
Gregory Yeric (TestChip Technologies Inc.)

11:00
6.1 **Measuring the span of stress asymmetries on high-precision matched devices**

*H.P. Tuinhout, *A. Bretveld and **W.C.M. Peters (Philips Research , *Philips Consumer Electronics, **Philips Semiconductors, The Netherlands)*

How far do mixed-signal circuit designers have to keep layout

asymmetries away from matched device constructions? This paper discusses test structures to answer this question, which is highly relevant for high precision analogue small signal processing as well as test structure de- signers interested in mismatch characterisation. How far do you keep your pads and metal wiring away from your matching test structures?

11:20 **Impact of pocket implant on MOSFETs mismatch for advanced**
6.2 **CMOS technology**

*K. Rochereau, *R. Difrenza, **J. Mc Ginley, *O. Noblanc, *C. Julien, **S. Parihar and *P. Llinares (Philips Semiconductors, *STMicroelectronics, **Motorola corp., France)*

This paper deals with MOS transistors mismatch for advanced 120 nm and 90 nm CMOS technologies. In particular we demonstrate pocket impact on gate contribution that becomes more and more important with the gate oxide thickness reduction. Such phenomenon can appear as a limit for matching improvement with CMOS technologies evolution.

11:40 **A New Test Circuit for the Matching Characterization of npn**
6.3 **Bipolar Transistors**

Jan Einfeld, Ulrich Schaper, Ute Kollmer, Peter Nelle, Jürgen Englisch and Matthias Stecher (Infineon Technologies AG, Germany)

A new test macro with an active device array is presented for the mismatch characterization of npn bipolar transistors. The macro contains a CMOS circuit which serves for the selection of each bipolar device individually. For each bipolar terminal a force/sense method is employed to assure the high voltage accuracy requested for bipolar transistors. The characterization of the array having transistors with different geometry gives a database on chip level sufficient for the statistical analysis. Matching parameter are given for collector current, current gain, and base-emitter voltage of a 0.5µm smart power technology.

12:00 - Lunch

13:30 - 13:40 ICMTS 2005

SESSION 7: Device Characterization

13:40 - 15:00

Co-Chairs: Manabu Kojima (Fujitsu Ltd.)
Kinam Kim (Samsung Electronics Co. Ltd.)

13:40 **Invited**
7.1 **Device Characterization and Physical Model of Strained-Si Channel CMOS**

,Shin-ichi Takagi, *Tatsuro Maeda, Toshinori Numata, Tomohisa Mizuno, Koji Usuda, Akihito Tanabe, Tsutomu Tezuka, Shu Nakaharai, Junji Koga, Toshifumi Irisawa, Yoshihiko Moriyama, Norio Hirashita and Naoharu Sugiyama (MIRAI-ASET, *MIRAI-AIST, **The University of Tokyo)*

Recent progress on the development of strained-Si CMOS is reviewed with emphasis on the electrical properties. The device parameters extracted from strained-Si CMOS and the physical models, indispensable in describing the electrical characteristics, are presented. In addition, new requirements for device characterization, specific to strained-Si devices, which include strain control and influence of Ge, will also be addressed.

14:10 7.2 **An array cell transistor test structure for the leakage current analysis of stacked capacitor DRAMs with diagonal cell scheme**

Young Pil Kim, Beom Jun Jin, Gi-Sung Yeo, Sun-Ghil Lee, Siyoung Choi, Uin Chung, Joo Tae Moon and Sang U. Kim (Samsung Electronics Co. Ltd., Korea)

A new test structure for a stacked capacitor DRAM cell transistors with a diagonal active-area was developed to analyze the leakage current characteristics of the cell transistors. The leakage current components of the low power DRAMs with different retention fail distributions was investigated in detail using the test structure. The test structure traces the main distribution of the retention characteristics well. The important aspect of the sub-threshold leakage component was discussed for below 0.11μm DRAM cell transistors.

14:30 7.3 **New Device Structure for 18-V, High-performance SOI Complementary Bipolar LSIs using Array Transistors and Flexible U-grooves**

*Yoichi Tamaki, *Kousuke Tsuji, **Osamu Ohtani, Hideaki Nonami, Toshiyuki Tomatsuri, Eiichi Yoshida and Masato Hamamoto (Hitachi Ltd., *Hitachi VLSI Engineering Co., **Renesas Eastern Japan Semiconductor Inc., Japan)*

We have developed a new device structure for high-performance and high-power mixed signal LSIs using SOI complementary bipolar transistors. New structure is composed of array transistors for various operating currents and flexible U-groove layout for high-power transistors. Simulation and test structure measurements showed the advantage of the new structure quantitatively.

14:50 7.4 **Characterization & Modelling of Low Electric Field Gate-Induced-Drain-Leakage**

D. Rideau, F. Agut, L. Giguerre, A. Dray, G. Gouget, M. Minondo and A. Juge (STMicroelectronics, France)

The reduction of the junction leakage current of MOSFETs transistors becomes a crucial issue in the forth coming generation of devices. Besides the junction current that depends on the drain-to-bulk voltage, an additional leakage current that depends on the gate-to-drain voltage is observed at the drain terminal. This Gate Induced Drain Leakage (GIDL), which has become one of the most limiting factor on advanced double-oxide devices, can even be larger than the channel off-current of long devices. In this paper, we present measurements of GIDL at various temperatures and terminal biases. Besides Band-to-Band (BBT) tunneling leakage, we also observed Trap-Assisted-Tunneling (TAT) leakage current. While BBT GIDL has been considerably studied and is

now available in public domain compact models such as BSIM4, TAT GIDL has received less attention. In what follows, we propose an empirical model for TAT GIDL suitable for compact modelling.

15:10 - 15:20 Break

SESSION 8: Poster

15:20 -

Co-Chairs: Takashi Ohzone (Okayama Prefecutral University)
A. J. Walton (University of Edinburgh)

15:20 **Further Study of V_{TH}-Mismatch Evaluation Circuit**
8.1 *Kazuo Terada and Kouhei Fukeda (Hiroshima City University, Japan)*

A new test chip is developed for further studying the test circuit, with which the MOSFET threshold-voltage (V_{TH}) mismatch can easily be evaluated and which is proposed in the previous ICMTS. The data obtained from the test circuits having different design channel width, design channel length, MOSFET number and channel conductivity show reasonable dependency of the V_{TH}-mismatch on those parameters.

15:23 **Design and Measurements of Test Element Group Wafer Thinned**
8.2 **to 10um for 3D System in Package**
*Akihiro Ikeda, Tomonori Kuwata, Satoru Kajiwara, Tsuyoshi Fujimura, Hisao Kuriyaki, Reiji Hattori, *Hiroshi Ogi, *Kiyoshi Hamaguchi and Yukinori Kuroki (Kyushu University, *Hara Seiki Industry Co. Ltd., Japan)*

We designed and measured test element group wafers thinned to 10um for the evaluation of 3D system in package. Some of the pn- and np-diodes on the 10um thick wafer showed smaller forward currents than the currents of diodes on the 30um thick wafer or wafer without back grinding. The resistivity of Al wires or via contacts in the 10um thick wafer may be increased by wafer bending during wafer handling after the wafer thinning process. nMOSFETs and pMOSFETs were also measured on the 10um thick wafer.

15:26 **Flicker Noise Characterization of Co-Silicide/SiGe Contacts Using**
8.3 **TLM Test Structures**
Kun-Ming Chen and Guo-Wei Huang (National Nano Device Laboratories, Taiwan R.O.C)

The flicker noise characteristics of Co-silicide/p^+-SiGe contacts with different epitaxial structures have been studied. By using transmission line method (TLM) test structures, the contact and bulk noise contributions can be separated. In our work, we find that the contact noise in Co/Si/SiGe sample is lower than that in Co/SiGe one due to less defects at interface. The improved interface quality will reduce the contact resistance.

15:29 **A test structure to verify the robustness of silicided N+/P+ interface**
8.4 *Cheng -Yao Lo, Shyue-Shyh Lin, Wei-Ming Chen and Yuh-Jier Mii (TSMC Ltd., Taiwan R.O.C)*

We propose a new test structure that provides a single current path for silicide robustness detection at N+/P+ butted well tap interface with good sensitivity. Two reference test structures suspected with more than one current path and consequently give false results are also compared for structure and electrical performances.

15:32 8.5 **A Test Structure for two-dimensional Analysis of MOSFETs by Hot-Carrier-Induced Photoemission**

*T. Matsuda, A. Muramatsu, H. Iwata, *T. Ozone, **K. Yamashita, **N. Koike and **K. Tatsuuma (Toyama Prefectural University, *Okayama Prefectural University, **Matsushita Electric Ind. Co. Ltd., Japan)*

A test structure and method for two-dimensional analysis of fabrication process and reliability of MOSFET using a photoemission microscope are presented. Arrays of 20x10(=200) MOSFETs were successfully measured at a time and evaluated the fluctuation of their characteristics. The fluctuation of hot-carrier-induced photoemission intensity was larger as gate length becomes smaller. Although the intensity of photoemission in the same MOSFET was within small range, photoemission from all over the MOSFET array was relatively large and independent of the position in the array.

15:35 8.6 **Leakage current correction in quasi-static C-V measurements**

J. Schmitz and M. H. H. Weusthof (University of Twente, The Netherlands)

Several methods of leakage current correction in the quasi-static capacitance-voltage measurement are presented and discussed. Limitations of all methods are quantified and workarounds are proposed.

15:38 8.7 **A test chip to characterise P-MOS transistors produced using a novel organometallic material**

*M.H. Dicks, *G.M. Broxton, *J. Thomson, *J. Lobban, A.M. Gundlach, J.T.M. Stevenson and A.J. Walton (University of Edinburgh, *University of Dundee, U.K.)*

A test chip is reported to characterise MOS transistors with a platinum gate fabricated using a solid organometallic material. Threshold and source-drain characteristics are presented along with oxide leakage measurements. These results are compared with aluminium gate transistors manufactured on the same substrate. Both sets of characteristics are very similar with the major di erence being that the platinum gate devices have a lower sub-threshold slope.

15:41 8.8 **Characterization And Model of 4-Terminal RF CMOS With Bulk Effect**

M.T. Yang, Y.J. Wang, T.J. Yeh, Patricia P.C. Ho, Y.T. Chia and K.L. Young (TSMC Ltd., Taiwan R.O.C)

Special test structures using separated source and bulk contacts with the 3rd GSG probe for the substrate bias are described. These test structures allow characterizing 4-terminal MOSFETs with a standard two-port

Network Analyzer. The high-frequency behavior of bulk effect in MOSFETs is studied at different bias conditions for a 0.18 μm RF CMOS technology. Measurement result of RF NMOSFET shows that a good accuracy of the 4-terminal RF MOSFET modeling is achieved. The validity and accuracy of our approach is verified and analyzed from two-port Y-parameter results.

15:44 8.9 **High frequency test structures definition for the study of flip-chip process effects on inductor coupling in a BiCMOS process**
C. Clément, B. Van-Haaren, and Daniel Gloria (STMicroelectronics, France)

Study of flip-chip process effects on coupling between two inductors or an inductor and a ground plane has been achieved to define design rules for device relative placement on silicon and on glass face to face. In this paper, High Frequency test structures are described and results from S parameter measurements are presented. HFSS complementary simulations have been achieved to complete the coupling abacus and therefore define design rules.

15:47 8.10 **Design Guide and Process Quality Improvement For Treatment of Device Variations in an LSI Chip**
Masakazu Aoki, Shin-ichi Ohkawa and Hiroo Masuda (STARC, Japan)

We propose guidelines for LSI-chip design, taking the within-die variations into consideration, and for process quality improvement to suppress the variations. The auto-correlation length, λ, of device variation is shown to be a useful measure to treat the systematic variations. The random variations, on the other hand, exhibit complete randomness even in the closest pair transistors, which requires careful choice of gate size in designing balanced circuits. Poly-Si gate formation is estimated to be the most important process to ensure the special uniformity in transistor current and to enhance circuit performance.

15:50 8.11 **Method of and Test Structures for Measuring Intra-layer Coupling Capacitance based on Charge Based Capacitance Measurement Technique**
Kai-Ye Huang and Chuan-Jane Chao (Winbond Electronics Corp., Taiwan R.O.C)

This study presents an novel test structure and a two-step method for measuring intra-layer coupling capacitance C_c based on charge based capacitance measurement technique, which consumes less wafer area and gives simple and high-resolution extraction of interconnect parameters. The comparison on C_c between measurement and simulation results shows good agreement with error less than 5%.

15:53 8.12 **Optimization of 2.14 um^2 6T-SRAM cell by using Cell-like Test Structures**
Sunnys Hsieh, R.F. Tsui, Wesley Lin, C.Y. Yang , J.J. Liaw, Kelvin Y.Y. Doong and C.-M. M. Wu (TSMC Ltd., Taiwan R.O.C)

This work describes the optimization of shrink version of embedded 6T-

SRAM cell process and the evaluation of yield impact by using cell like test structures. The various test structures are designed to extract the cell characteristics and the electrical performances of cell-like test structure are used to evaluate the integration process. This work reveals that the concern and trade-off of SRAM cell-like test structure design and their electrical measurement. Design rule evaluation and process window optimization can be easily performed by using the electrical measurement as screening criteria, which of the complete set of SRAM cell-like test structures are proposed by this work.

15:56 **Implementing laser based failure analysis methodologies using test**
8.13 **vehicles**

**D. Lewis, V. Pouget, *F. Beaudoin, T. Beauchene, **G. Haller, ***R. Desplat, ***P. Perdu and P. Fouillat (IXL Laboratory, *Thales Microelectronics, **STMicroelectronics, ***CNES laboratory, France)*

Different test vehicles were designed in order to validate laser based failure analysis and process validation techniques. Two vehicles concerns defect localization in integrated circuits; the third one is designed for single event upset sensitivity study in digital integrated circuits.

15:59 **Error Evaluation of C-V Characteristic Measurements in Ultra-**
8.14 **Thin Gate Dielectrics**

Hiroyuki Suto, Satoshi Inaba and Kazunari Ishimaru (Toshiba Corporation Semiconductor Company, Japan)

The errors of C-V characteristic measurements by I-V method for ultra-thin gate dielectrics were studied from viewpoint of measurement systems. It was found that there were two reasons for the error at low measurement frequencies: (1) the uncertainty of the phase angle of measured impedance, and (2) the small parallel shift of measured impedance due to large DC currents. It was also found that the error due to (1) could be excluded by the phase rotation correction of the impedance and measurements at higher frequencies. The error due to (2) should be avoided only by measuring capacitors with small gate areas.

16:02 **An Accurate RF CMOS Gate Resistance Model Compatible with**
8.15 **HSPICE**

,H. W. Lin, *S. S. Chung and **S. C. Wong (*National Chiao Tung University, **Acer Lab. Inc., Taiwan R.O.C)*

A new gate resistance model for RF simulation in Spice is successfully developed. Physically, this gate resistance is modeled as the intrinsic gate resistance in parallel with a resistance coupled from the channel. This resistance coupling comes from the ac excitation of the high frequency signal through the gate. Therefore, it is bias dependent. Also, we observed that this gate resistance is temperature dependent. Both models can be incorporated into Spice for a good prediction of the RF CMOS high frequency characteristics.

16:05 **Development and Extraction of High-Frequency SPICE Models for**
8.16 **Metal-Insulator-Metal Capacitors**

W. Z. Cai, M. Azam, C. Hoggatt, G. H. Loechelt, S. C. Shastri, G. M. Grivna and S. Dow (ON Semiconductor Corporation, USA)

Metal-insulator-metal (MIM) capacitors are of great importance in mixed-signal and RF integrated circuits. Yet, the RF properties of a MIM capacitor are strongly influenced by its parasitic components, such as series resistance and inductance. Previous author used frequency-independent R_S and L_S without a thorough justification, while others claimed that a frequency-*dependent* R_S was needed in order to match experimental results. In this work, we demonstrate that a frequency-independent L_S fits the experimental results, and propose, for the first time, a distributed MIM model.

16:08 8.17 **Direct Extraction Methodology For Geometry-Scalable RF-CMOS Models**

*Sorin P. Voinigescu, *Mihai Tazlauanu, **P.C. Ho and **M.T. Yang (University of Toronto, *Quake Technologies Inc., Canada, **TSMC, Taiwan R.O.C)*

A new method to directly extract the MOSFET small-signal parameters - including non-quasi-static effects - from *Z* and *Y* parameter measurements is presented. This technique is employed to generate a scalable BSIM3v3 model valid for standard, low and high-threshold p- and n-channel MOSFETs at frequencies up to *50 GHz*. The model accurately captures cutoff frequency degradation for finger widths below 1μm and was employed to verify the measured jitter of a MOS-CML output driver at data rates as high as 14-Gb/s.

16:11 8.18 **Evaluating High Leakage Effects of Low V_{TH} Circuits using High V_{TH} Devices**

Takayuki Miyazaki and Takayasu Sakurai (University of Tokyo, Japan)

A scheme to emulate leakage current of low threshold MOSFET's using high threshold MOSFET's is proposed. The leakage current at any threshold voltage lower than the original threshold voltage can be emulated without changing a manufacturing process. Furthermore, a single test structure can be used to measure the leakage current at various threshold voltages. The DIBL (Drain Induced Barrier Lowering), source control, and substrate bias effect can be reproduced by the scheme. A test chip is manufactured and measured to show the validity of the proposed leakage emulator.

16:14 8.19 **Transistor Test Structures for Leakage Current Analysis of Partial SOI**

*K. H. Yeo, C. W. Oh, S. M. Kim, M.S. Kim, H. Sung, S. A. Lee, C. S. Lee, S. Y. Lee, S. Y. Han, E. J. Yoon, H. J. Cho, D. Y. Lee, B. M. Yoon, H. S. Rhee, B. C. Lee, J. D. Choe, *I. Chung, D. Park and K. Kim (Samsung Electronics Co., *Sungkyunkwan Univ., Korea)*

A highly manufacturable Pi (Partially Insulated) FET has been fabricated by Si/SiGe epitaxial growth and selective SiGe etch process. Using these technologies, pseudo-SOI (Silicon On Insulator) could be realized with excellent structural advantages through the hole and body-tied scheme without area penalty. Junction capacitance, leakage current, and DIBL

can be reduced comparable to SOI devices, while the floating body problem is cleared. We believe this PiFET structure is a promising candidate for the future transistors. We demonstrate the preliminary characteristics of two types of PiFETs.

16:17 **Merits and Limitations of Circular TLM structures for contact**
8.20 **resistance determination for novel III-V HBTs**
J.H. Klootwijk and C.E. Timmering (Philips Research Laboratories)

In the ever-continuing race for higher frequencies and velocities with semiconductor devices, rather common issues like realizing good ohmic contacts still are becoming increasingly important. In particular case of high-speed bipolar transistors, concerning higher frequencies with accompanying higher current densities, the contact resistance to the highly doped regions of the bipolar transistors(emitter, base and collector contact) increasingly dominates the device's performance. Therefore, there is still a need for accurate measurements in order to determine the contact resistance, R_c, and the specific contact resistance, ρ_c, of metal contacts to (highly doped) semiconductors. This paper describes merits and limitations of the so-called CTLM structures (Circular Transfer Length Method). These structures appear to be a simple yet very powerful tool in optimizing the contact resistance for III-V based heterojunction bipolar transistors(HBTs).

16:20 **New Test Structure for High Resolution Leakage Current and**
8.21 **Capacitance Measurements in CMOS imager applications.**
*Francois Odiot, *Jed Hurwitz, *Linsay Grant, Brendan Dunne, Jean. Michel Moragues (STMicroelectronics, France, *STMicroelectronics, U.K.)*

Measurement of dark current and capacitance of piel array are fundamental in the development of new sensor technologies. These parameters are usually very low and require large structures to be accurately measured. This is area consuming and, in any case, needs the use of high-resolution semi-automatic test bench. In this paper, a new methodology based on a capacitance discharge measurement is proposed and validated by comparison to direct measurements. It offers a small structure need, a low-test time and a high resolution, and can also be implemented on full automatic test bench for in-time monitoring.

16:23 **Variation Status in 100nm CMOS Process and Below**
8.22 *Keiji Nagase, Shinich Ohkawa, Masakazu Aoki and Hiro Masuda (STARC, Japan)*

This paper addresses a new variability diagnostics and variability design methodology in sub-100 nm process era. We developed a 130nm DMA(Device Matrix Array)-chip which diagnoses within-die device and circuit variations [1]. And then we enhanced it for 90nm process. Our experiments show a significant increase of MOS Ids variation in 90nm process. It is found that the Ids variation is caused by STI-trench mechanical stress as well as dopant-fluctuation under the active gate area. Foundary-provided worst-corner SPICE models were also intensively evaluated. Because of lack of detail investigation on within-die variation data at the foundary, it is found that the model parameters

suffer from unrealistic variation guard-band in both device performances and circuit characterizations. It reveals the worst-corner of the foundary practically cover only 1.5-sigma for small-size MOST's used in Library cells, which is clarified by the measured wafer data with the DMA test-structure.

16:26 **Test Structures and Analysis Techniques for Estimation of the**
8.23 **Impact of Layout on MOSFET Performance and Variability**
Sharad Saxena, Seán Minehane, Jianjun Cheng, Manidip Sengupta, Christopher Hess, Michele Quarantelli, Glenn M. Kramer and Mark Redford (PDF Solutions, USA)

The performance and variability of transistors with nanometer scale feature sizes found in modern IC technologies is impacted by their layout style and environment. This paper describes the use of an enhanced MOS array test structure to provide accurate and precise estimates of the impact of layout on transistor characteristics for an advanced 130 nm CMOS technology. Enhanced MOS arrays combined with statistical analysis of the measurements provide reliable information on the impact of layout on the transistor characteristics, which can form the basis for technology development, design rule development and modeling.

18:30 - Banquet

Thursday, March 25

SESSION 9: Parameter Extraction

8:30 - 11:00 R**egistration**

9:00 - 10:30

Co-Chairs: Satoshi Habu (Agilent Technologies Japan, Ltd.)
Kevin McCarthy (University College Cork)

9:00 **Invited**
9.1 **Test Circuits for Extracting Sub-100nm MOSFET Technology Variations with the MOSFET model HiSIM**
*Mitiko Miura-Mattausch, Hans Juergen Mattausch, H. Ueno, *S. Itoh, *K. Morikawa and *K. Nagase (Hiroshima University, *STARC)*

We propose a method for extracting the inter- and intra-chip variations of device parameters to secure reliable circuit design. The method employs circuits sensitive for technology variations and the circuit simulation model which enables to interpret the correlation, namely the MOSFET model HiSIM developed on the basis of the surface potential description. The method demonstrates the validity for advanced MOSFET technologies.

9:30 **Varactor Modeling Methodology for Simulation of the VCO Tuning**
9.2 **Sensitivity**
Domagoj Šiprak and Andreas Roithmeier (Infineon Technologies AG, Germany)

A modeling methodology for CMOS varactors is presented using a simple test structure and a new device target function which is based on the definition of the differential frequency tuning sensitivity K_{VCO} of a voltage controlled oscillator (VCO). Parameter extraction applying the new methodology is demonstrated for a BSIM4 MOS model. A good agreement between measurement and simulation of K_{VCO} for a 4 GHz VCO built in a 0.25µm BiCMOS technology is achieved using a varactor model extracted with the new methodology.

9:50
9.3 **A New Analytical Inductance Extraction Technique of On-wafer Spiral Inductors**
Hideki Shima, Toshimasa Matsuoka and Kenji Taniguchi (Osaka University, Japan)

We derived a simple scalable self-inductance model of interconnection lines connected to spiral inductors. With the use of the model, intrinsic inductance of any spiral inductors with square shape can be extracted from the measured results without any special fixtures. It is experimentally proved that the method is accurate enough to extract intrinsic inductance of on-wafer spiral inductors within the error of 3%.

10:10
9.4 **Experimental Measurements and Extraction of the Silicide/Silicon Interface Resistance for Designing High Performance MOS Transistor**
Jae-Hun Jeong, Hoon Lim, Soon-Moon Jung, Joon Bum Park, Jae Kyun Park and Kinam Kim (Samsung Electronics Co. Ltd., Korea)

The new and simple test structure for extracting the resistance of salicide/ Si active interface is proposed. From extracting Rint and measuring the current characteristics of the MOSFET for various process conditions, it is proved experimentally for the first time that the performance of MOSFET is directly proportional to the salicide-Si active interface resistance. The new test structure is a very accurate and effective tool to optimise the process condition for the high performance CMOS process, such as n+(or p+) S/D ion implantation and Cosalicidation process.

10:30 - 10:50 Break

SESSION 10: Capacitance

10:50 - 12:10

Co-Chairs: Hiroaki Hazama (Toshiba Corporation Semiconductor Company)
Alexander Rahm (SIEMENS AG)

10:50
10.1 **An Impedance-phase angle (Z-theta) Method for Capacitance Extraction of Ultra-thin Gate Dielectrics at Intermediate Frequency**
Joyce Lin, Chien-Hwa Chang, Sharad Prasad and William Loh (LSI Logic, USA)

Traditional C-V measurement is not accurate for extraction of gate oxide thickness below 15 Å due to high gate leakage current. In this paper, without using such high frequency approach as S-parameter extraction, we propose a new approach using Z-theta (Impedance-Phase angle) measurement and a more comprehensive equivalent circuit

model. A Parameter Extraction Tool (PET), consisting of HSPICE simulator and a least square optimizer, is developed to extract the gate capacitance from the Z-theta measurement and a new equivalent circuit model. This method can account for parasitic effects such as stray capacitance induced by chuck and inductance at high frequency. We demonstrated that this proposed approach has the capability to measure the gate capacitance correctly down to 10 Å.

11:10
10.2 **An Accurate Measurement and Extraction Method of Gate to Substrate Overlap Capacitance**

Masanori Shimasue, Yasuo Kawahara, Takeshi Sano and Hitoshi Aoki (MODECH Inc., Japan)

Gate-to-bulk overlap capacitance (*CGBO*) cannot be ignored for long gate channel MOSFET's that are used for various I/O and analog circuits. We present a simple and yet accurate *CGBO* measurement and extractions by using a group of MOSFET's. Dedicated test structures using 0.18 μm shallow trench isolation technology were fabricated for the purpose. The effect of *CGBO* has been successfully analyzed by comparing measured and simulated time period delay of ring oscillators.

11:30
10.3 **Optimal frequency range selection for full C-V characterization above 45MHz for ultra thin (1.2-nm) nitrided oxide MOSFETs**

*W. Jeamsaksiri, A. Mercha, J. Ramos, S. Decoutere and *F.N. Cubaynes (IMEC, *Philips Research Leuven, Belgium)*

We demonstrate a very simple and accurate way to select the proper frequency range in order to achieve full *C-V* curves with RF test structures. The technique is demonstrated on ultra thin nitrided oxide down to 1.2 nm with very high gate leakage densities (3490 A/cm^2 at V_{GS} = 2.5 V). For a test structure with high series resistance, the *C-V* curves are corrected using 2-frequency method (2FT) and show frequency independence proving the validity of the correction.

11:40
10.4 **Accuracy improvement of the "Single Pattern Driver" method for the characterization of interconnect capacitance in the context of nanometer technology development**

H. Brut, S. Martin and B. Froment (STMicroelectronics, France)

Characterization, modelling and monitoring of interconnect capacitance are of first interest for CMOS and BICMOS technology development, especially for circuit delay evaluation. An improvement of the Single Pattern Driver method is proposed in this paper to take into account MOST intrinsic and diode leakages which can introduce errors of the order of few hundred aF in advanced nanometer technologies. The accuracy is hugely improved and reaches now few aF.

12:00 End of Exhibition

12:10 Best Paper Announcement
Closing Remarks

12:15 End of Conference

12:30 Excursion

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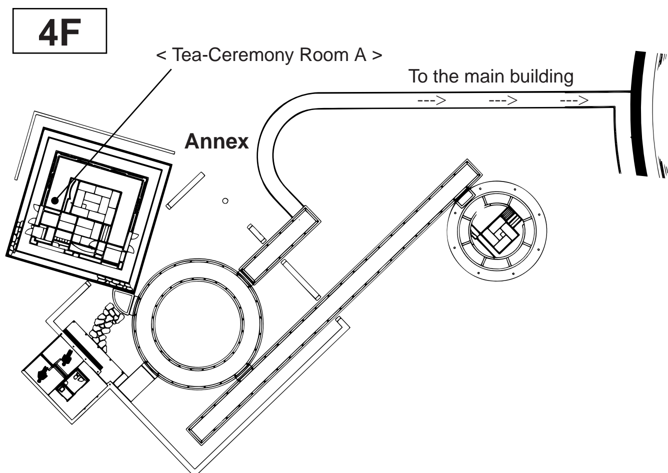
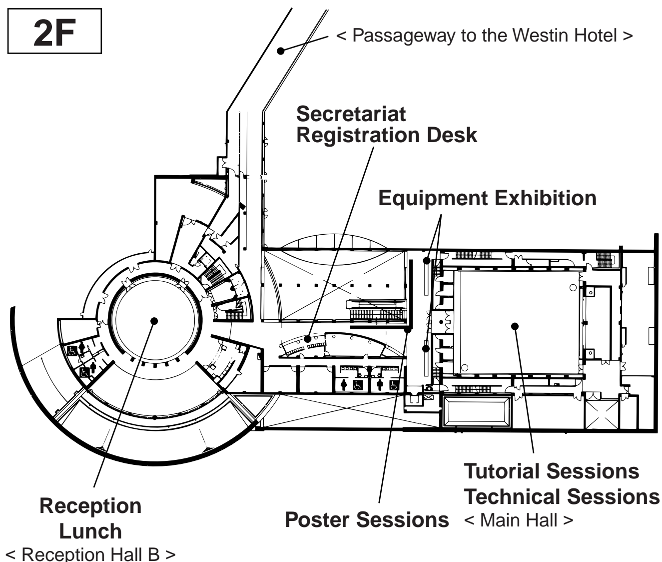
Map of Conference Site





*Banquet will be held in "The Miracle Planet Museum of Plants" in Awaji Yumebutai.

ICMTS 2004 CONDENSED PROGRAM

Monday, March 22

Time	Event
8:00	Registration
9:00	Introduction
9:05	Test Structure Fundamentals
9:55	Test Vehicle Design
10:45	Break
11:15	Gate Capacitance Evaluation
12:05	Lunch
13:30	Yield & Variation
14:20	Spice Modeling
15:10	Break
15:40	RF Modeling
16:30	Matching
17:20	Wrap-Up and Conclusion
	Welcome Reception

Tuesday, March 23

Time	Event
8:00	Registration
9:00	Opening Remarks
9:10	Session 1 (Reliability & System Integ.)
10:40	Exhibition Presentations
10:50	Break
11:20	Session 2 (CD Metrology)
12:20	Lunch
13:50	Session 3 (RF)
15:50	Break
16:10	Session 4 (Interconnect)

Wednesday, March 24

Time	Event
8:30	Registration
9:00	Session 5 (Process Characterization)
10:30	Break
11:00	Session 6 (Matching)
12:00	Lunch
13:30	ICMTS2005
13:40	Session 7 (Device Characterization)
15:10	Break
15:30	Session 8 (Poster)
18:30	Banquet

Thursday, March 25

Time	Event
8:30	Registration
9:00	Session 9 (Parameter Extraction)
10:30	Break
10:50	Session 10 (Capacitance)
12:00	End of Exhibition
12:10	Best Paper Announcement Closing Remarks
12:15	End of Conference
12:30	Excursion