ICMTS 2003

International Conference on Microelectronic Test Structures

Tutorial and Technical Program

March 17-20, 2003

DoubleTree Hotel at Fisherman?s Wharf

Monterey, California USA

Dear Colleague,

On behalf of the committee, I am pleased to invite you to attend the 2003 International Conference on Microelectronic Test Structures (ICMTS 2003) in Monterey, California. The conference, sponsored by IEEE Electron Device Society, brings together designers and users of test structures from all over the world to discuss the most recent test structure developments and future directions.

Semiconductor manufacturing feature sizes have been reduced on a constant path over the last 30 years, which has allowed designers to put more and more devices and circuit components on a single chip. With every newly introduced technology node such designs will run faster as well. Given today's design and manufacturing complexity, it is crucial to maintain the bridge between chip design and manufacturing process steps to guarantee functionality, performance and yield. Designing chips requires more accurate simulations not just of the single devices and parts of circuits, but also a timing and performance simulation of the entire chip. The complexity of systems on a chip even more challenges simulation capabilities due to the mixture of digital logic design, memory components as well as analog circuits. All these simulations rely on models that need a constantly increasing number of calibration variables, which have to be extracted from a semiconductor manufacturing process. Chips containing a variety of test structures are the main vehicles used to extract such variables as well as to calibrate and control each individual manufacturing process step.

ICMTS 2003 is the 16th time ICMTS will be held as an international conference. ICMTS began in 1986 as a workshop, becoming an international conference in 1988. The conference has been able to maintain its workshop-like friendliness through ample social activities. Coffee breaks, hosted lunches, and a banquet ensure that participants get the chance to interact frequently, meeting others in their field and sharing common experiences.

This year?s conference consists of 43 papers in 10 sessions including a poster session with 7 papers. The conference format provides a single program track (without parallel sessions) on subjects including CD METROLOGY, MEMS AND SENSORS, YIELD, RF, PARAMETER EXTRACTION, RELIABILITY, CAPACITANCE, PROCESS CHARACTER-IZATION, MATCHING. Oral presentations are fifteen minutes long with five minutes for questions. Authors in the poster session will present a brief oral summary of their work in addition to answering questions at their posters. The Poster Session, which will be held as a reception to provide a unique opportunity for a less formal and more in depth discussion with the authors.

The Tutorial Short Course will be held on Monday, March 17, preceding the conference. Eight industry, government, and university experts will give participants guidelines on superior test structure design, efficient and precise test methods, and state of the art data analysis. These presentations are intended to give the audience an introduction to the essential concepts as well as exposure to the current state-of-the-art. There will also be an equipment exhibition for evaluation of the latest versions of measurement equipment, data analysis software, and other test structure related products.

The Conference will be held at the DoubleTree Hotel adjacent to Fisherman's Wharf in the center of Monterey. This beautiful seaside resort community provides the charm of small town America and an endless variety of recreational and cultural activities. Monterey is also home of a world-class aquarium, where this year?s ICMTS banquet will be held on Wednesday, March 19. Both the DoubleTree Hotel and the charming town of Monterey will provide an excellent back drop for a very rewarding technical conference.

Sincerely,

Christopher Hess

General Chairman

GENERAL INFORMATION

The 2003 IEEE ICMTS will be held at the DoubleTree Hotel at Fisherman?s Wharf in Monterey, California. The Conference headquarters hotel will provide guest accommodations as well as meeting facilities for all attendees. The technical program, consisting of ten sessions of contributed papers and a poster session, will be held March 18-20. A tutorial short course will be offered on Monday, March 17.

CONFERENCE REGISTRATION

Payment of the TECHNICAL SESSION registration fee entitles the registrant to one copy of the Technical Digest, entrance to all technical sessions and the exhibit hall, and all social events.

Payment of the SHORT COURSE registration fee entitles the registrant to one copy of the Short Course Workbook and luncheon. Short Course participants must register in advance.

For **Advance Registration,** complete the Registration Form and mail the form with payment to the Conference Headquarters. Advance registration forms must be received by the Conference Headquarters NO LATER THAN February 24, 2003 in order to receive the

reduced registration fee. Registrations received after February 24 will be charged the late registration fee. Short Course participants should register in advance to guarantee a space at the course. On-site short course registration will only be accepted based on space availability.

If you fax your registration form, you must included credit card information and a 5% processing fees for the credit card transactions

Mail or fax your conference registration form and remittance to: 2003 ICMTS Conference

16220 South Frederick Ave., Suite 312

Gaithersburg, MD 20877

1-301-527-0900 x104 * Fax: 1-301-527-0994

Email: wendyw@widerkehr.com

CANCELLATIONS: Refund requests must be received, in writing, by March 3 in order to receive a full refund, less a $25.00 processing fee. Due to financial commitments, refund requests received after March 3 cannot be guaranteed.

IEEE Members: In order to qualify for the member fees, you must list your IEEE membership number.

	ADVANCE (by February 24)	REGULAR (after February 24 and on-site)
Technical Session		
IEEE Member	$420	$480
Non-Member	$470	$530
Student	$275	$330
Short Course (ADVANCE Registration Only)		
IEEE Member	$280	$300
Non-Member	$280	$300
Student	$140	$140

HOTEL RESERVATIONS

A block of rooms has been reserved at the DoubleTree Hotel at Fisherman?s Wharf, Monterey, California. To make a reservation, complete the enclosed Hotel Reservation form and return it, along with one night?s lodging to:

DoubleTree Hotel at Fisherman?s Wharf

2 Portola Plaza

Monterey, CA 93940

Reservations: 800-222-TREE (8733)

Tele: 831-649-4511 Fax: 831-649-3109

Rates: $150 + tax single/double

HOTEL RESERVATIONS MUST BE RECEIVED BY FRIDAY, FEBRUARY 21 to guarantee the conference rate.

All changes and cancellations should be made directly with the hotel. It is the responsibility of each participant to make changes or cancellations no later than 48 hours prior to scheduled arrival. Room reservations will be held until 6:00 p.m. unless a later time is guaranteed by a credit card. Rooms are generally not available for check-in until 3:00 p.m. on the day of arrival.

Parking is available. Valet is $15.00 per day and self-parking is $13.00 per day. There is public parking available at a nominal charge located one block from the hotel.

TECHNICAL SESSION INFORMATION

The Technical Sessions will be held in the Bonsai Ballroom.

POSTER SESSIONS: Poster Session authors will present a five minute talk describing their poster on Tuesday at 3:50 p.m. The poster descriptions will be followed by the poster presentations in the DeAnza Ballroom I. The authors will be available at their displays for questions and discussion.

Posters will be displayed from Tuesday at 1:00 p.m. until Thursday at 12:00 noon.

EQUIPMENT EXHIBITS: ICMTS vendor exhibits will be displayed in the DeAnza Ballroom 1 on Tuesday, March 18 from 1:00 p.m. and will remain on display until 12:00 noon on Thursday, March 20.

If you would like to exhibit at the conference, please contact Jim Reedholm at Reedholm Instruments, 512-869-1935; jimr@reedholm.com. Past exhibitors have included: BTA Technology, Keithley Instruments, Silvaco, Sandia National Laboratories, TestChip Technologies, Cadence, Avanti!, Cascade Microtech, Agilent Technologies, QualiTau, Lucas/Signatone Corp. and Reedholm Instruments.

TECHNICAL DIGEST

Extra copies of the Technical Digest can be purchased by conference through Advance Registration at a cost of $75.00. After the conference, digests will be available through the IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08855.

SOCIAL EVENTS

A Continental Breakfast (8:00 a.m. - 9:00 a.m.) will be available each day of the meeting. The conference will host a Tuesday Luncheon and an Awards Luncheon on Wednesday.

The Conference Banquet will be held on Wednesday,

March 19 at the Monterey Bay Aquarium. The Aquarium is within walking distance of the hotel, but round trip bus transportation will be provided for those who would rather ride. Buses will depart from the front of the hotel starting at 6:30 p.m. One ticket is included with the registration fee, additional guest tickets may be purchased for $75.00.

An opening reception will be held on Monday evening from 7:00 p.m. - 9:00 p.m. and a reception will be held in the Exhibit Hall during the poster displays on Tuesday evening from 4:20 p.m. -- 5:30 p.m.

TRANSPORTATION

By Air: Monterey Peninsula Airport is served by many airlines including American Eagle, Skywest/Delta, Northwest, United and US Air. There are nearly 100 arrivals and departures daily to and from San Francisco and Los Angeles with connections to all domestic and foreign locations. The distance from the airport to the DoubleTree is approximately four miles.

By Car: The drive from San Jose is approximately 60 miles; San Francisco is approximately 120 miles.

Airport Transportation: Taxi service is recommended. The cost is approximately $10.00.

Rental Cars: Several rental car agencies are located at the Monterey Airport: Avis, Budget, Dollar, Hertz, National, and Thrifty.

MESSAGES

A message board will set up in the registration area for conference attendees. Call the hotel at 831-649-4511 and ask for the ICMTS Registration Area. The guest fax number is 831-372-0620.

WEATHER

Monterey enjoys a unique weather pattern, with coastal temperatures averaging 57 degrees year-round. Average temperatures in March range from 45°F - 62°F. It is advisable to bring a jacket, sweater or coat.

MONTEREY AREA ATTRACTIONS

Monterey Bay Aquarium: This fascinating, internationally acclaimed aquarium focuses on educating visitors about the mysteries and wonders of the Monterey Bay.

Big Sur: A 90-mile stretch of coastline that begins in Monterey County a few miles south of Carmel and ends in San Luis Obispo County at San Simeon (Hearst Castle).

Cannery Row: An historic area of the city of Monterey, located on the Bay between the Coast Guard wharf and the pacific Ocean.

Carmel-by-the-Sea: A village in a forest setting located above a breathtaking white-sand beach 5 miles south of Monterey.

Carmel Valley: Twelve miles due east of Carmel-by-the-Sea.

Fisherman?s Wharf and Wharf II: Located on Monterey Bay, in the historic heart of Monterey, off of Del Monte Avenue.

Pebble Beach: On the southern tip of the Monterey Peninsula, due west of Monterey and due north of Carmel-by-the-Sea.

Hearst Castle: A California State Historical Monument containing 165 beautifully furnished rooms, a huge collection of art and antiques, impressive swimming pools, gardens and terraces. Located 90 miles south of Monterey.

TOUR PROGRAM

Thursday, March 20

1:30 p.m. - 5:30 p.m.

$40 per person

Become a connoisseur for the day! A wine tasting and tour has been designed especially for ICMTS participants. Sample award winning wines of Monterey County while touring renowned wineries and tasting rooms. Several wineries are a short picturesque drive from the Peninsula. You?ll sample the wines from Heller Estates, Joullian, Talbot, and Georis. Enjoy interesting narration about this area's history, agriculture and wine industry blended with the writings of famed local author, John Steinbeck

The tour is limited to 40 people, so sign up early to avoid disappointment. To register for the tour, please use the conference registration form.

TUTORIAL SHORT COURSE:

Monday, March 17, 2003

8:30 Registration

9:00 Introduction - Larg Weiland, *PDF Soluttions*

> **9:05 Test Structure Fundamentals - Prof Anthony J. Walton, *Scottish Microelectronics Centre, Department of Electronics and Electrical Engineering, University of Edinburgh, Edinburgh***

Summary:

This presentation will begin with a review of test chips, which will include the development of test structures and their application. Measurement and equipment issues will be addressed concentrating procedures for obtaining accurate and repeatable measurements. The presentation will conclude with a brief review of test structures for measuring sheet resistance, linewidth and contact resistance.

Biography:

Anthony J. Walton is professor of Microelectronic Manufacturing in the School of Engineering and Electronics at the University of Edinburgh. He has been actively involved with the semiconductor industry in a number of areas associated with silicon processing which includes both IC technology and micro-systems. For the 20 years he has had a direct interest in the design, fabrication and measurement of microelectronic test structures as well as taking an active role in the organisation of ICMTS.

He played a key role in setting up the Scottish Microelectronics Centre (SMC), which is a purpose built facility for R&D and company incubation consisting of approximately 300m^2 of class 10 cleanrooms. He has published widely on test structures and is an associate editor of the IEEE Transactions on Semiconductor Manufacturing and The Journal of Electronics Manufacturing.

9:50 Test Pattern for Lithography Process Characterization - Hans Eisenmann, *PDF Solutions GmbH, Munich, Germany*

Summary:

From the early development phases up to the production phase, test pattern play a key role for micro-lithography. This paper discusses the underlying principles of lithography and the different impacts on pattern fidelity. Then, it explains what type of test pattern are used and which effects they characterize. It shows typical measurement curves and gives examples of test pattern applications.

Biography:

Hans Eisenmann received his diploma degree in physics and his doctorate degree in electrical engineering from Technical University in Munich in 1993 and 1999, respectively. His interest is in design automation, algorithm theory, lithography modeling and the correction of lithography-based effects. Dr. Eisenmann holds a best paper award from Design Automation Conference and a best poster award from BACUS.

10:35 Coffee Break

11:00 Pattern Dependent Characterization of Copper Interconnect - Duane Boning, *Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA*

Summary:

Copper technology is gaining acceptance as one means to improve the performance of interconnects and circuits. However, a major challenge continues to be a strong

pattern dependency in the actual thickness of copper wires: pattern density and feature size effects in the electroplating and chemical mechanical polishing (CMP) processes result in across-chip variation in both deposited and polished copper lines. This tutorial will introduce these pattern dependencies, discuss test structures designed to characterize these effects, and show how experimental data can be coupled to chip-scale models for chip screening and design rule generation.

First, single level (e.g. metal1) test structures are covered, where arrays of lines and spaces across a wide range of feature sizes are used with physical (e.g. profilometry) and electrical measurements. These provide information on feature step heights and array "bulges" resulting from electroplating. After polishing, measurements provide information about pattern dependent dishing and erosion of copper and supporting dielectric. Models for copper CMP can then be tuned using such test structures, so that chip-scale predictions can be made for copper line thickness in arbitrary layouts. Second, multi-level (e.g. metal 1/2) test structures will also be described, which enable characterization of the cumulative effect of topography on upper level metal geometry. Extensions for copper/low-k will also be discussed.

Biography:

Duane S. Boning is Associate Professor of Electrical Engineering and Computer Science at MIT, and is Associate Director of the MIT Microsystems Technology Laboratories. His degrees are from MIT in electrical engineering and computer science, earning the Ph.D. degree in 1991. From 1991 to 1993 he was a Member of the Technical Staff at Texas Instruments in Dallas, where he worked on process/device simulation tool integration, semiconductor process representation, and statistical modeling and optimization. At MIT, his research focuses on variation modeling, interconnect technology, and control in semiconductor processes, with special emphasis on chemical mechanical polishing and plasma etch. Additional interests include CAD tools for statistical process, device, and circuit design, network technology for distributed design and fabrication, and computer integrated manufacturing. Dr. Boning has over 120 papers and conference presentations in these areas of research. He is Editor for the IEEE Transactions on Semiconductor Manufacturing, and is a member of the IEEE, ECS, MRS, and ACM.

11:45 Recent Advancements for Improved Yield and Performance based on E-test and Data Mining - Andrew Skumanich, *Applied Materials, Santa Clara, CA*

Summary:

Device performance has become critically important in current advanced processing and defects constitute only a only sub-set of the yield and revenue detracting issues. Electrical test data of test structures is necessary to assess device performance and to potentially flag in-line processing issues. Short-loops are increasingly necessary for characterization. Data mining can assist in finding yield limiting issues at a Fab by establishing the connections between the final device performance and the e-test characterization, as well as defectivity. Data mining can be used to find actionable items to correct yield or process issues across a wide range of product types and processes.

Biography:

Dr. Andy Skumanich is the Senior Technologist at Applied Materials (Santa Clara CA). He has been active in the fields of yield analysis as well as process diagnostics and control. He was a consultant for thin film and semiconductor analysis and was awarded a contract to develop a unique metrology system with Lockheed-Martin. Previously, he worked at KLA-Tencor on advanced technology for optical and electron beam inspection. Before KLA, he was a staff scientist at IBM Research working on semiconducting thin films. Skumanich has authored papers on yield enhancement, defect reduction, and process diagnostics in addition to novel materials, and metrology techniques. He holds several patents. A Hertz Foundation Fellow, he received his PhD in Physics from the University of California at Berkeley for work on optical and electronic properties of amorphous semiconducting thin films.

12:30 Lunch

1:45 Latchup Characterization in CMOS Technologies -

Robert Ashton, *Agere Systems, Orlando, FL*

Summary:

The fundamentals of latchup in CMOS technologies will be introduced. Test structures to characterize latchup will be presented and the basic measurements that can be made on them will be described, including holding voltage, holding current, and DC and transient triggering conditions. Measurement of latchup on full integrated circuits, including transient latchup, will also be covered.

Biography:

Robert Ashton is a Distinguished Member of Technical Staff in the Silicon and Interconnect Technology Laboratory of Agere Systems. Dr. Ashton received his B. S. and Ph.D. from the University of Rhode Island in Physics and did post doctoral positions at Rutgers University and Ohio State University. He then joined AT&T Bell Laboratories, which later became Bell Laboratories, Lucent Technologies before Agere Systems was spun off from Lucent Technologies. Since joining industry Dr. Ashton has been involved in CMOS technology integration and characterization, test structure design, and evaluation of technologies for ESD robustness. He is a member of the ICMTS Technical and Steering Committees. He is also a member of the IEEE Electron Device Society and the Electrostatic Discharge Association and has been a member of the Technical Committee of the Electrical Overstress and Electrostatic Discharge Symposium.

2:30 RF Modelling of MOSFETs - Kevin McCarthy, *UCC, Ireland* and Dirk B. M. Klaassen, *Philips Research, The Netherlands*

Summary:

With the continued down-scaling of CMOS technology, modern MOSFETs achieve cut-off frequencies of 20GHz and above. They can thus be selected as active devices

for the design of RF circuits especially those operating in the low GHz frequencies. Additionally, in the past decade compact MOSFET models have undergone a dramatic revolution that has seen their performance greatly improve for the prediction of analog and mixed-signal circuits.

MOSFET models must now undergo another evolution to allow the same level of accuracy to be achieved for the new application area of RF. This tutorial reviews the modeling of MOSFETs at RF and looks at the architecture and equations of some of the compact models being presently proposed for this purpose. Issues to be discussed include: intrinsic small-signal parameters; extrinsic elements such as junction and overlap capacitances; equivalent substrate networks; quasi-static and non-quasi-static operation.

Biography:

Kevin McCarthy (MIEI, MIEEE) obtained the B.E., M.Eng.Sc. and Ph.D. degrees from University College Cork (UCC), Ireland in 1982, 1986 and 1992 respectively. He is a lecturer in the Department of Electrical and Electronic Engineering, UCC, where his main teaching and research interests are communications and microelectronic devices and circuits for communications, especially in the RF and mixed-signal area. Previously, he was a senior research scientist at the National Microelectronics Research Centre, Ireland (NMRC) where he worked on the simulation of advanced MOSFET and bipolar devices for digital and analog applications with emphasis on parameter extraction and statistical analysis methodologies. Before joining UCC/NMRC he worked with Analog Devices in product engineering and CAD engineering roles. Dr. McCarthy has been a member of the Scientific Program Committee for ESSDERC 2000-2002 and is presently a member of the ICMTS Technical Program Committee.

Dirk B.M. Klaassen received the Ph.D. degree in experimental physics from the Catholic University of Nijmegen, The Netherlands, in 1982. He joined Philips Research Laboratories, Eindhoven, The Netherlands, where he has worked on various subjects in the field of luminescence from the solid state and modelling for silicon device simulation. Currently, he is involved in compact transistor modelling for circuit simulation.

3:15 Coffee Break

3:45 MOSFET Model Parameter Extraction - Colin McAndrew

Summary:

The tutorial will cover the following topics:

- **Review of basic types of MOS models**
- **MOS modeling problems, their consequences, and how to detect them**
- **Model parameters versus "physical" parameters**
- **Complete modeling flow (test structures, data, extraction, assembly, QA)**
- **Generic extraction strategy for MOS characterization**
- **What to fit: there is more to modeling than direct extraction and optimization of relative error in current**

- **Process and geometry modeling basis for statistical modeling, the advantage of models based on a small number of uncorrelated, physical parameters**
- **Statistical characterization**

Biography:

Colin McAndrew received the Ph.D. and M.A.Sc. degrees in Systems Design Engineering from the University of Waterloo, Waterloo, Ontario, Canada, in 1984 and 1982 respectively, and the B.E. degree in Electrical Engineering from Monash University, Melbourne, Victoria, Australia, in 1978. Since 1995 he has been with Motorola, Tempe AZ, and is at present Director, Enabling Technology in the Analog-Mixed Signal Technology Center. >From 1987 to 1995 he was at AT&T Bell Laboratories, Allentown PA. His work is primarily on compact and statistical modeling and characterization for circuit simulation.

4:30 Test Structures for Characterization of Parametric Mismatch and Fluctuations - Hans Tuinhout, *Philips Research, Eindhoven, The Netherlands*

Summary:

Parametric mismatch and fluctuations have received considerable attention in the recent parametric test literature and will no doubt continue to do so, as aggressive device scaling and mixed-signal system-on-chip integration are increasing the demands for good understanding and control of parametric mismatch and fluctuations. This tutorial will discuss an overview of the main requirements and challenges of characterization of parametric mismatch fluctuations. After an introduction on terminology, mismatch effects, characterization techniques and test structure requirements, the two main test structure approaches will be discussed, namely the stand-alone matched pair and the addressable array. The merits of these two types will be compared in terms of test chip area and measurement time, versus accuracy, statistical uncertainty and characterisation flexibility.

5:15 Wrap-Up and Conclusion

MONDAY, MARCH 17

8:30 a.m. - 10:00 a.m. Short Course Registration ONLY

9:00 a.m. - 5:30 p.m. Tutorial Short Course

4:00 p.m. - 8:00 p.m. Conference Registration

7:00 p.m. - 9:00 p.m. Registration Reception

TUESDAY, MARCH 18

8:00 a.m. - 9:00 a.m. Continental Breakfast

8:00 a.m. -5:00 p.m. Registration

TECHNICAL PROGRAM

8:15 a.m. - 9:00 a.m. Introduction

Conference Chair: Christopher Hess, *PDF Solutions*

Program Chair: Bill Verzi, *Agilent Technologies*

SESSION 1: CD METROLOGY

9:00 a.m. - 10:20 a.m.

Co-Chairs: Greg Yeric, *TestChip Technologies, Inc*.

Emilio Lora-Tamaya, *Universidad Autonoma de Barcelona*

9:00 Junction-Isolated Electrical Test Structure for

1.1 Critical Dimension Calibration Standards, *R.A. Allen, M.W. Cresswell and L.W. Linholm, NIST, Gaithersburg, MD*

NIST is developing single-crystal reference materials electrically isolated from the substrate by a pn junction rather than a buried insulator. Primary calibration of these reference materials is via imaging the cross-section of the feature with high-resolution transmission electron microscopy (HRTEM) at sufficient magnification to resolve and count the individual lattice plane while electrical test structure metrology techniques provide the transfer calibration.

9:20 Thermal Design Considerations for Greek

1.2 Cross Test Structures, *S. Enderling, M. Dicks, S. Smith, J. Stevenson and A. Walton, The University of Edinburgh, Edinburgh, United Kingdom*

This paper analyses the temperature rises associated with the currents forced during the measurement of a Greek cross. This was performed using Finite Element (FE) analysis software (Coventoware) which indicated that the temperature can rise by 100°C with a measurement current of 31mA. It is shown that the heating effect can be dramatically reduced by decreasing the arm length and increasing the pad size of the Greek cross. Using these new design rules currents up to 11mA can be forced through the cross structure without a significant rise in temperature. For typical metal layers this results in a measurement voltage of about 100m which is well within the capabilities of most available voltmeters.

9:40 Use of Test Structures for Characterising a

1.3 Novel Photsensitive Organometallic Material for MOS Process, *M. Dicks, G. Broxton*, J. Thomson*, J. Lobban*, A. Gundlach, J. Stevenson and A. Walton, , University of Edinburgh, Edinburgh, United Kingdom, *University of Dundee, Dundee, United Kingdom*

A novel process is presented that produces platinum features using direct UV exposure of a photosensitive organometallic material. The deposited films are

metallic and have a good adhesion to silicon dioxide. A test chip with MOS capacitors and sheet resistance structures fabricated using the new organometallic material has been characterised.

10:00 An Electrical Monitor of Deep Trench Depth,

1.4 ***T. Roggenbauer, V. Khemka, V. Parthasarathy, I. Puchades and R. Zhu, Motorola SPS, Chandler, AZ***

A novel, non-destructive measurement technique has been used to electrically monitor the depth of a deep trench in a submicron smart power process. The ratio of the injected emitter current to the captured collector current in a parasitic bipolar transistor has demonstrated the ability to resolve variations in trench depth of <0.2m and was used to qualify a new etch process.

10:20 a.m. - 10:50 a.m. Break

SESSION 2: MEMS AND SENSORS

10:50 a.m. - 12:10 p.m.

Co-Chairs: Willy Sansen, *KU Leuven*

Giovanni Soncini, *University of Trento/ IRST*

10:50 Influence of Masking Layer Stress on

2.1 Isotropic Silicon Etching in TMAH Solutions,*M. Decarli, V. Guarnieri*, R. Pal, F. Giacomozzi*, B. Margesin* and M. Zen*, ITC-IRST, Povo, Trento, Italy, *University of Trento, Povo, Trento, Italy*

Nowadays MEMS device fabrication requires an accurate knowledge of the silicon etching parameters. We studied the relation between thin film masking layers residual stress and the orientation dependence of the silicon etching rate using TMAH solutions. In particular we focused on widely used masking films such as SiO2 and Si3N4. Dedicated test structures were designed, fabricated and tested. We found an influence of the masking layer residual stress on the silicon etching rate anisotropy and a lower value of anisotropy for higher stressed structures.

11:10 Test Structures for Quantum Efficiency

2.2 Characterization for Silicon Image Sensors,

F. Odiot, J. Bonnouvrier, C. Augier and J.M. Raynor*, ST Microelectronics, Crolles, France and *ST Microelectronics, Edinburgh, United Kingdom

The quantum efficiency (QE) is an important parameter to characterize the sensitivity of the pixel in imager applications. This parameter depends on the design, of the technology and of the process. To study the spectral response, test structures are specially designed. This paper presents quantum efficiency results for different kind of Nwell / Pepi diodes. A comparison is

made between a diode under active and under STI with or without salicidation. The impact of the design (different Nwell geometries) and two reading nodes (CMOS and NMOS) are also studied. These measurements are then compared with the ISE simulation using a 2D simulation program DIOS.

11:30 Evaluation of Mechanical Properties by

2.3 Electrostatic Loading of Polycrystalline Silicon

Beams, *R. Cambie, F. Carli and C. Combi*, University of Pavia, Italy, *STMicroelectronics, Milan, Italy*

Different structural elements are designed to obtain reliable estimates of the failure stress and of the normal modulus of elasticity for usual component material of MEMS. At that purpose a capacitive micro-motor has been produced using a THELMA process for growing thick film (15m) of epitaxial polycrystalline silicon. Digital imaging of the designed test structures during the step-by-step actuation allows the evaluation of the failure stress in bending, of the Young?s modulus and the identification of the stress-strain law of bulk material until failure.

11:50 Process Stress Estimation for MEMS RF

2.4 Switches with Capacitive Test Structures

L. Ferrario, C. Armaroli, B. Margesin, M. Zen and G. Soncini, ITC-irst, Povo, Italy

One of the basic parameters in RF capacitive switches is the actuation voltage. It strongly depends on the process stress accumulated in the switching structure, typically a suspended thin bridge, made of conductive materials. The control and the tuning of the deposition steps require the monitoring and the reduction of the process stress. We present a method to accurately simulate the global process stress of the device taking advantage of the electrical characterization done on standard capacitive test structures integrated in the process layout.

12:10 p.m. - 1:40 p.m. Luncheon (DeAnza 2)

SESSION 3: YIELD

1:40 p.m. - 3:20 p.m.

Co-Chairs: Akella Satya, *KLA-Tencor Corp.*

Naoki Kasai, *SELETE*

1:40 An Advanced Defect-Monitoring Test Structure

3.1 for Electrical Measurements and Defect Localization, *Y. Hamamura, K. Tsunokuni, A. Sugimoto, H. Asakura and T. Kumazawa, Hitachi, Ltd., Atlanta, GA*

We present a new test structure that enables detecting short and open failures in the intra-layer wiring process to improve yield. An open-monitoring element (OME) in the 1st metal layer is meandering around lines of short-monitoring elements (SME) placed in contact with N-type diffusion regions to make the structure compact. Defective test structures can be screened through electrical measurements, and also, killer defects can be localized by using a voltage contrast method or an optical microscopic method.

2:00 Development of a Large-Scale TEG for

3.2 Evaluation and Analysis of Yield and Variation,

M. Yamamoto, H. Endo* and H. Masuda, Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan, *Hitachi ULSI Systems Co., Ltd., Tokyo, Japan

We have first developed the new TEG (Test Element Group) that has large-scale patterns which compare well to those of an SoC and has 4-corner address decoders. This TEG is based on the design rules of pure processes that are independent of the products. We have successfully measured pure process yield, failure terms, and failure locations and evaluated characteristic variation in a chip. Stress tests were implemented. With use of the electrical dimension measurement, charge-up damage, and analysis database software, this new TEG will become to be a strategic technology.

2:20 An Integrated Test Chip for the Complete

3.3 Characterization and Monitoring of a 0.25um CMOS Technology that fits into Five Scribe Line Structures 150um by 5,000um, *R. Lefferts and C. Jakubiec, Accelerant Networks, Beaverton, OR*

A test chip containing 340 different test devices was integrated into 5 scribe line test structures each with 14 probe pads. Up to 75 MOS devices were integrated into a single structure using an on-chip switching technique that preserved a noise floor of 10 pAmps. One row contains 50 CV structures and 4 ring oscillators also using 14 probe pads. This test chip was used to completely characterize a 0.25um Mixed Signal CMOS technology.

2:40 Test Time Reduction Methods for Yield Test

3.4 Structures, *C. Hess, H. Read, L. Weiland, J. Cheng*, C. Gan*, H. Karbasi* and S. Winters*, PDF Solutions, San Jose, CA, *PDF Solutions, San Diego, CA*

Complexity of integrated circuits has led to hundreds of millions of transistors, wiring lines, and layer to layer via connections on every chip. To allow accurate yield evaluation, it is required that process characterization test chips grow in complexity as well which has let to a significant bottleneck in testing them. Wafers that could be tested in less than two hours in a 0.35um technology now require 10 hours and more in a 0.13um technology. This paper will present methods how test structures can be redesigned to

better support testing. Based on those we will present modified test algorithms that will significantly reduce the test time by 50% and more, which will accelerate data analysis and increases efficient use of parametric test systems.

3:00 Analysis and Characterization of Device

3.5 Variation in an LSI Chip Using an Integrated Device Matrix Array, *S.-I. Ohkawa, M. Aoki and H. Masuda, Semiconductor Technology Academic Research Center (STARC), Yokohama, Japan*

For future LSI design technology, the Device Matrix Array (DMA), which precisely evaluates the variation of device parameters within a die, has been developed. The DMA consists of common units (14 x 14 arrayed with 240um pitch), each containing 148 elements of transistors (Tr), resistors (R), capacitors (C) and ring-oscillators. The leakage reduction circuits and hierarchical bus architectures enable to obtain the measurement accuracy of 90pA(Tr), 11m(R) and 23aF(C) in 3ó range and the spatial resolution of 240 um in the 4mm x 4mm area of the test chip fabricated by 0.13um-CMOS process.

3:20 p.m. - 3:50 p.m. Break

SESSION 4: POSTER SESSION

3:50 p.m. - 4:20 p.m.

Co-Chairs: Anthony Walton, *University of Edinburgh*

Takashi Ohzone, *Toyama Prefectural University*

4.1 A Combined Test Structure with Ring Oscillator

and Inverter Chain for Evaluating Optimum High-Speed/Low-Power Operation, *T. Matsuda, H. Iwata, T. Ohzone, S. Odanaka*, K. Yamashita, N. Koike** and K. Tatsuuma**, , Toyama Prefectural University, Toyama, Japan, *Osaka University, Osaka, Japan, **Matsushita Electric Ind. Co., Ltd., Kyoto, Japan***

A test structure combined with a ring oscillator, an inverter chain and an embedded monitor inverter, which allows accurate internal node access, is proposed. Vdd and well-bias dependence of gate delay and supply current measured by both ring oscillator and inverter chain scheme. VT control method by well biasing, particularly to forward direction, is effective for high speed operation under low supply voltage The new test structure can be utilized to evaluate optimum conditions for high-speed/low-power operations as well as high-reliability operations.

4.2 Scalable Ground-Shielded Open-Fixture

Applied to De-Embedding Techniques, *T. Kaija and E. Ristolainen, Tempere University, Tempere, Finland*

A new way to scale ground-shielded open-fixture is presented in this paper. Scalable open-fixture saves die space, since only one open-fixture is needed to carry out de-embedding with different sized DUTs. Furthermore, the distance between two probe-tips can be kept constant, which makes the measurements simpler. The validity of this new scaling method is verified through measurements and applying it to commonly used de-embedding methods on a frequency range from 45 MHz to 20 GHz. Several fixtures were fabricated using 0.35mm CMOS process.

4.3 Evaluation of Mobility in the MOSFET with High

Leakage Current, *O. Tonomura, Y. Shimamoto, S. Saito, K. Torii, H. Miki, M. Hiratani and J. Yugami, Hitachi, Ltd., Tokyo, Japan*

We applied a transmission-line circuit model to MOSFETs with a high gate leakage current, and measured the mobility precisely. The model was verified by a frequency dependence of the capacitance. We found that the channel length should be short to suppress the voltage drop along the channel. The obtained mobility of MOSFETs with a 1.5-nm-thick gate oxide agreed well with theoretical calculations.

4.4 Automatic, Wafer-Level, Low-Frequency Noise

Measurements for the Interface Slow Trap Density Evaluation, *J.A. Chroboczek, CEA-LETI, Grenoble, France*

A system for automatic, wafer-level, low-frequency current fluctuations measurements on semiconductor devices, involving a novel, programmable, biasing current amplifier is presented. A procedure for the current amplifier calibration by thermal noise is given. LFN results on MOSFETs with HfO2 gate dielectric were used for extracting the slow-trap density at the Si/dielectric interface. The method?s potential for repetitive device testing is discussed.

4.5 Reliable Extraction of Interface States from

Charge Pumping Method in Ultra-Thin Gate Oxide MOSFET's, *H.C. Lai, N.K. Zous, W.J. Tsai, T.C. Lu, T. Wang, Y.C. King* and S. Pan, Macronix International Co., Ltd., Hsinchu, Taiwan, ROC, *National Tsing Hua University*

The accuracy and validity of charge pumping (CP) method is questionable in ultra-thin gate oxide MOSFET?s due to the increase of the direct tunneling currents at low gate biases. A gate pulsing window for the CP technique is proposed to reduce the influence of this parasitic leakage current effect. Within the window, the CP method is still an excellent tool to measure the average interface trap density. Moreover, the range of this window strongly depends on the gate oxide thickness and the channel length.

4.6 Design and Integration of Electrical-based

Dimensional Process-Window Checking Infrastructure, *K.Y.Y. Doong, R.C.J. Wang, J.C.H. Huang*, S.C. Lin, L.J. Hung, S. Z. Lee, and K.L.Young, Taiwan Semiconductor Manufacturing Corp. Shinchu, Taiwan and *Silicon Canvas Inc., San Jose, CA*

The purpose of this work is to provide a design infrastructure for electrical-based dimensional process-window checking. With the aid of the novel test vehicle design platform, the discrepancy among design rule set, test structure design and testing plan can be minimized. Using the function-independent Test Structure Design Intellectual Properties (TSD-IP) provided by this infrastructure, the process-window could be quantified as the electrical testing of test structures. A cross-generation (130nm-90nm) test vehicle which focus on the evaluation of overlay and critical dimension variation cross the intra- and inter-photo field is enacted to demonstrate the design framework.

4:20 p.m. - 5:30 p.m. RECEPTION/POSTER DISPLAY

WEDNESDAY, MARCH 19

8:00 a.m. - 9:00 a.m. Continental Breakfast

8:00 a.m. - 5:00 p.m. Registration

SESSION 5: RF

9:00 a.m. - 10:20 a.m.

Co-Chairs: Alessandra di Paola, *Agilent Technologies*

Yoshi Hagiwara, *Sony Corp.*

9:00 Application of the TRM Self-Calibration on

5.1 Standard Silicon Substrates, *R. Gillon, W. Tatinian and B. Landat, AMI Semiconductors bvba, Oudenaarde, Belgium*

This paper reports the application of the TRM self-calibration technique for the de-embedding of on-wafer measurements on bulk-silicon substrates, for the first time. Two major issues that historically prevented this, have been identified and solved. The new procedure is duly validated by comparison with the already established in-situ TRL calibration. It remedies to the bandwidth limitation of TRL, still keeping the flexibility for moving reference planes.

9:20 Optimisation of Integrated RF Varactors on a

5.2 0.35m BiCMOS Technology, *S. Kelly, J. Power, M. O'Neill, Analog Devices, Limerick, Ireland*

Integrated varactors are becoming a common feature for many RF designs and in particular RF voltage controlled oscillators (VCOs). Optimisation of the quality of both the inductor and the varactor from the VCO core is essential. This work details the characterisation and optimisation of a number of varactor types available on a typical submicron BiCMOS process. Engineering of the bottom plate of the varactor was used to optimise the quality factor of the varactor. Integrated isolated diode varactors with quality factors of 30 at 2 GHz have been demonstrated with tuning capacitance ranges of 2.5. Integrated MOS capacitor varactors with quality factors of 50 at 2 GHz have been demonstrated with tuning capacitance range of 5.

9:40 BSIM3 RF Models for MOS Transistors: A

5.3 Novel Technique for Substrate Network

Extraction, *S. Rustagi, H. Liao, J. Shi and Y. Xiong, Institute of Microelectronics, Singapore*

A novel technique of extraction of the extrinsic components of the MOS transistor equivalent circuit based on BSIM3v3 core is reported. RF measurements from the common gate configuration of the MOS transistor in 'off-state' along with the normal common source configuration are used. Physically consistent values of the different resistance in the substrate network as well as the capacitance between source and drain due to fringing can be accurately estimated. The extracted model represents the large signal behaviour of the device very well.

10:00 Substrate Resistance Modeling for Noise

5.4 Coupling Analysis, *S. Kristiansson, S.P. Kagganti, T. Ewert, F. Ingvarson, J. Olsson and K.O. Jeppson*

A new semi-empirical model for the resistance between two contacts on a semiconductor substrate is presented. The model was tested on measurement data obtained from a set of test structures in a CMOS process. The model accurately describes the observed initial increase in resistance followed by the observed saturation as the contact separation increases. An example of noise coupling analysis where the new model is utilized is also presented.

10:20 a.m. - 10:50 a.m. Break

SESSION 6: Parameter Extraction

10:50 a.m. - 12:10 p.m.

Co-Chairs: Hans Tuinhout, *Philips Research*

Colin McAndrew, *Motorola*

10:50 New Technique to Extract Intrinsic and

6.1 Intrinsic Base-Collector Capacitances of Bipolar Transistors Using Y-Parameter Equations, ***S. Lee, Hankuk University of Foreign Studies, Yongin, Kyungki-do, Korea***

A new method utilizing the frequency-response of Y-parameter equations is developed to extract intrinsic and extrinsic base-collector capacitances of bipolar transistors independently, without any extraction of the base resistance and total base-collector capacitance. The sum of extracted intrinsic and extrinsic base-collector capacitances agrees well with the total base-collector capacitance obtained from the conventional method, verifying the accuracy of the new one.

11:10 Impact of Gate Current on First Order

6.2 Parameter Extraction in Sub-0.1um CMOS Technologies, ***N. Planes and H. Brut, STMicroelectronics, Crolles, France***

The impact of the gate leakage current on long MOS transistor characterization is investigated in this paper. Particularly for first order parameters extraction, a new method is proposed here to rid the gate current on advanced technologies with thin gate oxides. By demonstrating experimentally a 50/50 partition of the gate current between source and drain nodes in linear and in strong inversion regimes, the intrinsic channel current of the MOS transistor can be isolated. The proposed methodology then allows the extraction of first order parameter in case of large area devices strongly suffering from gate leakage, and also permits to extract these parameters in a more consistent way whatever the cases. Moreover, the extraction error on channel parameters that can be induced by the gate leakage current is discussed varying oxide thickness and channel length.

11:30 A Hybrid Table/Analytical Approach to MOSFET

6.3 Modeling, ***V. Bourenkov, K. McCarthy and A. Mathewson, University College Cork, Ireland***

In this paper, a new simple and accurate hybrid table/analytical model of the MOSFET drain current based on the interpolation of table parameters is proposed. The model has been implemented in the SPICE3f5 circuit simulator and performs well in DC simulations. This new hybrid table model has an accuracy similar to the well known BSIM3v3.2 model but requires no complex parameter extraction, and uses less memory for data storage than a fine-grid table model.

11:50 An Improved SPICE Model for Liquid Crystal on

6.4 Silicon Microdisplays, ***S. Smith, A. Walton, I. Underwood, C. Miremont, D. Vass, W. Hossack, M. Birch, A. Macartney and R. Nicol, The University of Edinburgh, Edinburgh, United Kingdom***

This paper presents the development of SPICE equivalent circuits for the electrical and optical modeling of ferroelectric liquid crystal on silicon devices. An electro-optical model has been evaluated in a previous publication and although it can simulate the optical output from a display cell it does not accurately model the drive current required to switch the LC material from one state to the other. A new SPICE model has been developed and the results of optimising this to fit electrical measurement data are presented.

12:10 p.m. - 1:40 p.m. Awards Luncheon (DeAnza 3)

SESSION 7: RELIABILITY

1:40 p.m. - 3:00 p.m.

Chair: Michael Cresswell, *NIST*

1:40 Polysilicon Resistive Heated Scribe Lane Test

7.1 Structure for Productive Wafer Level Reliability Monitoring of NBTI, *W. Muth, A. Martin, J. von Hagen, D. Smeets and J. Fazekas, Infineon Technologies AG, Munich, Germany*

A polysilicon resitive heated structure was designed with a P-MOS-FET embedded between two polysilicon heater stripes. A 4-terminal metal resistor upon the heaters allows temperature control via the temperature coefficient of the resistance. A stress algorithm allows simultaneous thermal and electrical stress. The real device temperature is gained by a comparison of the temperature measured at the metal level and the pn-junction temperature measured by the forward diode characteristics. Negative Bias Temperature Instability stress results from this structure are presented.

2:00 Test Structure and Verification on the MOSFET

7.2 under Bond Pad for Area-Efficient I/O Layout in High-Pin-Count SOC IC's, *M.-D. Ker, J.-J. Peng* and H.-C. Jiang, National Chiao-Tung University, Hsinchu, Taiwan, ROC, *Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, ROC*

To save layout area for ESD protection design in the SOC era, test chip with active devices placed under bond pads has been fabricated for verification. The bond pads had been drawn with different layout patterns on the inter-layer metals to investigate the impact of bonding stress on the active devices under the pads. The measurement results, including thermal shock and temperature cycling tests, show that there are only little variations between devices under bond pads and devices beside bond pads. This discovery can be applied to save layout area for on-chip ESD protection devices or I/O devices of IC products, especially when the IC?s are designed with high pin counts.

2:20 Test Structures and Test Methodology for

7.3 Developing High Voltage ESD Protection, *A. Concannon, V. Vaschenko, M. Terbeek and P. Hopper, National Semiconductor Corporation, Santa Clara, CA*

In this work, new test structures and a test methodology are developed to evaluate proposed ESD clamps in all modes of operation. TCAD analysis is used to identify possible ESD clamp structures. Standard ESD testing is used to screen the ESD capability of the candidate clamps. Transmission line pulse technique is used to evaluate the dynamic triggering characteristics of a snapback based clamp, and select an appropriate clamp for fast switching applications. Finally, a very efficient local ESD clamp based on a bipolar-silicon controlled rectifier in a 24V Complementary Power BiCMOS process is presented

2:40 New Evaluation Method for Reliability of Poly-Si

7.4 Thin Film Transistors using Pico-Second Time-Resolved Emission Microscope, *Y. Uraoka, N. Hirai*, H. Yano, T. Hatayama and T. Fuyuki, Nara Institute of Science and Technology, Nara, Japan, *Hamamatsu Photonics, Nara, Japan*

New evaluation method for reliability in low-temperature poly-Si thin film transistors was proposed. We have analyzed degradation of n-ch TFT under dynamic stress using pico-second time-resolved emission microscope. We have successfully detected emission at pulse fall edge for the first time. Further we have also obtained hot electron current during the pulse fall using the device simulation considering transient effect. Comparison between transient emission and the theoretical hot carrier current suggested that degradation occurs during the pulse fall.

3:00 p.m. - 3:30 p.m. Break

SESSION 8: CAPACITANCE

3:30 p.m. - 4:50 p.m.

Chair: Alexander Rahm, *Siemens AG*

3:30 Test Structure Design Considerations for RF-

8.1 CV Measurements on Leaky Dielectrincs, *J. Schmitz, F. Cubaynes, R. de Kort*, R. Havens* and L. Tiemeijer*, Philips Research Leuven, Leuven, Belgium, *Philips Research Laboratories, Eindhoven, The Netherlands*

We present Capacitance-Voltage measurements on MOS capacitors with ultra-thin, high-leakage gate dielectrics. The characterization problems associated with high leakage are effectively overcome using RF measurements. Capacitance-Voltage measurements are proven to be feasible in the entire range of accumulation, depletion and inversion, even when the leakage current density exceeds 1 kA/cm2. On the basis of our findings, test structure design guidelines are formulated.

3:50 Fast and Precise Subthreshold Slop Method for

8.2 Extracting Gate Capacitive Coupling Coefficient in Flash Memory Cells, *C. Cho, M.-J. Chen and C.-F. Chen*, National Chiao-Tung University, Hsinchu, Taiwan, ROC, *Actrans Systems, Inc., Santa Clara, CA*

A fast and precise subthreshold slope method for extraction of gate capacitive coupling coefficient is confirmed by the data from stack gate flash memory cells and split-gate ones. This new method furnishes promising potentials: (1) it can eliminate the effect of process variations and the effect of source or drain capacitive coupling measurement; and (2) a few measurements are needed and even dummy transistors can be removed out. The method is thereby suitable as an in-line process monitor.

4:10 Series Resistance Estimation and C(V)

8.3 Measurements on Ultra Thin Oxide MOS Capacitors, *D. Rideau, D. Roy, G. Gouget, P. Scheer, M. Minondo and A. Juge, STMicroelectronics, Crolles, France*

Based on extensive measurements on test structures, with varying physical silicon oxide thicknesses (from 21Å to 13Å) and areas (from 27000mm2 to 4mm2), this paper describes the effect of gate current on capacitance measurement using standard 10kHz-to-1MHz LCR-meter.

4:30 The Negative Capacitance Effect on the C-V

8.4 Measurement of Ultra Thin Gate Dielectrics Induced by the Stray Capacitance of the Measurement System, *Y. Okawa, H. Norimatsu, H. Suto* and M. Takayanagi*, Agilent Technologies Japan, Ltd., Tokyo, Japan, *Toshiba Corporation, Yokohama, Japan*

We clarified that an anomalous inductive effect or "Negative-Capacitance Effect" observed on the C-V measurement of the ultra thin gate dielectrics is induced by the parasitic component originate from the wafer chuck even if the calibration is executed appropriately at the tip of the probe needle. Also we propose the new methodology for the on-wafer C-V measurement reduces inductive effect induced by system parasitic for wider frequency rage over 100MHz.

6:00 p.m. Conference Banquet at the Monterey Aquarium

THURSDAY, MARCH 20

8:00 a.m. - 9:00 a.m. Continental Breakfast

8:00 a.m. - 5:00 p.m. Registration

SESSION 9: PROCESS CHARACTERIZATION

9:00 a.m. - 10:00 a.m.

Co-chairs: Robert Ashton, *Agere Systems*

Charles Alcorn, *BAE Systems*

9:00 Study on STI Mechanical Stress Induced

9.1 Variations on 90nm CMOSFETs, *Y.M. Sheu, K. Doong, C.H. Lee, M.J. Chen* and C.H. Diaz, Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan, ROC, *National Chiao-Tung University, Hsin-Chu, Taiwan, ROC*

Impact of STI mechanical stress on MOSFET drive current was investigated by a full-matrix active area layout experiment in 90nm technology node. This work specifically shows that transistor drive current density per unit width is not independent of the active area size; particularly along the direction of the channel current flow. Opposite sensitivities are observed between n/pMOSFETs with respect to lateral active area size. Furthermore, this work shows drive current sensitivity to both active area size and gate placement inside the active area. A modified principal component analysis was used in this study.

9:20 Test Structures for Analyzing Mechanisms of

9.2 Wafer Chemical Contaminant Removal, *J. Yan, H.J. Barnaby, B. Vermiere*, T. Peterson and F. Shadman, University of Arizona, Tucson, AZ, *Ridgetop Group, Inc., Tucson, AZ*

Deep trenches are currently an integral part of both front-end processes (deep trench isolation) and back-end processes (multi-layer metal interconnect). One of the major problems encountered by technologies that utilize deep trenches is the difficulty in monitoring the efficacy of surface preparation and cleaning of the lower levels of the trench. Considering that nearly one third of the steps in a typical fabrication process are associated with wafer cleaning, this step has a serious impact on the productivity of the semiconductor industry. Therefore, it is very important to understand the mechanisms associated with contaminants in deep trenches. The test structure introduced in this paper is an electrochemical sensor that facilitates the identification and analysis of these mechanisms.

9:40 Measuring the Effects of Process Variations on

9.3 Circuit Performance by Means of Digitally-Controllable Ring Oscillators, *A. Bassi, A. Veggetti*, L. Croce* and A. Bogliolo, University di Ferrara, Ferrara, Italy, *ST Microelectronics, Agrate Brianza, Italy, **Universita di Urbino, Urbino, Italy***

We present a test chip for the direct measure of the effects of inter/intra-chip process variations on the performance of CMOS circuits. The test structure is a ring oscillator made of modified CMOS inverters that may exhibit two slightly different delays depending on the value of a digital control signal. The incremental delay of each cell is measured from the oscillation periods

obtained with different configurations of the control bits. Results are reported for a corner lot a 0.18mm process.

10:00 a.m. - 10:30 a.m. Break

SESSION 10: MATCHING

10:30 a.m. - 12:10 p.m.

Chair: Anthony Walton, *University of Edinburgh*

10:30 Test Structures for Studying Adjacent Layout

10.1 Effects on Current Mirror Mismatch, *H.P. Tuinhout, A. Bretveld* and W.C.M. Peters, Philips Research Laboratories, Eindhoven, The Netherlands, *Philips Consumer Electronics, Eindhoven, The Netherlands, **Philips Semiconductors Process Development, Nijmegen, The Netherlands***

This paper discusses a new current mirror based test structure, used to identify and quantify systematic mismatch degradation associated with layout features close to high precision current mirror transistors. This type of study provides invaluable insights into possible performance degradation of the common current mirror, one of the most often used elementary building blocks in any CMOS or BiCMOS mixed signal system.

10:50 A Test Circuit for Measuring MOSFET

10.2 Threshold Voltage Mismatch, *K. Terada and M. Eimitsu, Hiroshima City University, Hiroshima, Japan*

A new test circuit is proposed for evaluating MOSFET threshold voltage mismatch. This test circuit consists of many parallel-connected cells, in which two MOSFETs are serially-connected to each other and the node between them is connected to common wiring through a switch. The threshold voltage mismatch is derived from the DC currents flowing through this test circuit.

11:10 Improvement of Poly Emitter n-p-n Transistor

10.3 Matching in a 0.6 Micron Mixed Signal Technology, *G. Lau, X-FAB Semiconductor Foundries AG, Erfurt, Germany*

Standard high frequency n-p-n poly emitter transistor pairs show a significant parameter offset depending on the position on the wafer. The main reason for this offset is an non-uniform development process of the resist mask for the emitter cut etch. By the use of a new development process and area optimized dummy structures the matching performance could be improved. As a "byproduct" the bipolar transistor parameter variation across the wafer also could be noticeable reduced.

11:30 Characterization and Modeling of MOSFET

10.4 Mismatch of a Deep Submicron Technology, ***M. Quarantelli, S. Saxena, N. Dragone, J. Babcock, C. Hess, S. Minehane, S. Winters, J. Chen, H. Karbasi and C. Guardiani, PDF Solutions, Richardson, TX***

This paper compares two common approaches for estimating mismatch: a) pooling mismatch measurements from a number of die across a wafer and from multiple wafers to get mismatch statistics, and b) the use of arrays to get a large sample of measurements from a single die. Measurements taken from a 0.13 um technology illustrate the inaccuracies that result from the use of pooled measurements to estimate mismatch statistics. Use of arrays shows that *1/sqrt(WL)* relationship holds for Idsat mismatch even for very small devices sizes. In addition, in this technology the impact of distance on mismatch appears to be negligible for the range of distances covered by a single array.

11:50 Impact of Grain Number Fluctuations in the

MOS Transistor Gate on Matching Performance, ***R. Difrenza, J.C. Vildeuil, P. Llinares and G. Ghibaudo*, STMicroelectronics, Crolles, France, *IMEP, Grenoble, France***

This paper presents a compact model for the gate impact on MOS transistor matching. It is based on the random variations of grain number in the polycristalline gate. The model is validated by fitting mismatch increase with substrate bias. This study highlights the importance of local polysilicon depletion and gives a better understanding of complex mechanisms that are responsible for MOSFET mismatch.

CONFERENCE COMMITTEE

GENERAL CHAIR

Christopher Hess
PDF Solutions, Inc.
333 W. San Carlos Street
Suite 1200
San Jose, CA

TECHNICAL PROGRAM CHAIR

Bill Verzi
Agilent Technologies
5114 Balcones Woods Drive
Suite 307, ATTN: PMB 328
Austin, Texas 78759 USA

TUTORIAL CHAIR

Larg Weiland
PDF Solutions, Inc.

333 W. San Carlos Street
Suite 1200
San Jose, CA

EXHIBIT CHAIR

Jim Reedholm
Reedholm Instruments
Four Sierra Way
Georgetown, TX 78626

U.S REPRESENTATIVE

Loren W. Linholm
NIST
Tech Bldg, B-360
Gaithersburg, MD 20899

ASIAN REPRESENTATIVE

Takashi Ohzone
Toyama Prefectural University
Kurokawa, Kosugi Machi
Imizu-Gun
Toyama 939-03, Japan

EUROPEAN REPRESENTATIVE

Anthony A.J. Walton
Dept. Electrical Engineering
University of Edinburgh
Kings Buildings
Edinburgh EH9 3JL, Scotland

TECHNICAL PROGRAM COMMITTEE

Charles N. Alcorn
BAE Systems
Manassas, VA

Robert Ashton
Agere Systems
Orlando, FL

Michael W Cresswell
NIST
Gaithersburg, MD

Gerard Ghibaudo
LPCS/ENSERG

Grenoble, France

Satoshi Habu
Agilent Technologies Japan, Ltd.
Tokyo, Japan

Yoshiaki Hagiwara
Sony Corp.
Atsugi, Japan

Hiroaki Hazama
Toshiba Corp.
Mie, Japan

Kazunari Honma
Sanyo Electric Co.
Gifu, Japan

Kjell O Jeppson
Chalmers University of Technology
Goteborg, Sweden

Naoki Kasai
SELETE
Ibaraki, Japan

Akio Kawamura
Sharp Corp.
Hiroshima, Japan

Junko Komori
Mitsubishi Electric Co.
Hyogo, Japan

Jun Kudo
Sharp Corp.
Nara, Japan

Emilio Lora-Tamayo
Universidad Autonoma de Barcelona
Barcelona, Spain

Alan Mathewson
NMRC
Cork, Ireland

Colin McAndrew
Motorola

Kevin McCarthy
University College
Cork, Ireland