**International Conference on Microelectronic Test Structures (ICMTS) 2002**

**April 8-11, Cork, Ireland**

ICMTS2002 will be held in Cork which is a small but vibrant city on the south coast of Ireland. It has a population of around 200,000 of which 30,000 are students at one of the many institutes of education in the city (http://www.cork-guide.ie/corkcity.htm). Cork has recently been selected by the European Parliament as European Capital of Culture for 2005, an accolade which reflects the high levels of cultural and entertainment activities in the city.

## Registration Information

# Conference Registration form
# Hotel registration form

## Technical committee

## Contact information

### Chairman's Letter

Dear Colleagues,
On behalf of the committee, I welcome you to the 2002 International Conference on Microelectronic Test Structures (ICMTS 2002) in Cork, Ireland. This is the 15th ICMTS to be held as an international conference and the 1st one to be held in Ireland. The conference is sponsored by the IEEE Electron Devices Society and hosted by University College Cork.
The purpose of the conference is to bring together designers and users of test structures to discuss recent developments and future directions. This year's conference consists of 44 papers in 9 oral sessions and 1 poster session. Session topics will include *Lithography, RF Characterisation and Modelling, Process Characterisation, Parameter Extraction, Non-Volatile Memory Characterisation* and *Modelling, Interconnect, Yield and Reliability, MEMs and Photonics and Matching.* Oral presentations are 15 minutes long with 5 minutes for questions. The poster session covering a wide variety of topics is preceded by 5 minute oral presentations by each author.
This year's conference highlights the continued importance of good test structure design for the rapid development of deep sub-micron and nano-scale devices and for the introduction of new processes and materials. We see the application of test structures to new areas such as MEMS and optical components as well as their use for high-frequency and mixed analogue/digital applications. I believe that well designed test structures will continue to provide the basis for our understanding of new technologies and for the development of good process, device and circuit models as the industry continues its journey to provide innovative, timely and cost effective IC solutions into the 21st century.
The one-day Tutorial Short Course will be held on Moday April 8th 2002. This is intended to provide participants with a good knowledge of the design and use of test structures in support of modern process and device development and modeling. The tutorial topics are: *Electrical Linewidth and Overlay, Wafer Level RF Measurements, Thin-Oxide CV Measurements and Reliability in Thin Oxides, Electrical Evaluation of SiGe Heterojunction Transistors* and *Latchup Characterization in CMOS Technologies.* The short course instructors have many years experience in these specialized and evolving topics which will facilitate a good "technology transfer" to the course participants.
During the conference, there will be an equipment exhibition of the latest developments in test equipment for test structure measurement and analysis.
Cork is a small but vibrant city on the south coast of Ireland with a population of around 200,000. It has a long history, originating as a monastic settlement in the early seventh century. Later, its deep harbour allowed the city to became a major trading port and a strategic naval base. Cork has recently been selected by the European Parliament as European Capital of Culture for 2005, an accolade which reflects the high levels of social and cultural activity in the city.
May I take this opportunity to wish you a successful and enjoyable conference. I hope that it will allow you to gain new technical knowledge and an insight into Irish culture as well as being the beginning of many new and fruitful friendships.
Sincerely,
Alan Mathewson
General Chairman

### Getting to Cork

**By Air**

There are frequent flights between Cork airport and Dublin and London with Aer Lingus (www.aerlingus.ie) (Heathrow and Gatwick) and RyanAir (www.ryanair.ie) (Stanstead), and other airlines. There are also frequent flights to other UK and European destinations. Visitors to Cork from outside Europe usually need to travel through Dublin or London.A list flights into Irish airports is provided on the Irish Airport Authority's web site ( Aer Rianta - www.aer-rianta.ie ).

**By Ferry**

Swansea-Cork Ferries (www.swansea-cork.ie) have a direct ferry daily between Swansea (Wales) and Cork with a travel time of about nine hours.Irish ferries (www.irishferries.ie ) run ferry services between Holyhead andDublin (approx. 250km from Cork) and between Pembroke and Rosslare (approx. 180km from Cork).They also have ferries from Cherbourg and Roscoff to Roslare.Brittany Ferries (link to www.brittany-ferries.co.uk) have a weekly ferry between Roscoff and Cork with a travel time of about 14 hours.

## By Train

From Dublin (Heuston Station), there are about 8 trains daily with a journey time of about 3 hours.See Iarnrod Eireann's site (www.iarnrodeireann.ie) for timetables.Trains stop at Mallow for connections with Killarney, and at Limerick Junction for connections with Limerick (for Shannon Airport).Taxis from the railway station to the designated accommodation should cost around 10 euro.

### Getting Around in Cork

The conference venue (University College Cork), the suggested hotels and guesthouses and the city centre are all within a 15 minute walking distance of each other which should facilitate the conference delegates exploring the city and its large collection of bars and restaurants during the evenings.

## From Airport to City

Cork airport is a 15 minute drive from the city centre and a taxi will cost approximately 12 euro.

**Car Rental**
Car rental is not essential for the conference itself because of the compact nature of the city.á If you plan to spend a few days in Ireland before or after the conference and wish to hire a car, comprehensive information can be found on The Irish Tourist Board's site, www.ireland.travel.ie/home.

### City Buses

Two bus routes serve the university campus and the conference accommodation.

| Bus no. | To City Centre | From City Centre | Every |
|---|---|---|---|
| 8 | marked Lotabeg or Statue | marked Bishopstown | 1 5 mins |
| 5 | marked Mallow Road or Statue | marked Institute | 45 mins |

The no. 8 bus passes Jury's Hotel and Lancaster Lodge and the no. 5 bus passes Hayfield Manor Hotel and Brookfield Hotel/Holiday Village.

**Climate**

April temperatures in Cork range from an average low of 2oC to an average high of 12oC but like Irish weather in general, the weather in Cork is unpredictable. Visitors are advised to bring light rainwear, a wooly cap and sunglasses for luck. Before travelling consult http://weather.yahoo.com/forecast/Cork_IE_c.html for a more up to date prediction.

**Currency and Banking**

The currency in Ireland is the euro. Banks are open from 10.00-16.00 Tuesday to Friday and 10.00-17.00 on Monday. Bank of Ireland has a branch in University College Cork, adjacent to the conference venue.

**Electricity**

Electricity in Ireland is at 220 volts, 50 Hz and the electrical outlets take 3-prong square-pin plugs.

**Insurance**

While the organizing committee will make every effort to ensure the safety and well being of all participants, it cannot accept responsibility for any personal accident or loss or damage to private property of participants and accompanying guests, which may occur either during or indirectly arising from ICMTS2002.áWe recommend that delegates from EU member states carry a completed E-111 form for any emergency medical treatment.á All delegates should obtain appropriate travel insurance for their stay at ICMTS2002.

## Visa Requirements

Please consult your travel agent to determine if you need a visa to enter Ireland. The local organizing committee can provide an invitation letter if this is required for your visa application. When requesting this please give your name as it appears on your passport, the passport number and the dates (from/to) of your visit to Ireland. If you are traveling to Cork via the United Kingdom or another country, a transit visa may be required for that country. Information about visa requirements for Ireland appears in http://www.irlgov.ie/iveagh .

## Short Course

A short course on microelectronic test structures will be held on Monday 8th April 2002. The tutorial will cover a range of topics of current interest in device characterization theory and implementation. Issues to be covered are:

- Electrical Linewidth and Overlay: Loren Linholm (National Institute of Standards and Technology, Gaithersburg, Maryland)
- Wafer Level RF Measurements: William Larson/Carl Scharrer (Keithley Instruments)
- Thin oxide CV measurements/Reliability in thin oxides: Jurriaan Schmitz/Robin Degraeve (Philips Research Leuven, IMEC)
- Electrical evaluation of SiGe heterojunction transistors: Lis Nanver (DIMES, Delft University of Technology, the Netherlands)
- Latchup Characterization in CMOS Technologies: Robert Ashton (Agere Systems)

# Lecturer Biographies

**Loren W. Linholm**
Loren W. Linholm received the B.S. degree in Electrical Engineering from the University of California, Berkeley, in 1968, and the M.S. degree in Electrical Engineering from the University of Maryland, College Park, Maryland, in 1973. He has been employed by the Naval Missile Center, Point Mugu, California, and the Department of Defense, Ft. Meade, Maryland. Since 1978, he has been with the Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, Maryland, and heads the Integrated Circuits Technology Group. His research interests include the design, evaluation, and application of test structure based measurement methods for evaluating advanced integrated circuit performance, manufacturing tool control, reliability and failure analysis, and fabrication process diagnosis and control. Mr. Linholm is a fellow of the IEEE and a co-founder of the IEEE International Conference on Microelectronic Test Structures.

**William Larson**
William Larson received his M.S. degree in Materials Science from Stanford University in 1974. He has 28 years of experience in silicon process development and device modeling at Micron Technology, Ramtron, Cypress Semiconductor and is currently employed at Honeywell International in Plymouth, Minnesota. His research activities have included the development of ferroelectric memories while at Ramtron and magnetic memories (MRAM) at Honeywell. His current responsibilities are process development and device modeling of Honeywell's silicon-on-insulator (SOI) CMOS process for RF applications.

**Carl Scharrer**
Carl Scharrer is a Senior Semiconductor Industry Consultant with Keithley Instruments. His prior employment with TI, Fairchild and Motorola spanned 20 years and involved design, test and yield enhancement of high performance digital ICs.

**Lis K. Nanver**
Lis K. Nanver is professor with the Department of Information Technology and Systems, Delft University of Technology, the Netherlands. She works in DIMES in the Laboratory of Electronic Components Technology and Materials, where she heads the research on high speed silicon devices. This research is mainly directed towards optimization and development of Si bipolar and SiGe heterojunction transistors using new technologies such as RPCVD epitaxy, dopant activation by excimer laser annealing and substrate transfer techniques. The activities extend to supplying bipolar processes to designers and research on substrate modification techniques to enhance the high frequency performance of integrated passives. She is at present a program subcommittee member for the BCTM and in the past for ESSDERC.

**Jurriaan Schmitz**
Jurriaan Schmitz was born in 1967 in Elst, The Netherlands. He obtained his Ph.D. from the University of Amsterdam, NL in 1994 in experimental high-energy physics. He subsequently joined Philips Research and until 1999 worked on CMOS device scaling. He chaired the IEDM CMOS committee in 1999. His present research focus is on gate oxide characterization and reliability; and he gives technical training. He has (co)-authored over 25 papers in the field of silicon devices and holds 5 US patents.

**Robin Degraeve**
Robin Degraeve was born in Gent, Belgium in 1968. He received the M.Sc. degree in electrical engineering from the University of Gent, Belgium in 1992 and the Ph.D. degree from the Catholic University of Leuven, Belgium in 1998. He joined the Interuniversity Micro-Electronics Center (IMEC) in Leuven in the Technology Reliability and Yield group where he is currently working as a researcher. His present interests and activities include hot-carrier reliability issues in MOSFETs, the physics of degradation and breakdown phenomena in thin oxides, the reliability of ultrathin gate oxides in VLSI technologies, and the study of high-k gate dielectrics as MOSFET gate insulators for future CMOS generations.

**Robert Ashton**
Robert Ashton is a Distinguished Member of Technical Staff in the Silicon and Interconnect Technology Laboratory of Agere Systems. Dr. Ashton received his B.S. and Ph.D. degrees from the University of Rhode Island in Physics and did post doctoral positions at Rutgers University and Ohio State University. He then joined AT&T Bell Laboratories which later became Bell Laboratories, Lucent Technologies before Agere Systems was spun off from Lucent Technologies. Since joining industry Dr. Ashton has been involved in CMOS technology integration and characterization, test structure design, and evaluation of technologies for ESD robustness. He is a member of the ICMTS Technical and Steering Committees. He is also a member of the IEEE Electron Device Society and the Electrostatic Discharge Association and has been a member of the Technical Committee of the Electrical Overstress and Electrostatic Discharge Symposium.

# Banquet

The conference banquet will take place on Tuesday 10th April 2002, in JuryÆs Hotel, Western Road, Cork. One banquet ticket is included with the conference registration fees and additional tickets may be purchased as indicated on the registration form.

## Excursion

The conference ends at 12.30pm Thursday 11th April. An excursion is planned for that afternoon to The Jameson Heritage Centr, Midleton Co. Cork (http://www.cork-guide.ie/attractions/jhc.htm ) where visitors will be taken on a guided tour of an old whiskey distillery and have an opportunity to sample one of the most popular varieties of Irish whiskey. The excursion (including bus journeys to and from Midleton) will last from 2pm to 5pm. Tickets for the excursion are not included in the conference fees and must be booked separately on the registration form.

# Conference programme

## Monday 8th April 2002

**Tutorial Programme**

Boule lecture Theatre 3 (see map for location)

8.15am Registration

9.10am Opening Remarks - Johan Klootwijk, Philips Research Laboratories, The Netherlands

9.15am Electrical Linewidth and Overlay - Loren Linholm, National Institute of Standards and Technology, USA.

- Introduction
- Electrical Linewidth
- Electrical Structures:
  - van der Pauw Resistor
  - Cross-Bridge Resistor
  - Multi-Bridge Resistor
- Reference Standards
- Electrical Overlay
- Electrical Structures:
  - Differential
  - van der Pauw
  - Sliding Wire
  - MOATS
- Summary

10.05am Wafer Level RF Measurements - William Larson/Carl Scharrer, Keithley Instruments, USA.

The authors will discuss the product yield enhancement opportunity available on certain product types when wafer level s-parameter sampling is employed. Consideration will be given to the attributes of the data, test system and test structures used for this purpose. Specific discussion points will be:

- The Need for Fully Automated, On Wafer S Parameter Measurements.
- Test System Requirements for optimal data integrity.
- Extraction Techniques.
- VNA Use Characteristics.
- Considerations for Probe Selection.
- Device Layout Considerations.

10.55am Coffee Break

11.25am Electrical Evaluation of SiGe Heterojunction Transistors - Lis Nanver, DIMES, The Netherlands.

- Differences between Si BJTs and SiGe HBTs.
- Emitter-base characteristics.
- Collector-base characteristics.
- Thermal behavior.
- Cut-off frequency.
- Measurement strategy

12.15pm Lunch

2.00pm Thin Oxide C-V Measurements and Reliability in Thin Oxides - Jurriaan Schmitz, Philips Research, Belgium/Robin Degraeve, IMEC, Belgium

- Thin oxide C-V measurements:
  - Theory of MOS C-V behaviour
  - CV measurement: classical approaches
  - Impact of gate leakage
  - Leaky dielectrics: test structures and procedures
- Reliability in thin oxides:
  - Intrinsic reliability: statistics and prediction methods
  - Extrinsic reliability: measurement procedures and test structures
  - Impact of increasing leakage current on correct reliability measurements

3.10pm Coffee

3.40pm Latchup Characterization in CMOS Technologies - Robert Ashton, Agere Systems, USA.

- Introduction to Latchup.
- Test Structures for Latchup Characterization.
- Measurements on Test Structures.
- Latchup Measurement of Full ICs.

4.30pm Closing Remarks

7.00pm **Conference Welcome Reception** - Auxa Maxima (see map for location)

**TECHNICAL PROGRAM SCHEDULE**
Boule lecture Theatre 3 (see map for location)

# TUESDAY, APRIL 9, 2002

**8:00am - 5.00pm** Registration
**9:00am**Opening Remarks
**Alan Mathewson**, General Chairman
**Anthony Walton**, Technical Chairman

# SESSION 1: LITHOGRAPHY

**9:10am - 10:10am**
**Co-chairs**:**Gregory M. Yeric**, TestChip Technologies Ltd.
**Michael W. Cresswell**, NIST

**09:10 Measurement of the Linewidth of Electrical Test-Structure Reference Features by Automated Phase-Contrast Image Analysis**
*B.A. am Ende, M.W. Cresswell, R.A. Allen, T.J. Headley*, W.F. Guthrie, L.W. Linholm, E.H. Bogardus** and C.E. Murabito, National Institute of Standards and Technology, *Sandia National Laboratories, **International SEMATECH, U.S.A.*
NIST, Sandia National Laboratories, and International SEMATECH are developing a new type of linewidth standard for calibrating Critical Dimension (CD) metrology instruments for lithographic process control.The standard reference feature is the bridge of an electrical linewidth test structure that is patterned in a mono-crystalline silicon film.Phase-contrast images of the cross sections of a sample of the bridge features on each wafer, produced by High-Resolution Transmission-Electron Microscopy (HRTEM), are used to trace the measured electrical linewidths of the standard reference feature to the lattice constant of silicon.This paper describes the automated analysis of the phase-contrast images that was developed in order to minimize the cost and uncertainty of the linewidths of the standards.

**09:30 Electrical CD Characterization of Binary and Alternating Aperture Phase Shift Masks**
*S. Smith, *M. McCallum, A.J. Walton and J.T.M. Stevenson, The University of Edinburgh, *Nikon Precision Europe, U.K.*
Many of the recent advances in optical lithography have been driven by the utilisation of complex photomasks using Optical Proximity Correction (OPC)or phase shifting technologies. These masks are difficult and expensive to manufacture so the ability to test and characterise the mask making process is very important. This paper examines the issues involved in the use of Electrical Critical Dimension (ECD) measurement of mask features.Modified cross-bridge test structures have been designed to allow the on-mask measurement of dense and isolated binary and phase shifted layouts. The results of electrical and Critical Dimension Scanning Electron Microscope (CD-SEM) testing of these structures are presented and indicate the lower variability associated with ECD measurements. In particular the adverse effect of phase shifting elements on the accuracy of SEM measurements is highlighted.

**09:50 Test Structures for Referencing Electrical Linewidth Measurements to Silicon Lattice Parameters using HRTEM**
*R. A. Allen, M. W. Cresswell, C. E. Murabito, William F. Guthrie, Loren W. Linholm, Coleen H. Ellenwood and E. Hal Bogardus* National Institute of Standards and Technology, Gaithersburg, *International SEMATECH, U.S.A.*
A technique has been developed to determine the linewidths of the features of a prototype reference material for the calibration of CD (Critical Dimension) metrology instruments. The reference features are fabricated in mono-crystalline-silicon with the sidewalls aligned to the (100) lattice planes. A two-step measurement procedure is used to measure the CDs. The primary measurement is via lattice-plane counting of selected samples using High-Resolution Transmission Electron Microscopy (HRTEM); the transfer calibration is via Electrical CD (ECD) test-structure metrology. Samples of these prototype materials were measured and provided as NIST Reference Material RM8110, to International

SEMATECH for evaluation by its member companies. In this paper, we will describe the measurement procedure and show the combined uncertainty of less than 15nm was derived.

**10:10am - 10:40am**Break

### SESSION 2: RF CHARACTERIZATION AND MODELLING

**10:40am - 12:00pm**
**Co-chairs**:**Yoshiaki Hagiwara**, Sony Corp.
**Kevin McCarthy**, University College Cork

**10:40 Impact of probe configuration and calibration techniques on quality factor determination of on-wafer inductors for GHz applications**
*R.J. Havens, L.F. Tiemeijer and L.Gambus*, Philips Research Laboratories, The Netherlands, *Philips Semiconductors, France*
We demonstrate that the quality factor measured on on-wafer (spiral)inductor test-structures are largely influenced by the choice between ground-signal and ground-signal-ground probe configuration. In particular, when the SOLT network analyzer calibration technique is used in combination with ground-signal probing, the quality factor value can be overestimated significantly.

**11:00 Metallization Proximity Studies for Copper Spiral Inductors on Silicon**
*C.B. Sia, K.S. Yeo*, Shao-Fu Chu, Z. Zeng and T.H. Lee, , Chartered Semiconductor Manufacturing Ltd., *Nanyang Technological University, Singapore*
Theimpact of metallizationproximityforcopper spiral inductors on siliconhavebeeninvestigated in this paper.Performance of the spiral inductorversusareaconsumptiontrade-offwithrespecttoits core diameterisevaluatedqualitativelyfor the first time.Effects of the inductor? sproximategrounded metallizationonitsoverallinductive performance are also analyzed.

**11:20 High frequency test structures definition for electromagnetic coupling study between two symmetrical inductors. Electrical modelling of the whole coupling between coils**

***C. Clement, B. Van Haaren and D. Gloria, ST Microelectronics, France***

High frequency test structures for electromagnetic coupling study between two symmetrical inductors are described. Results from the $S_{12}$ parameter measurement are compared to HP-Momentum electromagnetic (EM) simulations and show that coupling doesn?t reach -25dB and is smaller than -40dB for a separation distance between coils higher than 200µm. An electrical modelling of the whole coupling between coils is proposed and compared with experimental ones.

**11:40 Extraction Method for Substrate Resistance of RF MOSFETs,***J. Han, M. Je and H. Shin, KAIST, Korea*
This paper proposes a simple and accurate method for extracting substrate resistance of an RF MOSFET from the measured network parameters. The extraction results for 0.18mm MOSFETs are presented for various bias conditions and devices with different geometries.

**12.00pm -1:30pm**LUNCH

## SESSION 3: PROCESS CHARACTERIZATION

**1:30pm - 2:50pm**
**Co-chairs**: **Christopher Hess**, PDF Solutions Inc.
**Alan Mathewson**, NMRC

**1:30 Low current application dedicated process characterization method**
*W. Rahajandraibe, C. Dufaza, D. Auvergne, B. Cialdella*, B. Majoux* and V. Chowdhury*, LIRMM/CNRS, *ST-Microelectronics, France*
We present in this paper a new characterization method dedicated to an analog low consumption application design. A test structure, based on a bandgap reference voltage, that allows parameters extraction at the circuit operating point, is presented. This test structure is used to adjust the final SPICE parameters in order to calibrate the electrical measurement value of each component of the circuit on the chip. An improvement of the design is simulated, tested and validated on silicon.

**1:50 A New Test Structure and Characterization Methodology to Identify Array Leakage Path in Mask ROM**
*T.H. Fan, K.Y. Chan, T.C. Lu and B. Pan, Macronix International Co. Ltd., Taiwan*
The array leakage is a crucial issue while developing ultra high-density planar Mask ROM memories. However, the conventional test structure of cell array is hard to identify this leakage and its mechanism because the cell surface punch leakage, cell bulk leakage, and surface buried drain to buried drain (BD to BD) leakage beyond cell channel region occur at the same time. By using this new test structure and test methodology, the mechanism of this leakage has been attributed to the surface BD to BD leakage. This leakage path occurs beneath the exposed silicon surface, which doping concentration near this region is lower due to PMOS blank N-type pocket implantation and spacer oxide over-etching.

**2:10 Test Structure for Precise Statistical Characteristics Measurement ofMOSFETs**

**Y. Shimizu, M. Nakamura, T. Matsuoka and K. Taniguchi, Osaka University, Japan**

A new test structure consisting of a MOSFET array and peripheral decoder circuits is proposed to study statistical variation (mismatch) in MOSFET characteristics. A Kelvin technique was implemented in the structure to cancel parasitic resistance of metal wiring and transmission gates in such a way that any MOSFET in the array can be measured at the same bias condition. Accurate electrical measurements using the structure make it possible to derive the statistical variation of threshold voltage and of the transconductance of MOSFETs placed in a small area.

**2:30An Assessment of Physical and Electrical Design Rule Based Statistical ProcessMonitoring and Modelling (PEDR-SPMM): For Foundry Manufacturing Line of Multiple-Product Mixed-Run**
*K. Yih-Yuh Doong*,**, S. Hsieh*, S.C. Lin*, L.J. Hung*, R.J. Wang*, B. Shen*, J.W. Hisa*,J.C. Guo*, I.C. Chen*, K.L. Young* and C. Ching-Hsiang Hsu**, *TSMC,**National Tsing-Hua University, Taiwan*
A novel methodology of physical and electrical design rule based statistical process monitoring and modeling (PEDR-SPMM) is proposed. By the aid of principal component analysis, the correlated physical and electrical parameters are decomposed into an independent variable set. The

key parameter of multiple products mixed-run can be formulated by the independent variable set, which reduces the modeling complexity, and also provides a way to get a comparison between different technology nodes.

**2:50pm - 3:20pm**Break

## SESSION 4: POSTER SESSION

**3:20pm - 4:05pm**

**Co-chairs**:**Takashi Ohzone**, Toyama Prefectural University
**Anthony Walton**, University of Edinburgh

**3:20 A Test Circuit for Measuring Standard Deviations of MOSFET Channel Conductance and Threshold Voltage**

*K. Terada and M. Sumida, Hiroshima City University, Japan*

A new test circuit is proposed for measuring the standard deviations of both MOSFET channel conductance and threshold voltage.This test circuit consists of the matrix-shape MOSFET array in which several switches and wiring are added.DC currents flowing through this array are measured, changing the ON/OFF states of the switches, and then the standard deviations are calculated from them.

**3:25 A consistent and scalable PSPICE HFET-Model for DC and S-Parameter- Simulation**

*S. Ehrich, R. M. Bertenburg*, M. Agethen*, A. Brennemann*, W. Brockerhoff and F.-J. Tegude, Gerhard-Mercator-University, *IPAG, Germany*

For simulation of digital circuits realized in **D**irect **C**oupled **F**ET **L**ogic using depletion-type as well as enhancement-type **H**eterostructure-**F**ield **E**ffect **T**ransistors a consistent model that is able to describe both types of transistors is necessary. The developed analytical PSPICE model takes into account all device relevant intrinsic and parasitic effects. This model can be used for dc- as well as rf-simulations and is scaleable with respect to gate-width as well as gate-length.

**3:30 Extraction of the Base and Emitter Resistances in Bipolar Transistors Using an Accurate Base Resistance Model**

*F. Ingvarson, M. Linder* and K. O. Jeppson, Chalmers University of Technology, Malardalens Hogskola, Sweden*

A straightforward method for extracting the base and emitter resistances is presented. The method has the following properties: 1) only a standard forward Gummel measurement on one transistor is required, 2) current-crowding and conductivity-modulation in the base are accounted for through the use of an accurate base resistance model, and 3) the resistance parameters are extracted using a non-linear optimization step. Furthermore, a technique for extraction of the high-injection parameters of a modified collector current model is also presented.

**3:35 Sensitive measurement method for evaluation of high thermal resistance in bipolar transistors**

*N. Nenadovic*, L.K. Nanver*, H. Schellevis*, D. de Mooij**, V. Zieren** and J.W. Slotboom*,**, *DIMES/Delft University of Technology, **Philips Research Laboratories, The Netherlands*

A sensitive measurement method is used to discern between the thermal effects of very small changes in device surroundings and to extract high thermal resistance values. The description of electro-thermal behavior is complemented by nematic liquid crystal imaging and FEM simulations of the heat spreading around the device.

**3:40 CV doping profiling of boron out-diffusion using an abrupt and highly doped arsenic buried epilayer**

*C.J. Ortiz*, L.K. Nanver*, W.D. van Noort*, T.L.M. Scholtes* and J.W. Slotboom*,**, *DIMES/Delft University of Technology, **Philips Research Laboratories, The Netherlands*

The CV doping profiling of boron regions using an abrupt and highly doped buried n+ epilayer is demonstrated.For boron profiles with an abruptness of a few nm/dec an n-p-n+ structure gives the most accurate result. The method can be used to evaluate the TED of ultra shallow boron junctions and epitaxially grown boron spikes.

**3:45 Strategies and Test Structures for Improving Isolation between Circuit Blocks**

*D. Szmyd, Laurent Gambus* and W. Wilbanks**, Philips Semiconductors, Hopewell Junction, USA, *Philips Semiconductors, France, **Philips Semiconductors, Albuquerque, U.S.A.*

RF coupling of signals between circuit blocks can be severe. We quantify electrical isolation on concentric test structures using s-parameter measurements up to 50GHz. The use of deep trenches greatly improves isolation. Guard rings and junction isolation is also beneficial.

**3:50 A Test Structure for Spectrum Analysis of Hot-Carrier-Induced Photoemission from Subquarter-Micron CMOSFETs**

*T. Matsuda, T. Ohzone, S. Odanaka*, K. Yamashita**, N. Koike** and K. Tatsuuma*

*Toyama Prefectural University, *Osaka University, **Matsushita Electric Ind. Co. Ltd., Japan*

Hot-carrier-induced photoemission of subquarter-micron CMOSFETs are analyzed using a specially designed test structure, which has a wide channel width of 2.0 mm for sufficient photoemission intensity. Since the test structure consists of parallel-connected unit MOSFETs and photoemission images are uniform, it can be estimated that measured spectra are the same as that from unit MOSFETs. The relation between photon counts and photon energy suggests that photon energy has a Boltzmann distribution; $\exp(-h\nu/kT_e)$.

**3:55 A Novel Method to Characterize the Dielectric and Interfacial Properties of $Ba_{0.5}Sr_{0.5}TiO_3$(BST)/Si by Microwave Measurement**

*H.-T. Lue, T.-Y. Tseng and G.-W. Huang*, National Chiao-Tung University, *National Nano Device Laboratories, Taiwan*

We have developed a new method to investigate the dielectric and interfacial properties of gate dielectric thin films by microwave measurement. BST thin films were deposited on 10Ω-cm (normal) and 10kΩ-cm (high-resistivity, HR) substrates at the same time by RF magnetron sputtering. For the BST-HR silicon, coplanar waveguides (CPW) were fabricated and measured at microwave frequencies with Thru-Reflect-Line (TRL) calibration while CV measurements were carried out for BST/normal-silicon. From the phase change of CPW transmission line and the maximum capacitance in CV measurement, the dielectric constants of both BST thin film and interface layer can be determined. Furthermore, the behaviour of insertion loss versus bias voltage was found to be correlated with the density of trap states. The results indicate that our method can provide useful information to study the dielectric and interfacial properties of metal-insulator-semiconductor (MIS) structures.

**4:00A test structure for the design of thermal gas flow sensors**

*N. Sabate, I. Gracia, J. Santander and C. Cane, CNM-CSIC, Spain*

A test structure for the design and optimisation of thermal gas flow sensors has been developed. This test structure provides information about the temperature distribution created around a heated element as well as its modification due to a gas flow thus providing information about the thermal conductivity of the membrane material. Data obtained from the characterisation of the structure can be used in the optimisation of a flow sensor designed for any specific application.

***4:05 Exhibition Presentations***

## *WEDNESDAY, APRIL 10, 2002*

***8:30am****Registration*

## *SESSION 5: PARAMETER EXTRACTION*

***9:00am - 10:20am***
*Co-chairs****Kjell Jeppson****, Chalmers University of Technology*
***Hans Tuinhout****, Philips Research*

***09:00A Combined $R_G/C_F$ Large-Signal Extraction Methodology to Improve CMOS SPICE-Parameter Precision***

*S. Mecking, A. Korbel, E. Paparisto* and U. Langmann, Ruhr-Universitat Bochum, *Infineon Technologies AG, Germany*
This paper presents a simple and efficient parameter extraction methodology, based on time-domain large-signal measurements of two ring oscillators as test structures. This experimentally confirmed technique is a new tool for determining the parasitic gate resistance RG and for a fine tuning of the fringing capacitance CF of MOS transistors in one step. Thus CMOS switching speed can be predicted more accurately, compared to conventional parameter tuning methodologies and the expenditure of SPICE parameter extractions can be reduced.

***09:20 BSIM4.1 DC Parameter Extraction on 50nm n-pMOSFETs***

*D. Souil, G. Guegan, G. Bertrand, O. Faynot, S. Deleonibus and G. Ghibaudo*, CEA-LETI, *IMEP, France*
For the first time, DC characteristics of conventional 50nm MOSFETs have been correctly simulated by BSIM4.1 model. This paper briefly describes the conventional architecture of the devices, then the related strategy for parameter extraction is depicted. Typical simulation results are shown, putting forward that reverse short channel and 2D charge sharing effects are well fitted by this compact model.

***09:40 Useful Numerical Techniques for Compact Modeling***

*C. C. McAndrew, Motorola Inc., U.S.A.*
This paper presents three useful numerical techniques for compact modeling. First, a new approach to modeling non-uniform vertical doping profiles in MOSFETs is presented, based on a non-linear mapping of the backgate bias. Second, a technique that guarantees that limiting of Vds at saturation will not lead to glitches in output conductance is presented. And third, requirements for limiting functions for Vds that do not cause discontinuities in high order derivatives at Vds=0 are defined. Examples of limiting functions that maintains proper symmetry are given. The techniques to eliminate glitches in output conductance and maintain symmetry are applicable to MOSFET and resistor models.

***10:00 Influence of Probing Configuration and Data Set Size for Bipolar Junction Capacitance Determination***

*D. MacSweeney, K.G. McCarthy*, L. Floyd***, A. Mathewson***, P. Hurley***, J.A. Power**** and S.C. Kelly****, Cypress Semiconductor, *University College Cork, ***NMRC, ****Analog Devices, Ireland*
In this paper, the on-wafer measurement of Junction Depletion Capacitance is examined. This work provides an in-depth discussion of possible probing configurations which can be used. It outlines a method to consistently measure the junction capacitances accurately.The results from this method compare favourably with those extracted using S-parameter measurements. Additionally a method is formulated to determine the minimum number of data points required to maintain extraction accuracy.

***10:20 - 10:50*** *Break*

## *SESSION 6: NON-VOLATILE MEMORY CHARACTERIZATION AND MODELING*

***10:50am - 12:10pm***
***Co-chairs****:****Hiroaki Hazama****, Toshiba Corp.*
***Michael Peter Kennedy****, University College Cork*

***10:50 New Spider-Webs Test Structure and Characterization Methodology for Flash Memory Tunnel Oxide Quality***

*T.H. Fan, T.C. Lu and S. Pan, Macronix International Co. Ltd., Taiwan*
The tunnel oxide quality is a key parameter in Flash memories. A high quality tunnel oxide will result in good cell endurance characteristics. However, the conventional tunnel oxide characterization is based on a large area test structure with high sheet resistance floating gate, therefore, an over-estimated oxide quality is obtained. In this paper, not only a new spider-webs test structure for evaluating tunnel oxide quality but also new tunnel oxide test methodology for Flash memories are proposed. By using this new test structure and test methodology, a more accurate and reliable tunnel oxide lifetime prediction is obtained, which can be correlated to the program/erase endurance failure mechanism.

**11:10 Extraction of the Coupling Coefficients for the Top-Floating-Gate (TFG) flash EEPROM Cell**

*D. McCarthy, M. O?Shea, R. Duane, K.G. McCarthy*, A. Concannon** and A. Mathewson, NMRC, *University College Cork, Ireland, **National Semiconductor Corporation, U.S.A.*
A new measurement technique involving a new test structure is applied to the existing sub-threshold methodology for modelling the coupling ratios of a Top-Floating-Gate (TFG) nonvolatile memory cell. This new technique proves the benefits of the TFG cell design and will be used in further development and optimization of this recently demonstrated cell.

**11:30 Wafer-Level Characterization of EEPROM Tunnel Oxide Using a Fast Floating-Gate Technique and a Realistic Memory Cell-based Test Structure**

*S. Renard, P. Boivin andJ.-L. Autran*,ST-Microelectronics, *Universite Aix Marseille, France*
We report on the development of a fast characterization technique of EEPROM tunnel oxide based on the floating-gate technique and using a realistic memory cell-based test structure. A sequential measurement procedure and data analysis have been successfully implemented to perform automatic wafer screening of leakage currents in terms of charge retention and tunnel oxide defectivity.

**11:50 Compact Model Development for a New Non-Volatile Memory Cell Architecture**
*M. O'Shea, D. McCarthy, R. Duane, K.G. McCarthy*, A. Concannon** and A. Mathewson, NMRC, *University College Cork, Ireland, **National Semiconductor Corporation, U.S.A.*
A model for a novel flash memory device, the Top Floating Gate (TFG) cell, is described.The development of an accurate model for flash memory is complicated by the variable nature of the cell. In standard flash memory, the threshold voltage and therefore the drain current of the cell varies as the cell is programmed or erased. In the TFG case both the threshold voltage and series resistance vary which further complicates the model development. The model is SPICE compatible and accurate over the complete range of operation of the cell.

**12:0pm - 1:30pm**LUNCH
**1:30pm - 1:40pmICMTS 2003**

# SESSION 7: INTERCONNECT

**1:40pm - 3:00pm**
**Co-chairs**:**Alexander Rahm**, Siemens AG
**Kunihiro Asada**, University of Tokyo
1:40 **Test Structures for the Electrical Characterisation of Platinum Deposited by Focused Ion Beam**
*S. Smith, A.J. Walton , S.Bond, A.W.S. Ross, J.T.M. Stevenson and A.M. Gundlach The University of Edinburgh, Scotland*
Focused Ion Beam (FIB) systems are commonly used to image, repair and modify integrated circuits by cutting holes in passivation to create vias or to selectively break metal tracks.The ion beam can also be used to deposit a metal, such as platinum, to create new connections. These techniques are very useful tools for debugging designs and testing possible changes to the circuit without the expense of new mask sets or silicon. This paper presents test structures to characterise an FIB platinum deposition process. Sheet resistance test structures have been fabricated using an FIB tool and the results of testing these structures are presented. This data will enable resistors with a known value to be fabricated in addition to conducting straps.

**2:00 Passive Multiplexer Test Structure For Fast and Accurate Contact and Via Fail Rate Evaluation**
*C. Hess, B. E. Stine, L. H. Weiland, T. Mitchell*, M. Karnett* and K. Gardner**
*PDF Solutions Inc., San Jose, *Philips Semiconductors, U.S.A.*
Complexity of integrated circuits has led to many millions of contacts and vias on every chip. To allow accurate yield evaluation, it is required to determine fail rates of < 10 faults per billion which requires test structures with huge chains of 1 million or more contacts and vias. At the same time contacts and vias are getting smaller and thus their resistance is increasing for every new technology node. Consequently, the resistance of such chains becomes impossible to measure. To overcome this limit without increasing the number of measurement pads, we are proposing a Passive Multiplexer Array of via chains, which breaks up a huge contact/via chain in many individually measurable sub-chains. Accuracy of fail rates will be increased, since the fail rate can be determined based on many sub-chains, instead of being determined based on one huge chain only. Furthermore, this test structure better supports failure analysis, since it is faster to locate a faulty contact or via. No additional devices or process steps are required which allows implementation as short flows for fast process problem debugging.

**2:20 Verification Structures for Transmission Line Pulse Measurements**
*R. A. Ashton, Agere Systems, U.S.A.*
Test structures intended for performance verification of transmission line pulse (TLP) systems have been designed and tested. They consist of simple resistors in either copper or silicide-clad polysilicon. The copper structures proved unsuitable due to excess heating and melting of any reasonable geometry. The silicide-clad polysilicon proved more successful. A simple model of resistive heating accounts for observed non-linearity in the structures under high current stress.

**2:40 Direct Measurement of Field Transistor Threshold Voltages using Inversion Layer Field Transistors in Deep-Submicron Processes**
*J. N. Ellis, Zarlink Semiconductor, U.K.*
Polysilicon field transistors are traditionally overlapped onto thin oxide regions to connect to the source and drain of a transistor. Submicron processes have gate oxides with breakdown voltages below the field threshold and the traditional layout is not suitable. It is however necessary to maintain a channel to the source and drain, but this can be accomplished using a field plate device. By placing a metal gate over the poly gate, and biasing the metal gate into strong inversion, it is possible for the polysilicon gate to control the transistor current. In fact with this one structure both the polysilicon and metal field threshold voltages can be ascertained.

**3:00pm - 3:30pm**Break

# SESSION 8: YIELD AND RELIABILITY

**3:30pm - 4:50pm**
**Co-chairs**:**Akella Satya**, KLA-TENCOR
**Bill Verzi**, Agilent Technologies
**3:30 Methodology for Defect Impact Studies under Conditions of Low Electrical Testing Coverage**
*A. Skumanich and E. Ryabova, Applied Materials, U.S.A.*
A methodology is described which establishes the prioritization of targeted defects based on electrical impact of the different defect types using a Short Loop Yield Monitor under conditions of low statistics. Probe results from electrical test patterns for interconnect structures are

correlated with optical defect inspection data to determine the quantitative kill rates of various defects. To assess defect impact with reasonable likelihood of correlation, defects are deliberately introduced at specific process points. These deliberately introduced defects are used to evaluate the effect of native defects at a given level.

**3:50 Novel Charge Pumping Method without Using MOS Transistor for SOI Wafer Inspection**

*T. Takami, H. Yoshida, T. Uchihashi and S. Kishino, Himeji Institute of Technology, Japan*

A novel charge pumping method without using MOS transistors is proposed for obtaining a spatial distribution of interface traps in an SOI wafer. The proposed method can be performed without fabrication processes for the source/drain of MOS transistors which are essential for conventional charge pumping methods. In this method, Schottky contacts are used instead of the normal source/drain diffused layer. The results demonstrate that the proposed method is effective in application to SOI wafer inspection.

**4:10 Logic Characterization Vehicle to Determine Process Variation Impact on Yield and Performance of Digital Circuits**

*C. Hess, B. E. Stine, L. H. Weiland and K. Sawada*, PDF Solutions, U.S.A., *Toshiba Corporation, Japan*

Manufacturing of integrated circuits relies on the sequence of many hundred process steps. Each of these steps will have more or less variation, which has to be within a certain limit to guarantee the chips functionality at a target speed. But, not every chip layout is susceptive to process variation the same way, which requires a link between process capabilities and product design. This paper will present a novel Logic Characterization Vehicle (LCV) to investigate the yield and performance impact of process variation on high volume product chips. The LCV combines and manipulates new or already documented circuits like memory cells and combinatorial logic circuits within a JIG interface that allows fast and easy testability. Beside the functionality of such circuits, also path delay as well as cross talk issues can be determined.A standard digital functional tester can be used, since all timing critical measurements will be performed within the JIG. The described method allows early implementation of existing circuits for future technology nodes (shrinks). A Design Of Experiments (DOE) based implementation of possible layout manipulations will determine their impact on yield and performance of a target design as well as its sensitivity to process variation. The described approach can be used at a much earlier stage of product and process development, which will significantly shorten yield ramp.

**4:30 Test Structures for Analyzing Radiation Effects in Bipolar Technologies**

*H. J. Barnaby, R.D. Schrimpf*, K.F. Galloway*, D.R. Ball*, R.L. Pease** and P. Fouillat***, University of Arizona, *Vanderbilt University, **RLP Research,U.S.A., **University of Bordeaux, France*

Structures integrated onto BiCMOS test chips were specially designed to characterize the complex mechanisms related to proton radiation response in bipolar technologies.Bipolar devices from two commercial processes were modified to include independent gate terminals. Through the use of gate control, the effects of proton-induced defects on discrete bipolar devices and analog bipolar circuits can be analyzed independently, thereby facilitating a quantitative, experimentally verified, description of the non-linear relationship between the radiation defects and electrical response at both the device and circuit level.

# THURSDAY, APRIL 11, 2002

**8:30am**Registration

# SESSION 9: MEMS AND PHOTONICS

**9:00am - 10:00am**

**Co-chairs:Colin McAndrew**, Motorola

**Robert Ashton**, Bell Laboratories

**09:00 Test Structures for a MEMS $SiO_x$/metal process**

*M. Hill, C. O'Mahony, P.J. Hughes, B. Lane and A. Mathewson, NMRC, Ireland*

The application of a method to extract material parameters in $SiO_x$/metal composite films of MEMS infrared sensors is presented. Arrays of cantilever beam test structures are used to determine the elastic modulus, residual stress and stress gradient in fully processed wafers. The material properties are extracted from pull-in voltage and static deflection measurements. The benefits of 3D finite element models to include structure buckling, non-ideal mechanical boundary conditions and capacitance fringing effects in the parameter extraction process are described.

**09:20 Characterisation of Microfluidic Devices**

*D.C.S. Bien, S.J.N. Mitchell and H.S. Gamble, Queen?s University Belfast, U.K.*

Silicon micromachining techniques have enabled the fabrication of a wide range of microfluidic components and systems.Given the small volumes of liquid and low flow rates involved, the accurate characterisation of such systems presents a challenge. To date many of the measurements have been performed manually; this is both time consuming and prone to inaccuracies.This paper describes an automated measurement technique and presents results for a surface micromachined valve.

**09:40 Triple-Junction Colour Sensor Fully Compatible with CMOS Technology: Results of a Test Chip**

*G.-F. Dalla Betta*, N. Zorzi*, P. Belluti*, M. Boscardin* and G. Soncini*,**, *ITC-IRST, **Universita di Trento, Italy*

We show that a triple-junction photosensor can been obtained within a CMOS n-well technology with no additional process steps but a simple layout modification of the p-channel-stop mask. Results from the electro-optical characterisation of a specially designed test-chip proved that the wavelength selectivity of the sensor can be used for colour detection and confirmed the device full compatibility with CMOS technology.

**10:00am - 10:30am**Break

# SESSION 10: MATCHING

**10:30am - 12:10pm**

**Co-chairs:Loren Linholm**, NIST
**Johan Klootwijk**, Philips Research

**10:30 Design and Characterisation of a High Precision Resistor Ladder Test Structure**

*H.P. Tuinhout, G. Hoogzaad*, M. Vertregt, R.L.J. Roovers and C. Erdmann**, Philips Research, The Netherlands, *Philips Semiconductors, The Netherlands, **Philips Semiconductors, France*

A new sub-site stepped multi-resistor Kelvin test structure for characterizing small resistance mismatch effects in resistor ladders is introduced. Using a dedicated measurement and statistical evaluation technique, this approach enables identification of very small (<0.05%) systematic mismatch patterns, which are associated with local mechanical stress as well as nanometre scale mask writing artifacts.

**10:50 A Robust and Production Worthy Addressable Array Architecture for Deep Sub-micronMOSFET's Matching Characterization**

*S.B. Yeo, J. Bordelon*, S. Chu**, M.F. Li, A. Tranchina*, M. Harward*, L.H. Chan** and A. See**, The National University of Singapore, *TestChip Technologies Inc., **Chartered Semiconductor Mfg. Ltd., Singapore*

A robust addressable array test structure is presented, which allows automated characterization of the MOSFETmatching, with high area and time efficiency, accuracy and repeatability. It features CMOS switches to ensure a full test operation range, and prevent gate oxide breakdown of individual DUTs from destroying the functionality of the whole test structure. The test structure provides superior isolation to minimize cross talk while providing greater flexibility in testing. Test results ($I_d$ mismatch) from wafers on 0.18µm technology will be presented.

**11:10 A comparison of extraction techniques for threshold voltage mismatch**

*J.A. Croon[1,2], H.P. Tuinhout[3], R. Difrenza[4,5], J. Knol[6], A.J. Moonen[6], S. Decoutere[1], H.E. Maes[1,2] and W. Sansen[2], [1]IMEC, Belgium, [2]ESAT/K.U. Leuven, Belgium, [3]Philips Research, The Netherlands, [4]ST Microelectronics, France, [5]LPCS/ENSERG, France, [6]Philips Semiconductors, The Netherlands*

In this paper commonly used extraction methods of MOSFET threshold voltage mismatch are compared. The $V_T$ mismatch is extracted on the exact same device population by four independent characterization groups. Significant differences are observed, which are caused by differences in measurement setup and differences in extraction algorithms. The observed differences are analyzed. In addition merits and limitations of the various techniques are evaluated

**11:30 Comparison Between Matching Parameters and Fluctuations at the Wafer Level**

*R. Difrenza*, **, P. Llinares*, S. Taupin*, R. Palla* and G. Ghibaudo**, *ST Microelectronics, **LPCS/ENSERG, France*

This paper compares the random local fluctuations, commonly known under the term of mismatch, with the variations that appear at the wafer level for the MOS transistor and the polysilicon tresistor. In particular, it highlights the strong decrease of MOSFET matching performance when the device area is reduced, by comparison to the fluctuations at the wafer level. This amazing tendency involves that the well known phenomenon responsible for the MOS transistor mismatch do not dominate for the smallest devices. In particular, the impact of polysilicon edge roughness induced by stochastic process during photolithography or etching is investigated.

**11:50 Systematic Mismatch in Diffusion Resistors caused by Photolithography**

*Hausser, S. Majoni, H. Schligtenhorst and G. Kolwe, Philips Semiconductors GmbH, Germany*

During the qualification of a 0.35µm CMOS process, it was observed that diffusion resistors showed a systematic mismatch, depending on the position on the wafer. The mismatch increased from the center of the wafer to the outer regions. Various experiments showed that the mismatch was caused by spinning the wafer during the resist developmentprocess. Changing this process eliminated the systematic diffusion resistor mismatch.

**12:10pm - 12:30 pm**Break

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**12:30pm**Best paper announcements and closing remarks