ICMTS 2001

International Conference on Microelectronic Test Structures

Tutorial and Technical Program

March 19-22, 2001

International Conference Center Kobe

Kobe, Japan

CONTENTS

CONFERENCE REGISTRATION FORM

CONFERENCE OFFICIALS

Conference Committee
Steering Committee
Technical Committee

ICMTS 2001

CHAIRMAN'S LETTER

Dear Colleague,

On behalf of the committee, I welcome you to the 2001 International Conference on Microelectronic Test Structures (ICMTS 2001) in Kobe, Japan. This is the 14th ICMTS as an international conference and the 4th one to be held in Japan. The conference is sponsored by IEEE Electron Devices Society and Association for Promotion of Electrical, Electronic and Information Engineering in cooperation with Institute of Electronics, Information and Communication Engineers, and Japan Society of Applied Physics.

The purpose of the conference is to bring together designers and users of test structures to discuss recent developments and future directions. This year's conference consists of 48 papers in 9 oral sessions and 1 poster session. Session topics will include: "Device Characterization", "Yield & Process Characterization", "Interconnect", "Reliability", "Parameter Extraction", "Matching" and "RF Measurements". Oral presentations are 15 minutes long with 5 minutes for questions. The poster session is preceded by a 5 minutes oral presentation by the author.

I am convinced that the test structures for new process, device and circuit developments become important as the feature size is scaled down into deep submicron; introduction of new materials, new CMOS or SOI devices, and high frequency and precise digital/analog circuit design. Furthermore, an advantage of test structures, which can provide the rapid transfer and quick yield improvements of new LSIs from R&D section to factories as well as between factories, becomes widely recognized. The well-designed test structures will also support the worldwide distribution of IP (Intellectual Properties) for SoC (System-on-a-Chip) in the 21st century.

The one-day Tutorial Short Course will be held on March 19. The course is intended to provide the participants with a guideline on good design, test and analysis. The seven instructors have many years of experience in the field of test structures. The Tutorial will cover Key Note Presentation, CD-Measurements, TCAD, Parameter Extraction, SOI Devices, RF Measurements and Reliability.

There will be an equipment exhibition relating to the latest test structure measurements: measurement instruments, wafer probing equipment, computer software for data analysis, parameter extraction and measurement control.

In 1981, Kobe City built a convention complex on Port Island-the world's first "Cultural City on the Sea". The Conference will be held at the International Conference Center Kobe on the Port Island. Kobe port was opened about 130 years ago to the external trade, and thus historical buildings related to the foreigners are well preserved such as Ijin-kan (Foreigner's Mansion) and Old Settlement. Now, Kobe City is Japan,s 7th largest city with a population of about 1.4 million, and one of the most modern and prominent trading ports in the world.

I am sure that ICMTS 2001 in Kobe will give you excellent technical experience, cultivation of friendship with many engineers as well as understanding about Japanese cultures. We are looking forward to seeing you in Kobe!

Sincerely,

Takashi OHZONE

General Chairman

GENERAL INFORMATION

Conference Information

The IEEE Electron Devices Society and Association for Promotion of Electrical, Electronic and Information Engineering are sponsoring the 2001 International Conference on Microelectronic Test Structures to be held in cooperation with The Institute of Electronics, Information and Communication Engineers (IEICE), and The Japan Society of Applied Physics (JSAP). The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The Conference will be preceded by a one-day Tutorial Short Course on Microelectronic Test Structures.

Presentation

The official language of the conference is English and it will be used for all presentations, printed materials. An overhead foil projector and a data projector connected to a laptop PC will be available for your presentation of ICMTS 2001. We prefer the usage of the data projector and suggest using your own PC for the presentation to avoid some troubles. We will prepare a laptop PC and accept presentations as **PDF files or MS Power Point files** only, if you send it the ICMTS secretariat until **March 10**, 2001 by e-mail. Please **bring backup foils of your presentation**, in case something accidentally does not work on the data projector as expected. There will be no slide projector available. All speakers are requested to report to the speaker's registration desk located in front of the conference room before their presentation.

Best Paper Award
One paper presented will be selected for the Best Paper Award. Presentation of the award will be made at the ICMTS 2002.

Conference Proceedings
The IEEE ICMTS 2001 will publish a proceedings. One copy of the proceedings is included in the registration fee. Additional copies will be available at the Conference for 5,000yen per copy for members of the IEEE or IEICE or JSAP, 7,000yen per copy for non-members, or from the IEEE after the conference.

One-site registration schedule
On-site registration for the conference will be conducted in the Lobby (3rd floor) at International Conference Center Kobe as follows:

Monday,	March 19	8:00-19:00
Tuesday,	March 20	8:00-17:00
Wednesday,	March 21	8:30-16:00
Thursday,	March 22	8:30-11:00

Conference registration fees
A registration form is included in the center of this booklet. Below are the conference fees for early, late, and on-site registrants.

Early Registration:(Postmarked by February 1, 2001)

	Member*	Non Member	Student**
Tutorial	18,000 yen	21,000 yen	8,000 yen
Technical Sessions	35,000 yen	43,000 yen	25,000 yen

Late Registration:(Registered after February 1, 2001)

Tutorial	25,000 yen	28,000 yen	10,000 yen
Technical Sessions	38,000 yen	46,000 yen	26,000 yen

One-site Registration:(Registration at the Conference)

Tutorial	31,000 yen	34,000 yen	13,000 yen
Technical Sessions	40,000 yen	48,000 yen	28,000 yen

* Must be a member of the IEEE or IEICE or JSAP.
**To qualify for reduced conference rates, you must be a Student Member, a full time student, not be self-employed, nor working part or full time at a facility or corporation.

Registration fees include admittance to technical sessions, equipment exhibits, morning and afternoon coffee breaks, reception, conference banquet, one copy of the proceedings.

Payment of the registration fees
HOTEL BOOKING and CONFERENCE REGISTRATION FORMS are available
Registration fees should be payable to the IEEE ICMTS 2001 and must be in **Japanese Yen only.**
(1) Bank Transfer in Yen to "EEE ICMTS 2001" Account at the Tokyo Mitsubishi Bank. Esaka Branch A/C No. 0936608
(2) Bank Check in Yen payable to the order of "EEE ICMTS 2001" Personal Checks are not acceptable.
(3) Credit Card in Yen: Master Card, VISA, Diner's Club, American Express*
(4) Cash in Yen at the conference registration desk.
*For credit card payments of registration fees, add 5% to the registration fee for handling charges.

Cancellation
Due to advance financial commitments, refunds of registration fees requested after March 1, 2001, cannot be guaranteed. 5,000 yen processing fee will be withheld from all refunds. Requests for refunds of registrations cancelled after March 1 will be considered after the conference.

Messages
If you need to be contacted during the Conference Sessions, a message can be left at +81-78-302-5200 (Ext. ICMTS Secretariat) between the hours of 9:00am and 5:00pm, March 19, 20, 21, and from 9:00 to 12:00pm on March 22. Messages will be placed on a Message Board beside the registration desk.

Banquet
The conference banquet will be held on Wednesday evening, March 21 at 7:00 pm. at Portopia Hotel (16F Room Rainbow, South Wing; connected by corridor from the Conference site). Conference registration fees include one banquet ticket. Guest ticket will be available for sale at the registration desk.

Excursion
We have arranged Excursion on Thursday, March 22.
Visit Scientific Museum of Akashi Bridge, longest suspension bridge of the world and Himeji Castle which has been designated a World Cultural Heritage site.
Time: 13:00-18:00
Fare: 4,000yen/person (Admission tickets and Lunch box are included)

Kobe Information
Located roughly in the center of Honshu, Japan's main island, Kobe is easily accessible by land, sea, and air. It is about 3 hours and 20 minutes from Tokyo by Bullet Train, and 25 minutes by high-speed boat from the Kansai International Airport. Together with Osaka and Kyoto, it forms the focal point for the economy of western Japan.

Climate and Clothing
The temperature in Kobe during the conference period will range between 8—C (46—F) at night and 18—C (64—F) during the day. The weather is, however, often unpredictable during this season. The average humidity is 63%, so light clothing and a sweater or light coat is recommended. Conference Center is fully air-conditioned.

Hotel Accommodations
The Japan Travel Bureau, Inc. (JTB) has been appointed the Official Travel Agent for ICMTS 2001 and will handle all travel arrangements to and within Japan. Please address all inquiries and application forms for hotel accommodation to:
Japan Travel Bureau, Inc. (JTB)
Tours & Convention Division, Kansai District
Nittochi-Dojima Bldg.
1-4-19 Dojimahama, Kita-ku
Osaka 530-0004, Japan
Phone:+81-6-6345-3979 Fax:+81-6-6345-0910

Japan Travel Bureau (JTB) has reserved a sufficient number of rooms at the following hotels for the conference participants at special discount rates. Those who wish to apply for hotel reservation are requested to complete the application form, and return it to JTB before March 7, 2001 with the necessary deposit (10,000 yen per room).
HOTEL BOOKING and CONFERENCE REGISTRATION FORMS are available
Hotel Assignment will be made on a first-come, first-served bases.
Daily room charges are as follows:

Class	Name of Hotel	Room Rate		
		Single	Twin	Deluxe Single*
A	Portopia Hotel	12,600 yen	11,550 yen	17,850 yen
B	Hotel Pearl City Kobe	11,025 yen	9,450 yen	
C	Sunside Hotel	7,770 yen	7,350 yen	

*Single occupancy of twin room
Note: 1) Above rates includes breakfast, service charge and tax.
2) The deposit of 10,000yen will be deducted from the balance of the hotel bill upon check-out.

Cancellation
In case of hotel cancellation, written notification should be sent directly to JTB.
Deposit will be refunded after deducting the following cancellation charges, when notification is received by JTB.

Up to 9 days before the first night of stay	1,000 yen per room
8-2 days before	20% of the daily room charge
One day before	80% of the daily room charge
On day, or no notice given	100% of the daily room charge

Equipment Exhibition
An equipment exhibition will be held besides the conference room during the Conference to display equipment closely paralleling the nature of this meeting. This equipment exhibition will permit one-on-one discussions between exhibitors and conference attendees on the latest test equipment. Exhibits will be open as follows.
March 19 13:00 - 18:00
March 20, 21 9:00 - 18:00
March 22 9:00 - 12:00
The exhibitors' list will be distributed on the day of the conference.

TUTORIAL SHORT COURSE
MONDAY, MARCH 19
Tutorial Program

8:00 a.m. Registration
9:00 a.m. **1. Welcome Talk - Shigeru Okamura, Fujitsu Lab.**
9:05 a.m. **2. Key Note Presentation**
Measurement Technology for Home Entertainment LSI Chips
-Yoshiaki Hagiwara, SNC Strategic Planning Department, Sony Corporation
*Some process & device technology aspects of home entertainment LSI chip sets such as digital cameras, home robotics, and games
*Test structures and measurement technology specifications for desired yield enhancements and device performance characterizations

10:45 a.m. Coffee Break

11:15 a.m. **3. Physical Model Parameter Extractions for Sub-Tenth Micron MOSFETs - Hitoshi Aoki, Agilent Technologies Japan Ltd.**
*Introduction, importance of accurate SPICE Model parameters
*To obtain "Good" MOSFETs Model parameters measurement setups, TEG design (device selection), extraction methods, and optimizations

*Numerical extraction methods for physical model parameters, DC parameter extractions, capacitance parameter extractions, and noise parameter extractions
*Parameter extraction methods for second order model parameters, local optimization and global optimization
*Model parameter verification using circuit modules digital and analog applications
*Conclusions

12:05 p.m. **4. Electrical Linewidth and Overlay - Loren W. Linholm, NIST**
*Introduction
*Electrical Linewidth
Background
Electrical Structure: Cross-Bridge Resister
Measurement Results and Comparisons
Enhancements
Future Applications
*Electrical Overlay
Background
Electrical Structures: van der Pauw, Sliding Wire, MOATS
Measurement Results and Comparisons
Future Applications
*Summary
12:55 p.m. Hosted Lunch

2:25 p.m. **5. TCAD and Its Practical Applications - Hiroo Masuda, STARC**
*Introduction
TCAD roles, previous and now.
*Problems
Process modeling problems, methodology and metrology of using TCAD.
*One of the Goals: TCAD Application
TCAD application flows and calibration strategy
*Predictive Circuit Model Parameter Generation
Examples of the practical applied TCAD
*Worst-Case Design Applications
TCAD and statistical worst-case definition methodology
*Future Application and Goals
Application technologies in 0.10mm technology-node
*Conclusions
TCAD, still more worthwhile even in DSM (Deep-sub-micron) era
3:15 p.m. **6. Fully-Depleted CMOS/SOI Device Characterization for Low Power Application - Yasuhiro Sato, NTT Lab**
*Why SOI?
*Fully-depleted vs. partially-depleted SOI devices
*Features of fully-depleted SOI devices
*Application to low-power high-speed LSI
*Summary

4:05 p.m. Break - 30min-

4:35 p.m. **7. Basics of RF/MW Measurement Using Vector Network Analyzer - Toru Sugawara, Cascade Microtech Japan**
*Linear and Non-Linear Behavior of RF/MW Devices
*What is S-Parameter?
*What is Vector Network Analyzer?
*VNA Calibrations
*On-Wafer RF/MW Device Measurement
*Summary

5:25 p.m. **8. Reliability issue for chip reliability - Masakazu Shimaya, NTT Electronics**
*Basic reliability concept
*Device reliability
Hot-carrier, TDDB, Radiation damage, Soft error
*Metal interconnection reliability
Electro and Stress Migration
*Reliability assurance
Burn-in, Screening
*Over stress protection
ESD, EOS

6:15 p.m. Closing Remarks
6:20 p.m. Close

ICMTS 2001 Tutorial Lecturer Biography

Yoshiaki Hagiwara

Yoshiaki Hagiwara received BS, MS and PhD from CalTech, in 1971,1972 and 1975 respectively and stated his career as a research engineer in a CCD camera project. He was also engaged in developing SRAM chips, which opened SONY's business on Cache SRAM nowaday. Yoshiaki Hagiwara has served ISSCC, and VLSI Circuit and Technology Symposia (1989-1994). He also served as the WG2 Convenor (1993-1996) of the International Electrotechnical Commission (IEC) Technical Committee TC47/SC47A. Currently he is serving the IEEE Computer Element MESA/VAIL workshops since 1991, and ICMTS since 1988. He also served as a Visiting Professor of Applied Physics and Electrical Engineering at CalTech, Pasadena, California for 1998 to 1999. Currently he is serving as the technical engineering manager in SNC Strategic Planning Department, Sony Corporation.

Hitoshi Aoki

Hitoshi Aoki received the BSEE from Musashi Institute of Technology in 1983. He worked at YHP from 1983 to 1991, where he was involved in several kind of jobs. In 1991, he joined Hewlett-Packard in U.S. as an R&D engineer. From 1994 to 1996, he was at the ULSI Research Laboratory of HP Laboratories as a member of research staff. He is currently with Design Technology group, Agilent Technologies Japan Ltd. as a managing consultant in the area of semiconductor and microwave EDA. His research interest includes compact modeling of any semiconductor devices and device characterizations. He authored and co-authored one book titled "Silicon FET Modeling" and 13 of technical papers. He is a senior member of IEEE and a member of IEICE and SID. He is listed on "Who's who in Science and Engineering, America".

Loren W. Linholm

Loren W. Linholm received the B.S. degree in Electrical Engineering from the University of California, Berkeley, in 1968 and the M.S. degree in Electrical Engineering from the University of Maryland, College Park, Maryland, in 1973. He has been employed by the Naval Missile Center. Point Mugu, California, and the Department of Defense, Ft. Meade, Maryland, and since 1978, the Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, Maryland. He heads the Integrated Circuits Technology Group, which is responsible for designing, developing, and evaluating measurements methods for evaluating silicon integrated circuits, manufacturing tools, and processes with emphasis on test structures, associated data analysis techniques, novel sensors, and advanced microelectromechanical systems. Mr. Linholm is a member of the IEEE Electron Devices Society and a co-founder of the International Conference on Microelectronic Test Structures.

Hiroo Masuda

Hiroo Masuda received the B.S. degree in applied physics and Dr. of Engineering in electric system from Tokyo Institute of Technology, Tokyo, in 1970 and 1979, respectively. In 1970, he joined Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan. From 1982 to 1987 he conducted research on the world's first three dimensional device simulator which led to a practical use in MOS LSI design including alpha-particle induced soft-error analysis of dynamic memories. From 1988 he engaged in research on a MOS device modeling, and management of modeling group for circuit simulation. From 1991 to 1999, he was with Device Development Center, Hitachi Ltd., where he worked on Computer Aided Engineering for VLSI's, including TCAD application methodology and statistical yield modeling and metrology. He is now with STARC (Scientific Technology Academic Research Center), Technology Development Department, Physical Design Group as a Senior Manager and Group Leader, where he is engaged in research and development works on SoC chip-implementation and circuit design for deep sub-micron VLSIs. Dr. Masuda is senior member of the IEEE and a member of the Japan Society of Applied Physics and Institute of Electronics, Information and Communication Engineers of Japan.

Yasuhiro Sato

Yasuhiro Sato received the B.S. and M.S. degrees in chemistry from the University of Tokyo, Tokyo, Japan, in 1987 and 1989, respectively. In 1989, he joined the Nippon Telegraph and Telephone Corporation (NTT) LSI Laboratories, Atsugi, Kanagwa, Japan. From 1989 to 1992, he worked on the research of Si surface chemistry. From 1992, he has been engaged in the research of Ultrathin-film CMOS/SOI device technology and their applications.
Mr. Sato is a member of the IEEE, the Japan Society of Applied Physics, and the Institute of Electronics, Information and Communication Engineers of Japan.

Toru Sugawara

Toru Sugawara graduated from Waseda University, Japan and joined Hewlett Packard Japan in 1982. For 8 years worked for Hewlett Packard Japan as a Sales Engineer. And from 1990 to 1998 worked as a Marketing Engineer for Microwave Instruments including Vector Network Analyzer. In 1998, he joined Cascade Microtech Japan as a Technical Support Specialist for Microwave Measurements. His works is specially focusing on On-Wafer Microwave Measurements Support for Japanese Semiconductor Customer.

Masakazu Shimaya

Masakazu Shimaya was born in Japan on January 19, 1956. He received the B.S., M.S. and Ph.D. degrees in electrical engineering from Kyushu University, Fukuoka, Japan, in 1978, 1980, and 1988, respectively. In 1980, he joined the Electrical Communication Laboratories, Nippon Telegraph and Telephone Public Corporation, Tokyo, Japan. He was engaged in the research on radiation effects in MOS devices and the research for reliability of SOI devices from 1980 to 1998. In 1999, he joined the NTT electronics. His current work is the reliability assurance for high-speed optical communication modules. Dr. Shimaya is a member of the Institute of Electronics, Information, and Communication Engineers of Japan. He was a Technical Program Committee member of the ICMTS from 1995 to 1999.

TECHNICAL PROGRAM SCHEDULE
TUESDAY, MARCH 20

8:00 a.m.-5:00 p.m. Registration
9:00 Opening Remarks
Takashi Ohzone, General Chairman
Hiroaki Hazama, Technical Program Chairman

SESSION 1: MATCHING I

9:10 a.m. - 10:10 a.m.
Co-Chairs: Hans P. Tuinhout, Philips
Junko Komori, Mitsubishi

9:10 1.1 **Evaluation of the Impact of Mechanical Stress on CMOS Device Mismatch**
U. Schaper, C. Linnenbank, U. Kollmer, H. Mulatz, R. Schmidt, R. Tilgner and R. Thewes, Infineon Technologies AG, Germany

Mechanical stress occurs during packaging and frontend processing. The impact of mechanical stress on device mismatch is investigated. The measurement setup is presented which uses a beam bending technique to apply mechanical stress. The characterization of mismatch is based on a test macro for the extraction of pair mismatch and long distance mismatch. It is found that the device characteristics change when stress is applied dependent on the device orientation with respect to the stress direction. In the processes investigated no influence of mechanical stress is observed on the pair-mismatch of directly neighboring devices.

9:30 1.2 **Effect of Substrate Voltage and Oxide Thickness on MOSFET Matching Characteristics for 0.18µm CMOS Technology**
*R. Difrenza, P. Llinares, E. Granger, H. Brut and *G. Ghibaudo, ST Microelectronics, *LPCS ENSERG, France*

Matching characterization has been performed on 0.18µm CMOS technology for different substrate voltage values V_b and for various oxide thicknesses T_{ox}, in order to determine the origin of the difference between experimental results and matching theory. Both experimental results and simulations outline an obvious tendency of mismatch to increase with T_{ox} and V_b. Moreover, this study demonstrates that threshold voltage mismatch is entirely attributed to the statistical fluctuations of channel dopant number. Nevertheless, Poisson distribution of channel dopant number fluctuations does not explain the absolute amplitude of threshold voltage mismatch which could be either related to channel dopant clustering or to deviation from Poisson statistical law.

9:50 1.3 **High Frequency MOS Transistor Matching Measurements for the Determination of Mixer Port Crosstalk**
S. Laursen, Aalborg University, Denmark

The cancellation of port crosstalk in an integrated mixer is limited by random transistor mismatch. A method for calculating this crosstalk at gigahertz frequencies is presented. The crosstalk is calculated from the differences between measured transistor scattering parameters for a pair of identical devices. Measurement results give guidance on how to select transistor widths to obtain a required second order intercept point of the mixer.

10:10 a.m. - 10:40 a.m. Break

SESSION 2: PARAMETER EXTRACTION

10:40 a.m. - 12:00 a.m.
Co-Chairs: Colin McAndrew, Motorola
Charles N. Alcorn, Lockheed Martin Federal Systems

10:40 2.1 **A New Leff Extraction Approach for Devices with Pocket Implants**
T.S. Hsieh, Y.W. Chang, W.J. Tsai and T.C. Lu, Macronix International Co., Taiwan R.O.C.

In this paper, we propose a new approach to extract L_{eff} of MOSFET. C_{gb} is measured and L_{eff} can be extracted from two devices with different gate lengths. It has been verified by both experimental data and simulation. The extracted L_{eff} is very close to the metallurgical channel length. In addition, compared to S&R method, which fails to extract the accurate L_{eff} of devices with pocket implants, our approach still works well for the devices with pocket implants even down to 0.1µm regime.

11:00 2.2 **Statistical SPICE Analysis of a 0.18µm CMOS Digital/Analog Technology During Process Development**
*N.S. Rankin, *C. Ng, *L.S. Ee, *F. Boyland, *E. Quek, *L.Y. Keung, A.J. Walton and *M. Redford, The University of Edinburgh, Scotland, *Chartered Semiconductor Manufacturing Ltd., Singapore*

This paper gives details of a methodology to extract statistical SPICE models on a developing deep sub micron CMOS technology. The approach uses a TCAD framework which integrates process, device, parameter extraction, and statistics software. The TCAD tools are calibrated by physical and electrical measurements on transistor test structures with different channel widths and lengths. Once calibrated, a Monte Carlo experiment is run on all process control input parameters with realistic variations and the results then compared to in-line and E-test distributions. When satisfied that the variance in TCAD and measured distributions match the framework can be used to extract BSIM3v3.2 parameters to generate statistical models. Multivariate statistics is used to determine the key process parameters which need to be controlled in-line to minimize device variation.

11:20 2.3 **A New Test Structure for Parasitic Resistance Extraction of Bipolar Transistors**
*M. Linder, *F. Ingvarson, *K.O. Jeppson, S.-L. Zhang, J.V. Grahn and M. Ùstling, Royal Institute of Technology(KTH), *Chalmers University of Technology, Sweden*

A new test structure is proposed which allows for fast and accurate extraction of the emitter, base and collector resistances in bipolar transistors. The structure is designed as a regular transistor, equipped with two base terminals and two collector terminals. The extracted resistances agree well with those extracted by other methods. The use of the additional collector contact also enables monitoring of the onset of the base push-out effect.

11:40 2.4 **A Procedure for Characterizing the BJT Base Resistance and Early Voltages Utilizing a Dual Base Transistor Test Structure**
*F. Ingvarson, *M. Linder, K.O. Jeppson, *S.-L. Zhang, *J.V. Grahn and *M. Ùstling, Chalmers University of Technology, *Royal Institute Technology(KTH), Sweden*

A procedure for measuring the bipolar transistor base resistance and voltage dependent Early voltages is proposed. A transistor test structure with two separated base terminals is used together with measurements in the cut-off region. This approach makes it possible to measure the base resistance without having to account for current crowding, base conductivity modulation or base push-out.

12:00 a.m. - 1:30 p.m. Luncheon

SESSION 3: DEVICE CHARACTERIZATION I

1:30 p.m. - 2:50 p.m.
Co-Chairs: Kunihiro Asada, Univ. Tokyo
Loren W. Linholm, NIST

1:30 3.1 **FeRAM Retention Analysis Method Based on Memory Cell Read Signal Voltage Measurement**
*H. Koike, *K. Amanuma, T. Miwa, J. Yamada and *H. Toyoshima, NEC Corporation, *NEC Electron Devices, Japan*

A novel retention analysis method for ferroelectric random access memory (FeRAM) has been developed, in which read signal voltages from memory cells are measured. It employs on-chip sample/hold circuits, an off-chip A/D converter, and memory LSI testing equipment. FeRAM chip reliability is estimated on the basis of FeRAM read signal voltages after retention periods of 1 day and longer. When used as a tool to estimate long-term data retention in FeRAM chips, and when used to analyze fluctuations in FeRAM cell characteristics, this method can be of significant help in improving the reliability of FeRAM chips.

1:50 3.2 **A New Method for Measuring the Coupling Coefficient of a Split-Gate Flash EEPROM without an Additional Test Structure**
H. Fujiwara, M. Arimoto, T. Kaida, S. Sudo, K. Kurooka, H. Nagasawa, T. Hiroshima and K. Mameno, Sanyo Electric Co. Ltd., Japan

A new method for measuring the actual coupling coefficient of a split-gate Flash EEPROM whose floating gate voltage is controlled by the source voltage is presented, which uses no additional test structure or non-floating gate TEG. In this method, the subthreshold current is measured twice as the source voltage is increased after the control gate transistor has turned on sufficiently. After the drain voltage is slightly altered (ΔV), the subthreshold curve is $\alpha \cdot \Delta V$ shifted from the previous one. The coefficient a obtained by this method agrees with the value obtained by the well known subthreshold slope method using a test structure.

2:10 3.3 **A Novel Approach to the Estimation of Confidence Limits for BJT Model Sets Using a Bootstrap Technique**
*D. MacSweeney, M. Riordan, K. McCarthy, L. Floyd, L. Sattler, A. Mathewson, *J. Power and *S. Kelly, University College Cork, *Analog Devices, Ireland*

In this paper, a novel method for the estimation of confidence intervals of extracted parameter values is proposed. The technique is based on a Bootstrap method which evaluates the error distributions associated with parameter extraction techniques. These in turn allow confidence intervals to be estimated. Results are presented for DC, capacitance and high frequency measurements.

2:30 3.4 **Limitations of the Two-Frequency Capacitance Measurement Technique Applied to Ultra-Thin SiO_2 Gate Oxides**
*A. Nara, N. Yasuda, H. Satake and *A. Toriumi, Toshiba Co., *University of Tokyo, Japan*

An improved C-V extraction guideline for ultra-thin MOS structures is proposed, in order to overcome the limitations of the conventional two-frequency C-V technique. We have experimentally demonstrated, down to 1.8 nm gate oxides, that dissipation should be less than 1.1 at least at one of the two measurement frequencies, in order to reduce the measurement error of the gate oxide thickness below 4%. For gate oxides thinner than 1.8 nm, although fitting of the frequency dependencies of capacitance and dissipation extends the applicability of multi-frequency C-V techniques, this is only possible to perform measurements at frequencies above 1 MHz with additional complications such as extra inductance effects.

2:50 p.m. - 3:20 p.m. Break

SESSION 4: POSTER SESSION

3:20 p.m. - 4:25 p.m.
Co-Chairs: Anthony J. Walton, Univ. of Edinburgh
Takashi Ohzone, Toyama Prefectural Univ.

3:20 4.1 **C-V Extraction Method for Gate Fringe Capacitance and Gate to Source-Drain Overlap Length of LDD MOSFET**

J.-R. Kahng, J.-W. Moon and J.-H. Kim, Hyundai Electronics Industries Co. Ltd., Korea

Gate to source-drain overlap length becomes a more critical quantity in device modeling as the channel length of transistor decreases. In this paper, we present an improved capacitance-voltage measurement method for the determination of gate to source/drain overlap length and gate sidewall fringe capacitance, which can be applicable to deep sub-micrometer devices. To achieve the goals, we take into account the effects of parasitic components, which mainly come from measurement equipment, test structures, and the device itself such as the gate fringe capacitance.

3:25 4.2 **Comparison of Interface Trap Density Measured by Capacitance /Subthreshold/Charge-Pumping Methods for n-MOSFETs with Si-Implanted Gate-SiO_2**

*T. Matsuda, R. Takezawa, K. Arakawa, M. Yasuda, T. Ohzone and *E. Kameda, Toyama Prefectural University, *Toyama National College of Technology, Japan*

The effects of Si implantation on interface trap density D_{it} distribution in the energy gap for n-MOSFETs fabricated by various Si-implantation doses and energies are analyzed by the three measurement methods; *(I)* high-low frequency capacitance, *(II)* subthreshold current, and *(III)* charge pumping. Although it can provide D_{it} distribution across the bandgap, method *I* may cause an underestimation of D_{it}. Method *II* with a simple DC measurement gives a D_{it} estimation with a reasonable accuracy. According to the linearity of Si-dose dependence of D_{it}, method *III* must be the most reliable method in our experiments.

3:30 4.3 **Statistical Modeling Techniques: FPV vs. BPV**

N. Telang and J.M. Higman, Motorola Inc., USA

Modeling the statistical variations in device and circuit performance is the ultimate goal of any statistical modeling technique. For a technology under development, where limited device data and almost no circuit data is available, this can be challenging task. In this paper we have compared two known statistical modeling methods, namely, the forward propagation of variance (FPV) method and the backward propagation of variance (BPV) method, using a limited data set. We demonstrate that even under these conditions the BPV can be used effectively to generate models that more accurately reflect the statistics of the process.

3:35 4.4 **Mis-Match Characterization of 1.8V and 3.3V Devices in 0.18μm Mixed Signal CMOS Technology**

T.-H. Yeh, J.CH. Lin, S.-C. Wong and J. Sun, Taiwan Semiconductor Manufacture Company, Ltd., Taiwan R.O.C.

This paper studies the mis-match characteristics of 1.8V and 3.3V multiple V_t devices, including nominal V_t, medium V_t and native devices in 0.18μm Mixed Signal CMOS technology for precision analog design. Three test structures, cross couple, stripe pair and parallel patterns, are presented to investigate the structure dependent mis-match behaviors. Matching characteristics of four analog parameters: V_t, I_{dsat}, b and G_{ds}, are investigated in terms of device size, layout configuration and process sensitivity. Additional contribution of local edge roughness on current mis-match has been verified, in addition to global distortion of gate oxide thickness and substrate doping concentration.

3:40 4.5 **Direct Extraction of Equivalent Circuit Model Parameters for HBTs**

R. Uscola and M. Tutt, Motorola, Inc., USA

A new analytical method for the direct extraction of small-signal equivalent circuit model parameters for Gallium Arsenide hetero-junction bipolar transistors has been developed. This new method completely eliminates the need for parameter optimization and provides the best agreement between modeled and measured s-parameters ever reported. The resulting models have been shown to be very accurate over the test frequencies from 0.5 GHz to 20 GHz. This analytical method, which uses a hybrid T equivalent circuit, provides unique and meaningful circuit model parameters.

3:45 4.6 **Modeling of Non-Linear Polysilicon Resistors for Analog Circuit Design**

R. Virkus, D. Weiser and K. Green, Texas Instruments Inc., USA

This paper focuses on modeling the effect of the silicide-silicon interface within a polysilicon resistor head that is typical of silicon process technologies used for precision analog circuit design. This interface introduces resistor non-linearity over bias which can be detrimental to circuit performance, e.g., by manifesting circuit distortion. A non-linear resistor model suitable for high-frequency circuit simulation and a methodology for obtaining model parameters are provided.

3:50 4.7 **Effective-Channel-Length Extraction for Double-Diffused MOSFETs**

*S. Ichikawa, Y. Eshima, K. Terada and *T. Matsuki, Hiroshima City University, *NEC Corporation, Japan*

A new method to extract the effective channel length for a double-diffused DMOSFET is proposed. This method models the DMOSFET by two MOSFETs serially connected each other. The effective channel lengths for these two MOSFETs are extracted from the single relation between the effective channel length and the gate voltage for the DMOSFET extracted by the conventional method.

3:55 4.8 **A Study of Measurement System Noise for Sensitive Soft Breakdown Triggering**

J. Schmitz and H.P. Tuinhout, Philips Research Laboratories, The Netherlands

We present a simple and effective method to determine the short term repeatability of current measurements on a parametric tester. The application of this result to Constant Voltage Stress is discussed, and we show that an automatic tester can be used for triggering on soft breakdowns of thin gate oxides under stress.

4:00 4.9 **Oxide Thickness Dependence of Nitridation Effects on TDDB Characteristics**
M.K. Mazumder, A. Teramoto, J. Komori and Y. Mashiko, Mitsubishi Electric Corp., Japan

Using wet oxide thicknesses ranging from ~50 to ~80 Ê effects of nitridation on time-dependent- dielectric breakdown (TDDB) characteristics have been investigated. Results show that the capacitors with nitrided oxide have shorter t_{BD} up to the thickness of ~60 Ê but a turn-around behavior was found for ~50 Ê nitrided oxide. It can be suggested that a turn-around behavior of t_{BD} of nitrided wet oxide of ~50 Ê comparing to the wet oxide seems to be due to the more nitrogen concentration in the interface than the thick wet oxide of above 60 Ê for the same nitridation conditions.

4:05 4.10 **A General Procedure for High-Frequency Noise Parameter De-Embedding of MOSFETs by Taking the Capacitive Effects of Metal Interconnections into Account**
C.-H. Chen and M.J. Deen, McMaster University, Canada

A general procedure by using one "OPEN" and two "THRU" dummy structures for the noise parameter de-embedding of MOSFETs based on cascade configurations is presented. This technique does not require any equivalent circuit modeling of probe pads or metal interconnections and is verified by RF noise measurements. This procedure is also valid for designs with long interconnections at the input and output ports of a device-under-test, and for devices operated at frequencies of several tens of GHz.

4:10 4.11 **A New Approach to Characterize Substrate Losses of On-Chip Inductors**
K. Schimpf, B. Benna and D. Proetel, Texas Instruments Deutschland GmbH, Germany

A new approach to characterize substrate losses of on-chip inductors is presented, that attributes the losses to a frequency dependence of the series resistor Rs. The technique to extract $R_s(f)$ from y-parameters is described in detail. To demonstrate the important role of de-embedding for accurate parameter extraction several de-embedding procedures are depicted and compared. As an example, results of a 5-turn inductor will be discussed.

4:15 4.12 **Effect of the Electrical Stress on the Frequency Performance of 0.18 µm Technology NMOSFETs**
S. Naseh, J. Deen and O. Marinov, McMaster University, Canada

The effect of electrical stress on transit frequency f_T in NMOSFETs, fabricated with 0.18 µm CMOS technology, is studied. Multi-finger transistors with dimensions W=120 µm, L=0.18-1 µm, oxide thickness of 40 angstrom are measured in frequency range of 50 MHz to 10 GHz. f_T was obtained after de-embedding the effect of the connection pads. Significant degradation in the NMOSFETs is caused at drain voltages above 3.5 V and drain currents of at least 0.5 mA. f_T and gm decrease by increasing the stress. Two slopes were found in the variation of f_T versus the stress duration.

4:20 4.13 **A New Robust On-Wafer 1/f Noise Measurement and Characterization System**
*A. Blaum, O. Pilloud, G. Scalea, J. Victory and *F. Sischka, Motorola Inc., Switzerland, *Agilent Technologies, Germany*

Performing accurate, robust and repeatable 1/f measurement is critical to meaningful modeling and simulation of 1/f noise. Accurate measurement and modeling of 1/f noise of such devices as deep submicron CMOS, HBTs and RF passive components is critical to design of RF circuits. In this paper, a new on-wafer flicker noise characterization system, well suited for technology characterization, is presented.

4:25 p.m. Exhibition Presentation

WEDNESDAY, MARCH 21

8:30 a.m. Registration

SESSION 5: RF

9:00 a.m. - 10:20 a.m.
Co-Chairs: **Satoshi Habu,** Agilent Technologies Japan
Kazunari Honma, Sanyo

9:00 5.1 **Extraction of the Induced Gate Noise, Channel Thermal Noise and Their Correlation in Sub-Micron MOSFETs from RF Noise Measurements**
*C.-H. Chen, M.J. Deen, *M. Matloubian and *Y. Cheng, McMaster University, Canada, *Conexant Systems Inc., USA*

An extraction method to obtain the induced gate noise ($i_g i_g$*), channel thermal noise ($i_d i_d$*) and their cross-correlation ($i_g i_d$*) in sub-micron MOSFETs directly from d.c., scattering and RF noise measurements has been presented and verified by measurements. In addition, the

extracted induced gate noise, channel thermal noise and their correlation versus frequency, bias and channel length characteristics have been presented, respectively.

9:20 5.2 **Test Structures and Techniques for On-Wafer CMOS TRL Calibration**
M.B. Jenner and T.E. Kolding, Aalborg University, Denmark

In this paper, we demonstrate for the first time a TRL calibration kit fabricated in CMOS technology. To fulfill a basic requirement of high probe-isolation of the TRL method, we have based all fabricated calibration standards on a shield-based measuring fixture that heavily reduces the effects of the semiconducting substrate. We analyze the electrical performance of the standards, including their accuracy, and the performance of CMOS-based TRL calibration is compared to a reference calibration based on the LRRM technique and a high-precision impedance standard substrate. We find that CMOS TRL calibration is indeed feasible for measurements in the low-gigahertz frequency range but not without implementation problems.

9:40 5.3 **Efficient Parameter Extraction Techniques for a New Surface-Potential-Based MOS Model for RF Applications**
*W. Liang, *R. van Langevelde, K.G. McCarthy, *D.B.M. Klaassen and A.Mathewson, University College Cork, Ireland, *Philips Reserch Laboratories, The Netherlands*

Efficient parameter extraction techniques for a new surface-potential-based MOS model are outlined. The new model is suitable for RF CMOS design because it has improved modeling of surface potential, mobility and conductance. The extraction techniques are based on analytical manipulation of the model equations and allow parameters to be extracted using as few as 12 measurements per device.

10:00 5.4 **Determining the Inductance of a Through Substrate Via Using Multiple On-Wafer Test Approaches**
R. Uscola and M. Tutt, Motorola, Inc., USA

Four on-wafer test approaches for determining the inductance, L_{via}, of through-substrate vias used in Gallium Arsenide monolithic microwave integrated circuits have been implemented and compared. All of the approaches yielded similar results enabling an accurate estimate for L_{via}. The implementations and features of the approaches are explained.

10:20 a.m. - 10:50 a.m. Break

SESSION 6: PROCESS CHARACTERIZATION

10:50 a.m. - 12:10 p.m.
Co-Chairs: **Akella Satya,** KLA-Tencor
Bill Verzi, Agilent Technologies

10:50 6.1 **Test Chips for Evaluating Strong Phase Shift Lithography**
R.A. Ashton, B.C. Kane, J.W. Blatchford and D.M. Shuttleworth, Lucent Technologies, USA

Test structures are presented for the evaluation of phase shift lithography on the gate level of a CMOS technology. The structures address the measurement of phase shift printed line width, the evaluation of transistors as a function of phase shifter geometry and the detection of misalignment of contact windows to phase shift printed gate.

11:10 6.2 **Use of Electrical Test Structures to Characterize Trench Profiles Etched on SOI Wafers**
*N. Guillaume, *J. Kiihamaki, *J. Karttunen and *H. Kattelus, The George Washington University, USA, *VTT Electronics, Finland*

This paper demonstrates the use of electrical test structures patterned on Silicon-On-Insulator (SOI) material to evaluate the performance of plasma etching process. Electrical characterization is performed by capacitance and resistance measurements. They are used to compare the etch results of slightly varied plasma etch processes. Subtle differences in submicron trench profiles are very difficult to distinguish and quantify when using scanning electron microscopy (SEM). The electrical measurements can reveal these differences which facilitates the etch process development. Experimental results are presented and compared to cross-section SEM analysis. The end goal of the development of test structures presented here is to establish a fast, low cost and non-destructive method to characterize and optimize deep trench etching process cycles needed in the fabrication of micromachined devices.

11:30 6.3 **Process Monitoring and Defect Characterization with Single Photon Avalanche Diodes**
*J.C. Jackson, *A.P. Morrison, **W.R. Harrell and B. Lane, National Microelectronics Research Centre, Ireland, *University College Cork, Ireland, **Clemson University, USA*

Silicon avalanche photodiodes operated in geiger mode above the breakdown voltage are extremely sensitive to defects within the depletion region. This dark count can be used as a convenient process monitor and characterization tool for single photon avalanche diodes (SPAD). Qualitative analysis of the defects within the depletion region and comparison to dark counts of the SPAD along with the test structures and test methodology needed will be presented.

11:50 6.4 **A New Method for Analyzing Boron Penetration and Gate Depletion Using Dual-Gate PMOSFETs for High Performance G-bit DRAM Design**
*N. Takaura, *R. Nagai, H. Asakura, *S. Yamada and S. Kimura, Hitachi Ltd., *NEC Hitachi Memory Inc., Japan*

We have developed a new method for a precise analysis of boron penetration and gate depletion using N+ and P+ dual-gate PMOSFETs. The impact of boron penetration and gate depletion on V_{th} shift and fluctuation was simply revealed by use of an N+gate PMOSFET immune to both boron penetration and gate depletion. We found that the V_{th} fluctuation of a P+ gate PMOSFET is dominated by boron penetration, and that it is possible to select fabrication processes that are robust to V_{th} fluctuation for high performance G-bit DRAM design.

12:10 p.m. - 1:30 p.m. Luncheon

1:30 p.m. - 1:40 p.m. ICMTS 2002

SESSION 7: INTERCONNECT

1:40 p.m. - 3:00 p.m.
Co-Chairs: **Christopher Hess,** PDF Solutions
Shigeru Okamura, Fujitsu

1:40 7.1 **Contact Resistance Measurement of a 130nm-Diameter Poly-Si Plug on a Lightly Doped Single Diffusion Region in Giga-bit DRAMs**
N. Kasai, H. Koga and Y. Takaishi, NEC Electron Devices, Japan

A practical method to extract contact resistance of a phosphorus-doped poly-Si plug on a lightly doped diffusion in giga bit DRAM memory cells is proposed. Resistance of the 130nm-diameter contact is experimentally obtained by the substrate bias change measurement, which can separate resistance of a bias-dependent lightly doped diffusion layer from total contact chain resistance. This method is an effective tool for the technology development of ways of forming low resistance contacts in giga bit DRAMs.

2:00 7.2 **New Test Chip for Electrical Linewidth of Copper- Interconnect Features and Related Parameters**
*M.W. Cresswell, *N. Arora, R.A. Allen, C. Richter, **A. Gupta, L.W. Linholm and ***P. Bendix, NIST, *Simplex Solutions, Inc., **Chartered Semiconductor, ***LSI Logic Inc., USA*

This paper reports a new electrical test structure for measuring the barrier-layer thickness and total physical linewidth of copper-interconnect features. The test structure has four reference segments of different drawn linewidths. The linewidth extraction algorithm has been extensively tested on *V/I* and sheet-resistance measurement simulations. A second test structure for measuring conducting feature and interlayer dielectric (ILD) thickness by use of the charge-based capacitance method (CBCM) is described. Test-chips featuring both of these structures have been patterned in aluminum using a standard 0.18 μm CMOS process and preliminary results are reported here.

2:20 7.3 **Test Structure and Method for Capacitance Extraction in Multi-Conductor Systems**
**B. Ward, J. Bordelon and B. Tranchina, TestChip Technologies Inc., *The University of Texas, USA*

A charge based capacitance measurement (CBCM) method is generalized to a multi-conductor system using a novel test methodology and test structure. The test structure and approach is applicable for characterizing multi-interconnect configurations representative of design applications, providing a powerful tool for experimental characterization. The approach is applicable to an arbitrary number of conductors. Manufacturing variations and process-induced changes to capacitance are readily measured using this technique.

2:40 7.4 **Evaluation of the Issues Involved with Test Structures for the Measurement of Sheet Resistance and Linewidth of Copper Damascene Interconnect**
S. Smith and A.J. Walton, The University of Edinburgh, Edinburgh, Scotland

The effect of the barrier layer and dishing in copper interconnect causes extra difficulties in measuring sheet resistance and linewidth when compared with equivalent measurements on aluminum tracks. This paper examines these issues and, for the first time, quantifies the effects of diffusion barrier layers and CMP dishing on the extraction of R_S from Greek cross type structures and the effect this has on linewidth measurement.

3:00 p.m. - 3:30 p.m. Break

SESSION 8: MATCHING II

3:30 p.m. - 4:50 p.m.
Co-Chairs: **Yoichi Tamaki,** Hitachi
Naoki Kasai, NEC

3:30 8.1 **Impact of Transistor Noise on High Precision DC Parametric Matching Measurements**
*H.P. Tuinhout, J.H. Klootwijk, *W.C. Goeke and *L.K. Stauffer, Philips Research Laboratories, The Netherlands, *Keithley Instruments, USA*

Utilizing the correlation of fluctuations of the drain and source currents of a MOSFET, this paper demonstrates that low frequency transistor noise (and Random Telegraph Signals) can be much higher than the noise contribution of bench-top DC semiconductor characterization systems. These results provide valuable insights into the limits of high precision parameter fluctuation (matching) measurement methods.

3:50 **Mismatch Characterization and Modelization of Thin Films**

8.2 **Resistors for Wireless Applications**
H. Thibieroz, M. Raymond, T. Remmel and P. Shaner, Motorola, USA

A new TaN thin film resistor (TFR) technology for application in analog and mixed signal Si-IC technologies has been characterized for mismatch and noise behavior. Because of excellent matching properties, optimal matching methodology and algorithms had to be developed to evaluate mismatch accurately. This analysis is performed for different layout configurations and temperatures. Based on these mismatch variations, an optimum layout set has been generated for design applications. Using this set, different models have been implemented and evaluated. In contrast to this TaN TFR, other resistors such as poly-silicon are found to exhibit a much higher mismatch. Correlation between thin film resistor mismatch and its crystal structure is therefore being investigated. Flicker noise measured on the TaN resistor confirms this hypothesis by showing a very low level of noise similar to metal resistors.

4:10 8.3 **A Simple Characterization Method for MOS Transistor Matching in Deep Submicron Technologies**
*J.A. Croon, M. Rosmeulen, S. Decoutere, *W. Sansen and H.E. Maes, IMEC vzw, *K.U. Leuven, Belgium*

This paper discusses two aspects of mismatch characterization of MOS transistors. First we present our new and simple four parameter mismatch model. This model is extensively tested on a 0.18 μm CMOS technology. Bulk bias dependence is modeled physically without the introduction of an extra parameter. Secondly we test the repeatability of our measurement system and parameter extraction, which both turn out to be good.

4:30 8.4 **Resistor Matching Characterization for Process Development Using D/A Converter**
*S. Katakam, B. Tranchina, J. Bordelon, W. Choi, *A. Ramaswamy and **S. Chu, TestChip Technologies Inc., USA, *is currently with Sun Microsystems Inc., **Chartered Semiconductor Inc., Singapore*

In-depth process evaluation and robust device models are essential for integrating analog circuits into logic processes. There is an increasing emphasis on process optimization in the early stages of technology development. This work will present a technique for resistor mismatch characterization using a D/A converter (DAC) test circuit. This design offers a fast, wafer-level test of large resistor arrays representative of converter applications allowing the designer to evaluate the impact of array area, resistor size, and resistor design on resolution limits. The test methodology is tailored for a production test environment.

4:50 p.m. End of Session 8

7:00 p.m. Banquet (Room Rainbow, 16F South Wing, Portopia Hotel)

9:00 p.m. End of Banquet

THURSDAY, MARCH 22

8:30 a.m. Registration

SESSION 9: RELIABILITY

9:00 a.m. - 10:20 a.m.
Co-Chairs: **Robert Ashton,** Lucent Technologies/Bell Labs.
Michael W. Cresswell, NIST

9:00 9.1 **A New Test Structure to Measure Precise Location of Hot-Carrier-Induced Photoemission Peak from Gate Center of Subquarter-Micron n-MOSFETs**
*M. Funada, T. Matsuda, T. Ohzone, *S. Odanaka, **K. Yamashita, **N. Koike and **K. Tatsuuma, Toyama Prefectural University, *Osaka University, **Matsushita Electronics Corp., Japan*

A new test structure, which has a 0.5 μm line & space polysilicon pattern, is proposed for hot carrier analysis of subquater micron devices. Hot-carrier-induced photoemission effects were measured with the photoemission microscope with a liquid N_2 cooled CCD imager. We successfully measured a peak position of photoemission intensity from the center of MOSFET's gate with a distance resolution less than ˜24 nm.

9:20 9.2 **An Accurate Discrimination Method of Gate Oxide Breakdown Positions by a New Test Structure of MOS Capacitors**
H. Uchida, S. Ikeda and N. Hirashita, Oki Electric Industry Co. Ltd., Japan

A new test structure of MOS capacitors for discrimination of gate oxide breakdown positions is proposed. The characteristic of this test structure is that Al marks to discriminate the positions are lined up diagonally. Oxide breakdown spots determined by using the test structure are investigated by cross-sectional transmission electron microscopy (XTEM) for a 5-nm-thick gate oxide. From these observations, this test structure is found to be useful for XTEM specimen preparation to analysis degradation phenomena of thin gate oxides.

9:40 9.3 **An Improved Experimental Setup for Electrostatic Discharge (ESD) Measurements Based on Transmission Line Pulsing Technique**
*J.C. Lee, *R. Young, J.J. Liou, *G.D. Croft and *J.C. Bernier, University of Central Florida, *Intersil Corp., USA*

Transmission line pulsing (TLP) is a useful technique to characterize electrostatic discharge (ESD) events in semiconductor devices. The pulse waveforms generated by a typical TLP setup, however, are often distorted and oscillatory. In this paper, a new and simple experimental setup

is developed to improve the shape of the TLP waveforms and thus to increase the effectiveness of the TLP technique. Experimental results obtained from the conventional and improved setups are presented and compared.

10:00 9.4 **Die Cracking Evaluation and Improvement in ULSI Plastic Package**
*K.Y. Chou, *M.J. Chen, C.C. Lin, Y.S. Su, C.S. Hou and T.C. Ong, Taiwan Semiconductor Mfg. Co., *National Chiao Tung Univ., Taiwan R.O.C*

A new test chip is particularly designed to evaluate the large die (12mm x 12mm, for example) plastic assembly reliability, and is able to sensitively detect the die cracking due to the thermo-mechanical stress when undergoing packaging and reliability testing. Die cracking failures are found in the chips with A1-0.5Cu six-layer metal, and depend strongly upon the encapsulant molding compound material properties during temperature cycling and thermal shock testing. While using Cu damascene technology for top two-layer metal in the same packaging, the chips show no cracking failures during the same reliability testing.

10:20 a.m. - 10:50 a.m. Break

SESSION 10: DEVICE CHARACTERIZATION II

10:50 a.m. - 12:10 p.m.
Co-Chairs: **Alexander Rahm,** Infineon Technologies AG
Yoshiaki Hagiwara, Sony

10:50 10.1 **Evaluation of High-Performance SOI Complementary BiCMOS Devices by Using Test Structures**
*Y. Tamaki, T. Iwasaki, *K. Tsuji, *Y. Chida, T. Tomatsuri, E. Yoshida, J. Kumazawa and C. Kamada, Hitachi, Ltd., *Hitachi VLSI Engineering Co., Japan*

We have evaluated the performance advantage of complementary bipolar transistors fabricated on SOI substrate using a 0.35 μm complementary BiCMOS process by the use of new test structures. Fabricated transistors realized cut-off frequency of 10.5/6.0 GHz and C-E breakdown voltage of 19.5/17.8 V for NPN/PNP. The test structure measurement showed that the high-performance was due to the new isolation structure and transistor layout.

11:10 10.2 **Analysis of Hot Carrier Effects in Low Temperature Poly-Si TFTs Using Device Simulator**
*Y. Uraoka, T. Hatayama, T. Fuyuki, *T. Kawamura and *Y. Tsuchihashi, Nara Institute of Science and Technology, *Matsushita Electric Industrial Co. Ltd., Japan*

We have analyzed hot carrier effects in low temperature poly-Si TFTs. Drain avalanche hot electron effect is confirmed by the stress bias dependence and observation by emission microscope. A new degradation model is proposed for device simulation. Hot electrons generated by drain avalanche generate electron traps at grain boundary in the poly-Si. Reasonable agreement between the experimental results and simulations was successfully obtained.

11:30 10.3 **Channel Width and Length Dependent Flicker Noise Characterization for n-MOSFETs**
H. Aoki and M. Shimasue, Agilent Technologies Japan Ltd., Japan

Gate channel width and length dependent flicker noise analysis and modeling for sub-micron n-channel MOSFETs have been presented. It was found that the flicker noise increased with channel width on the contrary to the existing theory. Drain current noise density measurements were performed with two different CMOS processes for analysis using our automated 1/f noise measurement system. Since model parameters in the model are all geometry dependent, only one size device is needed for the extractions.

11:50 10.4 **New Length Scaling of Current Gain Factor and Characterization Method for Pocket Implanted MOSFFET's**
M. Minondo, G. Gouget and A. Juge, STMicroelectronics, France

In order to fit the observed current gain factor b against the channel length in our 0.18 μm and 0.12 μm processes using pocket implantations, a new function is proposed which allows a correct description again. The idea consists of splitting into two regions for which a mobility value is defined in each one. This pragmatic function has been implemented in the BSIM3V3.2 model and showed very good modeling in the whole channel length range for N- and P-MOSFET's.

12:10 p.m. Best Paper Announcement and Closing Remarks

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