ICMTS 2000

International Conference on Microelectronic Test Structures

Tutorial and Technical Program

March 13-16, 2000

DoubleTree Hotel at Fisherman's Wharf

Monterey, California USA

Dear Colleague,

On behalf of the committee, I am pleased to invite you to attend the 2000 International Conference on Microelectronic Test Structures (ICMTS 2000) in Monterey, California. The conference, sponsored by IEEE Electron Device Society, brings together designers and users of test structures from all over the world to discuss the most recent test structure developments and future directions. ICMTS 2000 is the 13th time ICMTS will be held as an international conference. ICMTS began in 1986 as a workshop, becoming an international conference in 1988. The conference has been able to maintain its workshop-like friendliness through ample social activities. Coffee breaks, hosted lunches, and a banquet ensure that participants get the chance to interact frequently, meeting others in their field and sharing common experiences.

This year's conference consists of 47 papers in 10 sessions including a poster session with 11 papers. The oral sessions include CD metrology, device characterization, yield and interconnects, matching, reliability, process characterization, and RF characterization. Oral presentations are fifteen minutes long with five minutes for questions. Authors in the poster session will present a brief oral summary of their work in addition to answering questions at their posters.

As in the past, there will be an equipment exhibit. In addition to displaying their most recent test structure related wares, each vendor will have the opportunity to give a short presentation highlighting their latest products. A reception is planned to follow the equipment exhibitor's presentation.

The short course tutorial for ICMTS will be held on Monday, March 13, preceding the conference. Eight industry, government, and university experts will present tutorials on topics including silicon on insulator (SOI) test structures and characterization, VLSI yield optimization, RF measurements and modeling, electrostatic discharge (ESD), matching for analog CMOS applications, and test structures for critical dimension, overlay metrology, parameter extraction, and process characterization. These presentations are intended to give the audience an introduction to the essential concepts as well as exposure to the current state-of-the-art.

The Conference will be held at the DoubleTree Hotel adjacent to Fisherman's Wharf in the center of Monterey. The conference banquet will be held Wednesday, March 15 at Chateau Julian, an award winning winery in Monterey County a short bus ride from the hotel. Both the DoubleTree Hotel and the charming town of Monterey will provide an excellent back drop for a very rewarding technical conference.

Sincerely,

Lawrence Bair

General Chairman

GENERAL INFORMATION

The 2000 IEEE ICMTS will be held at the DoubleTree Hotel at Fisherman's Wharf in Monterey, California. The Conference headquarters hotel will provide guest accommodations as well as meeting facilities for all attendees. The technical program, consisting of ten sessions of contributed papers and a poster session, will be held March 14-16. A tutorial short course will be offered on Monday, March 13.

CONFERENCE REGISTRATION

Payment of the TECHNICAL SESSION registration fee entitles the registrant to one copy of the Technical Digest, entrance to all technical sessions and the exhibit hall, and all social events.

Payment of the SHORT COURSE registration fee entitles the registrant to one copy of the Short Course Workbook and luncheon. Short Course participants must register in advance.

For **Advance Registration,** complete the Registration Form and mail the form with payment to the Conference Headquarters. Advance registration forms must be received by the Conference Headquarters NO LATER THAN February 14, 2000. After February 14, you must register at the Conference and pay the late registration fee. Short Course participants must register in advance. On-site short course registration will only be accepted based on space availability.

If you fax your registration form, you must included credit card information, and a 5% processing fees for all credit card transactions

Mail or fax your conference registration form and remittance to: 2000 ICMTS Conference

101 Lakeforest Blvd., Suite 400-B

Gaithersburg, MD 20877

1-301-527-0900 x104 * Fax: 1-301-527-0994

Email: wendyw@widerkehr.com

CANCELLATIONS: Refund requests must be received, in writing, by February 28 in order to receive a full refund, less a $25.00 processing fee. Due to financial commitments, refund requests received after February 28 cannot be guaranteed.

IEEE Members: In order to qualify for the member fees, you must list your IEEE membership number.

ADVANCE REGULAR

	(by February 14)	(after February 14 and on-site)
Technical Session		
IEEE Member	$375	$435
Non-Member	$425	$485
Student	$260	$310
Short Course (ADVANCE Registration Only)		
IEEE Member	$250	$250
Non-Member	$250	$250
Student	$125	$125

HOTEL RESERVATIONS

A block of rooms has been reserved at the DoubleTree Hotel at Fisherman's Wharf, Monterey, California. To make a reservation, complete the Hotel Reservation form and return it, along with one night's lodging to:

DoubleTree Hotel at Fisherman's Wharf

2 Portola Plaza

Monterey, CA 93940

Reservations: 800-222-TREE (8733)

Tele: 831-649-4511 Fax: 831-649-3109

Rates: $129 + tax single/double

HOTEL RESERVATIONS MUST BE RECEIVED BY FRIDAY, FEBRUARY 11 to guarantee the conference rate.

All changes and cancellations should be made directly with the hotel. It is the responsibility of each participant to make changes or cancellations no later than 48 hours prior to scheduled arrival. Room reservations will be held until 6:00 p.m. unless a later time is guaranteed by a credit card. Rooms are generally not available for check-in until 3:00 p.m. on the day of arrival.

Parking is available. Valet is $12.00 per day and self-parking is $10.00 per day. There is public parking available at a nominal charge located one block from the hotel.

TECHNICAL SESSION INFORMATION

The Technical Sessions will be held in DeAnza Ballroom 1-2.

POSTER SESSIONS: Poster Session authors will present a five minute talk describing their poster on Tuesday at 3:30 p.m. The poster descriptions will be followed by the poster presentations in the DeAnza Ballroom 3. The authors will be available at their displays for questions and discussion.

Posters will be displayed from Tuesday at 1:00 p.m. until Thursday at 12:00 noon.

EQUIPMENT EXHIBITS: ICMTS vendor exhibits will be displayed in the DeAnza Ballroom 3 on Tuesday, March 14 from 1:00 p.m. and will remain on display until 12:00 noon on Thursday, March 16.

If you would like to exhibit at the conference, please contact Jim Reedholm at Reedholm Instruments, 512-869-1935; jimr@reedholm.com. Past exhibitors have included: Sandia National Laboratories, Cascade Microtech, Hewlett Packard, QualiTau, Lucas/Signatone Corp. and Reedholm Instruments.

TECHNICAL DIGEST

Extra copies of the Technical Digest can be purchased by conference through Advance Registration at a cost of $75.00. After the conference, digests will be available through the IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08855.

SOCIAL EVENTS

A Continental Breakfast (8:00 a.m. - 9:00 a.m.) will be available each day of the meeting. The conference will host a Tuesday Luncheon and an Awards Luncheon on Wednesday.

The Conference Banquet will be held on Wednesday,

March 15 at the Chateau Julien Vineyard. Round trip bus transportation will be provided. Buses will depart from the front of the hotel starting at 6:00 p.m. There will be a wine tasting when you arrive at the vineyard. One ticket is included with the registration fee, additional guest tickets may be purchased for $75.00.

An opening reception will be held on Monday evening from 7:00 p.m. - 9:00 p.m. and a reception will be held in the Exhibit Hall during the poster displays on Tuesday evening from 4:30 p.m. --7:00 p.m.

TRANSPORTATION

By Air: Monterey Peninsula Airport is served by many airlines including American Eagle, Skywest/Delta, Northwest, United and US Air. There are nearly 100 arrivals and departures daily to and from San Francisco and Los Angeles with connections to all domestic and foreign locations. The distance from the airport to the DoubleTree is approximately four miles.

By Car: The drive from San Jose is approximately 60 miles; San Francisco is approximately 120 miles.

Airport Transportation: Taxi service is recommended. The cost is approximately $10.00.

Rental Cars: Several rental car agencies are located at the Monterey Airport: Avis, Budget, Dollar, Hertz, National, and Thrifty.

MESSAGES

A message board will set up in the registration area for conference attendees. Call the hotel at 831-649-4511 and ask for the ICMTS Registration Area. The guest fax number is 831-372-0620.

WEATHER

Monterey enjoys a unique weather pattern, with coastal temperatures averaging 57 degrees year-round. Average temperatures in March range from 45°F - 62°F. It is advisable to bring a jacket, sweater or coat.

MONTEREY AREA ATTRACTIONS

Monterey Bay Aquarium: This fascinating, internationally acclaimed aquarium focuses on educating visitors about the mysteries and wonders of the Monterey Bay.

Big Sur: A 90-mile stretch of coastline that begins in Monterey County a few miles south of Carmel and ends in San Luis Obispo County at San Simeon (Hearst Castle).

Cannery Row: An historic area of the city of Monterey, located on the Bay between the Coast Guard wharf and the pacific Ocean.

Carmel-by-the-Sea: A village in a forest setting located above a breathtaking white-sand beach 5 miles south of Monterey.

Carmel Valley: Twelve miles due east of Carmel-by-the-Sea.

Fisherman's Wharf and Wharf II: Located on Monterey Bay, in the historic heart of Monterey, off of Del Monte Avenue.

Pebble Beach: On the southern tip of the Monterey Peninsula, due west of Monterey and due north of Carmel-by-the-Sea.

Hearst Castle: A California State Historical Monument containing 165 beautifully furnished rooms, a huge collection of art and antiques, impressive swimming pools, gardens and terraces. Located 90 miles south of Monterey.

TOUR PROGRAM

Thursday, March 16

1:30 p.m. - 5:30 p.m.

$35 per person

A tour program has been developed especially for ICMTS participants - for first-time visitors to the Monterey Peninsula, as well as "old-timers". Our custom-designed tour will take you from Point Lobos to Big Sur. You'll travel along a magnificent segment of the California coast line that stretches from the crest of the Santa Lucia mountains to the mesmerizing Pacific Ocean. Exceptionally scenic stops and captivating commentary complements this journey along "one of the most beautiful highways in the world." At Point Lobos, you'll have the opportunity for a guided nature walk and, through a high-powered spotting scope, a chance to observe sea otters, sea lions and harbor seals in their natural habitats. You'll also stop at Pfeiffer State Park for a short walk amongst the majestic redwoods, which are hundreds of years old. You'll want to bring your camera and wear comfortable shoes for this tour.

The tour is limited to 40 people, so sign up early to avoid disappointment. To register for the tour, please use the conference registration form.

TUTORIAL SHORT COURSE:

Monday, March 13, 2000

"An Introduction to the Design, Measurement, and Analysis of Microelectronic Test Structures"

The ICMTS Tutorial Short Course, which immediately precedes the conference, offers a blend of tutorial and advanced topics. Test structure creation and characterization basics are included. In addition, the ICMTS 2000 also includes tutorials on test structures for SOI characterization as well as yield modeling. The Tutorial is intended to provide the non-expert with the fundamentals associated with microelectronic test structures, while providing the more experienced user with information on various advanced topics. The course strives to provide design, test, and analysis guidelines so that superior test-structure practice will be followed, leading to improved process control, higher yielding product, and rapid product introduction. The course instructors have many years of experience in the field of test structures. The format will be interactive with emphasis on the practical use of microelectronic test structures.

Tutorial Schedule

Monday, 13th March, 2000

8:00am		REGISTRATION
9:00am	1.	Welcome Ellen G. Piccioli, Compaq Computer Corporation
9:05am	2.	Transferring Process Characterization to Production Control Bill Verzi, Agilent Technologies
9:50am	3.	Electrical Test Structures for Critical Dimension and Overlay Metrology

		Richard A. Allen, NIST
10:35am		Break
11:05am	4.	Test Structures, Extraction, and Statistical Techniques for SPICE Models Colin McAndrew, AT&T Bell Laboratories
11:50am	5.	Matching of Active and Passive Devices in Analog CMOS Applications Roland Thewes, Infineon Technologies
12:35pm		Hosted Lunch
1:50pm	6.	ESD Test Structures Robert A. Ashton, Lucent Technologies
2:35pm	7.	RF measurements and modeling, with special emphasis on test structures Franz Sischka, Agilent Technologies
3:20pm		Break
3:50pm	8.	An Introduction to Silicon on Insulator (SOI) Test Structures and Measurements Dr. Jeffrey W. Sleight, IBM
4:35pm	9.	Test Structures for VLSIC Yield Ramp Maximization Andrzej J. Strojwas, PDF Solutions and Carnegie Mellon
5:20pm	10.	Tutorial Conclusion Ellen G. Piccioli, Compaq Computer Corporation

Contents

- Test structures and measurements for SPICE modeling
  - DC, AC and noise, capacitance, calibration
  - geometry selection and experimental designs
- Basics of parameter extraction
- Statistical SPICE simulation, modeling and characterization
  - problems with common statistical modeling procedures
  - fundamental physical modeling basis
  - statistical extraction techniques, sensitivity analysis and propagation of variance
  - manufacturing (SGPC or ETEST) structures and measurements for modeling

5. Matching of Active and Passive Devices in Analog CMOS Applications - Roland Thewes, Infineon Technologies

- Introduction
- General approach
- Matching of MOS Transistors
  - Characterization
  - Experimental Results
  - Modeling
- Matching of Resistors
  - Characterization
  - Experimental Results
  - Modeling
  - Matching of Capacitors
    - Characterization techniques
- Long Distance Mismatch
- Conclusion

6. ESD Test Structures - Robert A. Ashton, Lucent Technologies

- Characterizing CMOS Technologies for ESD Robustness
  - Introduction to ElectroStatic Discharge (ESD)
  - ESD testing of Integrated Circuits (HBM,MM,CDM)
- Basics of ESD Protection Circuitry
  - Circuit Elements to be protected
  - Circuit Elements used for protection
  - Understanding Circuit Elements outside of Normal Operation
  - Transmission Line Pulse Measurement (TLP)
  - Test Structures for ESD Characterization
  - SEMATECH Structures for ESD Robustness

7. RF measurements and modeling, with special emphasis on test structures - Franz Sischka, Agilent Technologies

- Introduction
- Basics of device modeling from DC to RF
- RF measurements and modeling
- Special aspects of VNA calibration
- De-embedding and required test structures
- Harmonic Balance Modeling
- Summary

8. An Introduction to Silicon on Insulator (SOI) Test Structures and Measurements - Dr. Jeffrey W. Sleight, IBM

- SOI Technology Overview
- SOI Specific Test Structures and Measurements
  - Transient FET IV Measurements
  - Body Tie Types and Measurements
  - `History' Effect Measurements
  - Self-heating Measurements and Structures
  - Pass Gate Upset Measurements
  - SRAM and Array Tests
  - Dynamic Logic Tests and Issues
  - SOI Electrical Material Tests
- Summary

9. Test Structures for VLSIC Yield Ramp Maximization - Andrzej J. Strojwas, PDF Solutions and Carnegie Mellon

- Introduction
- Classification of Yield Loss Mechanisms
- Yield Loss Characterization Methods
    1. In-line Measurements
    2. Characterization Vehicles (CV's)
        - Short Flow, Half Flow and Full Flow Experiments
        - E-test Structures Measurements
        - Product Test Analysis
- Test Structures for Yield Loss Diagnosis
    - Random Defect Limited Yield Characterization Vehicles
    - Systematic Yield Loss Characterization Vehicles
    - Parametric Yield Loss Characterization Vehicles
- Software Tools for Yield Analysis
- Examples of Characterization Vehicles Applications for Yield
- Analysis/Improvement
- Future Trends

10. Tutorial Conclusion - Ellen G. Piccioli, Compaq Computer Corporation

Tutorial Short Course Instructors

Bill Verzi - Transferring Process Characterization to Production Control

Bill Verzi received a degree in Electronics Technology from West Valley College in 1981, supplemented with additional work in Physics, and Computer Science at San Jose State University. He joined the Intel Corporation in 1978 where he was involved in the production and quality assurance of memories. From 1979, he participated in the research and development of NMOS and CMOS processes used to make static/logic devices such as the first 8086 microprocessor. His work included transistor characterization and process integration through electrical test, designing test structures, test equipment, and measurement methods to evaluate the semiconductor process. He joined Hewlett Packard in 1988, supporting process evaluation through electrical test. He accepted an assignment to SEMATECH in 1990 to design and support electrical test methods for process characterization with a focus in plasma damage evaluation. He returned to Hewlett Packard in Austin, Texas in 1992, where he continues to support process evaluation by electrical test methods. He has been an IEEE member since 1986.

Richard A. Allen - Electrical Test Structures for Critical Dimension and Overlay Metrology

Richard Allen received the B.S. degree and the M.S. degree, both in Physics, from Rensselaer Polytechnic Institute, Troy, New York. He has worked at the Jet Propulsion Laboratory in Pasadena, California where he developed test structures for monitoring space radiation effects in the VLSI Technology Group and at College Park Software in Altadena, California, where he worked on the development of LISP-based expert systems tools. Since June 1990 he has been with Integrated Circuits Technology Group of the National Institute of Standards and Technology, Gaithersburg, Maryland. His present interests include developing test structures for nanometer-level linewidth and overlay metrology. Mr. Allen is a member of the American Physical Society and the Institute for Electrical and Electronics Engineers.

Colin McAndrew - Test Structures, Extraction, and Statistical Techniques for SPICE Models

Colin McAndrew received the Ph.D. and M.A.Sc. degrees in Systems Design Engineering from the University of Waterloo, Waterloo, Ontario, Canada, in 1984 and 1982 respectively, and the B.E. degree in Electrical Engineering from Monash University, Melbourne, Victoria, Australia, in 1978. Since 1995 he has been with Motorola, Tempe AZ, and is at present the Director of Enabling Technology in the Analog-Mixed Signal Technology Center. From 1987 to 1995 he was at AT&T Bell Laboratories, Allentown PA. His work is primarily on compact and statistical modeling and characterization for circuit simulation.

Roland Thewes - Matching of Active and Passive Devices in Analog CMOS Applications

Roland Thewes was born in Marl, Germany, in 1962. He received the Dipl.-Ing. degree and the Dr.-Ing. degree in Electrical Engineering from the University of Dortmund, Dortmund, Germany, in 1990 and 1995, respectively. From 1990-1995 he worked in a cooperative program between the Siemens Research Laboratories in Munich and the University of Dortmund in the field of hot-carrier degradation in analog CMOS circuits. Since 1994 he has been with the Research Laboratories of Siemens AG and Infineon Technologies, where he has been active in the design of non-volatile memories and in the field of reliability and yield of analog CMOS circuits. He has authored or co-authored some 40 publications. At present, he is managing projects in the fields of design for manufacturability, reliability, analog device performance, and analog circuit design. In 1998 he received a best paper award of the European Symposium on Reliability of Electron

Devices, Failure Physics and Analysis (ESREF) for a publication on the physical effects of hot-carrier degradation. He served as a member of the technical program committee of the International Electron Device Meeting (IEDM) and is a member of the technical program committees of the International Reliability Physics Symposium (IRPS) and of the European Solid State Device Research Conference (ESSDERC). Dr. Thewes is a member of the IEEE, of the German Association of Electrical Engineers (VDE), and of the German Information Technology Society (ITG).

Robert Ashton - ESD Test Structures

Robert Ashton received his B.S. and Ph.D. degrees in Physics from the University of Rhode Island in 1971 and 1977. After doing post doctoral positions in low temperature physics at Rutgers University and Ohio State University he joined AT&T Bell Laboratories in 1980. At AT&T Bell Labs and now at Bell Labs, Lucent Technologies, which spun off from AT&T in 1996, he has been a Member of Technical Staff in the VLSI Technology Laboratory. He has been involved in technology integration for core CMOS technologies, test structure design for technology development, and the technology issues of Electro-Static Discharge (ESD). He is a member of the IEEE Electron Device Society, the ESD Association and the SEMATECH ESD Working Group. He has been a member of the ICMTS Technical Committee since 1990 and served as Technical Chairman in 1994 and as General Chairman in 1997.

Franz Sischka - RF measurements and modeling, with special emphasis on test structures

Franz Sischka studied communication engineering at the University of Stuttgart, Germany, where he also received his M.S. (Diplom-Ingenieur) and the Ph.D. degrees in 1979 and 1984. After joining Hewlett-Packard in Germany, he worked for 5 years in R&D in the fiber optics group at HP Boeblingen and was co-developer of HP's first optical time domain reflectometer (OTDR). Since 1989, he is consultant for HP's (and now Agilent Technologies) device modeling software IC-CAP and author of the IC-CAP modeling reference book. His work is specially focusing on high frequency device modeling and model parameter extraction strategies for active and passive components on wafer.

Dr. Jeffrey W. Sleight - An Introduction to Silicon on Insulator (SOI) Test Structures and Measurements

Dr. Sleight received his Ph.D. degree in applied physics from Yale University in 1995. His Ph.D. thesis dealt with the physics and fabrication of sub-micron semiconductor structures that exhibit quantum size and charging effects. From 1995 to 1997, he was with the Device and Interconnect Physics group at Digital Semiconductor, Hudson, MA, where he worked primarily in the area of silicon on insulator (SOI) device development, modeling, and test structure design. During his time at Digital, Dr. Sleight was a member of the team that demonstrated one of the first CMOS VLSI SOI chips, an implementation of the StrongARM-110 Microprocessor. In 1998, he joined the Semiconductor Research and Development Center at IBM, where he is currently involved with advanced SOI technology development. Dr. Sleight has authored and co-authored over 30 papers in the areas of semiconductor device physics, fabrication, and modeling, and holds two US Patents.

Andrzej J. Strojwas - Test Structures for VLSIC Yield Ramp Maximization

Andrzej J. Strojwas is Professor of Electrical and Computer Engineering at Carnegie Mellon University and co-Director of Pennsylvania SEMATECH Center of Excellence. Since 1997 has served as Chief Technologist at PDF Solutions, Inc. He received the Ph.D. degree in electrical engineering from Carnegie Mellon University in Pittsburgh, PA, in 1982. He has held positions at Harris Semiconductor Co., AT&T Bell Laboratories , Texas Instruments, NEC, HITACHI, SEMATECH, KLA-Tencor and PDF Solutions, Inc. He serves as consultant to a number of industrial laboratories in the area of statistically based CAD/CIM of VLSI circuit. His research interests include modeling of IC equipment, fabrication processes and semiconductor devices, computer-aided design and verification of VLSI circuits, and control and diagnosis of the IC fabrication processes. In 1985 he received an award for the best paper published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, and the Best Paper Award at the 22nd IEEE-ACM Design Automation Conference. He is also a recipient of the SRC Inventor Recognition Award. He received the 1991 Best Paper Award from IEEE Transactions on Semiconductor Manufacturing. He was Editor of the IEEE Transactions on CAD of ICAS from 1987 to 1989. He served as Technical Program Chairman of the 1988 ICCAD and Conference Chairman of the 1989 ICCAD. Between 1991 and 1994 he was a Chairman of the IEEE Computer-Aided Network Design (CANDE) Committee and a member of the IEEE Steering Committee for Design and Manufacturing Engineering. In 1990 he was elected IEEE Fellow.

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MONDAY, MARCH 13

8:00 a.m. - 10:00 a.m. Short Course Registration ONLY

9:00 a.m. - 5:30 p.m. Tutorial Short Course

4:00 p.m. - 8:00 p.m. Conference Registration

7:00 p.m. - 9:00 p.m. Registration Reception

TUESDAY, MARCH 14

8:00 a.m. - 9:00 a.m. Continental Breakfast

8:00 a.m. -5:00 p.m. Registration

SESSION 1: CD METROLOGY

9:00 a.m. - 10:40 a.m.

Co-Chairs: Loren Linholm, NIST

Dieter Schroder, Arizona State University.

9:00 Characterization of Electrical Linewidth

1.1 Test Structures Patterned in (100) Silicon-on-Insulator for Use as CD Standards - *M. Cresswell, R. Allen, R. Ghoshtagore, N. Guillaume*, P. Shea+, S. Everist+, and L. Linholm, National Institute of Standards and Technology, Gaithersburg, MD, *George Washington University, +Sandia National Laboratories*

This paper describes the fabrication and test of electrical linewidth test structures patterned in (100) Silicon-on-Insulator (SOI) substrates. Their unique attributes are features having sidewall slopes of exactly 54.737°. The long-term goal is to develop a technique of ascertaining the physical linewidths of the structures' bridge resistors. The plan is to use electrical CD (Critical Dimension) metrology as a secondary reference means in the linewidth-certification path to provide traceability to fundamental physical constants. Their end-use is the calibration of SEM, AFM, optical, and other metrology systems used in wafer-fabrication process control. This is believed to the first report of electrical CD measurements made on such structures.

9:20 A New Test Structure to Measure Metal

1.2 Linewidths Using Minimal Real Estate - *M.*

Fallon and C. McGregor, National Semiconductor (UK), Ltd., Greenock, Scotland

A new approach is adopted to measure metal linewidths. Traditionally low resistive materials require long tracks and/or high-resolution voltmeters to measure the critical dimension. In this approach the test is forced into a non-Ohmic regime and so an appreciable voltage can be measured. The non-linearity is compensated by a balanced design layout.

9:40 Characterization of Mask Alignment Offsets

1.3 Using Null Wire Segment Holograms - A

Progressive Offset Technique - *S. AbuGhazaleh, P. Christie and A. Walton*, University of Delaware,*

*Newark, DE, *University of Edinburgh,*

Edinburgh, United Kingdom

This paper presents data characterizing alignment offsets in a commercial 1 μm fabrication process using a combination of null wire segment holograms and a progressive offset technique. The test structure is essentially a binary computer generated hologram constructed from wire segments and is designed to project a null image when the masks for the process are in perfect alignment. Characterization using the technique indicates a mask misalignment of between 0.1 and 0.3 μm, and this is confirmed using atomic force microscopy.

10:00 A Novel Method for Fabricating CD

1.4 Reference Materials with 100 nm Linewidths - *R. Allen, L. Linholm, M. Cresswell and C. Ellenwood, National Institute of Standards and Technology, Gaithersburg, MD*

A technique has been developed to fabricate 100-nm CD reference features with i-line lithography by utilizing unique characteristics of single-crystal silicon-on-insulator films. In this paper we will describe the technique, show results of the process, and present electrical critical dimension measurements that support the use of this technique for producing current and future generation of reference materials for the semiconductor industry.

10:20 High-Spatial-Frequency MOS Transistor

1.5 Gate Length Variations in SRAM Circuits - *X. Ouyang, T. Deeter*, C. Berglund, R. Pease and M. McCord, Stanford University, Stanford, CA, *Intel Corporation, Hillsboro, OR*

SRAM circuits were used as high-throughput, high-spatial-frequency electrical test structures to study short range spatial variations of MOS transistor effective gate length. Layout dependent errors were found to be dominant, which can be explained by proximity effects and overlay errors caused by stepper lens aberration. Pattern dependent coma effect may have caused transistor mismatch within the SRAM cell. The role of reticle errors is discussed.

10:40 a.m. - 11:10 a.m. Break

SESSION 2: DEVICE CHARACTERIZATION

11:10 a.m. - 12:10 p.m.

Co-Chairs: Robert Ashton, Lucent Technologies/Bell

Labs.

Kunihiro Asada, University of Tokyo

11:10 Fabrication of Twin Transistors Using

2.1 Sidewall Masks for Evaluating Threshold Voltage Fluctuation - *M. Okuno, T. Aoyama, S. Nakamura, R. Sugino and H. Arimoto, Fujitsu Laboratories Limited, Atsugi, Kanagawa, Japan*

We propose twin MOSFETs to evaluate a threshold voltage (Vt) fluctuation. The 95 nm twin gates were made using SiN sidewall masks which gave exactly the same gate lengths. From the difference in Vt between twin transistors, we can evaluate the Vt fluctuation due not to a global variations across a wafer such as a variation of gate oxide thickness but to local variations such as a variation of carrier concentration. The standard deviation of the gate length difference between twin transistors was found to be 1.2 nm, that could not be realized with an electron beam lithography.

11:30 Characterization of Sub-micron MOS

2.2 Transistors, Modified Using a Focused Ion Beam System - *D.W. Travis, C.M. Reeves and A.J. Walton, University of Edinburgh, Edinburgh, Scotland*

A focused ion beam system has been used to demonstrate the modification of the effective electrical width of a MOS transistor. The internal structure of the transistor test structure is modified using two distinct approaches, where the cut axis is either parallel or orthogonal to the source-drain axis. This paper demonstrates the feasibility of modifying transistor characteristics which can be used to evaluate processes and to modify circuit designs.

11:50 Extraction of Channel Thermal Noise of

2.3 MOSFETs - *C.-H. Chen, M. Deen, M. Matloubian* and Y. Cheng*, McMaster University, Hamilton, ON, Canada, *Conexant Systems, Inc., Newport Beach, CA*

An extraction method to obtain the channel thermal noise (id2) of MOSFETs directly from the d.c., a.c. and RF noise measurements is presented. It shows that the induced gate noise and its correlation with the channel thermal noise are negligible for frequencies up to 18GHz and the equations 8kTgm/3, 8kTgdo/3 and 8kT(gm+gds)/3 for calculation id2 are not valid for sub-micron MOSFETs biased in the saturation region.

12:10 p.m. - 1:40 p.m. Luncheon (Bonzai Ballroom)

SESSION 3: YIELD & INTERCONNECTS

1:40 p.m. - 3:00 p.m.

Co-Chairs: Akella Satya, KLA-Tencor

Larg Weiland, PDF Solutions

1:40 Addressable Failure Site Test Structures

3.1 (AFS-TS) for Process Development and Optimization - *K. Doong, S. Hsieh, S.-C. Lin, M.-H. Lee, B. Shen, Y.-H. Ho, J.-Y. Cheng, Y.-H. Yang, K. Miyamoto** and C. Hsu*, Worldwide Semiconductor Manufacturing Corporation, Sinchu, Taiwan, *National Tsing-Hua Univ., Rep. of China, **Toshiba Corp.*

Two types of addressable failure site test structures are developed. In-house program is coded to extract the electrical information and simulate the failure mode. A complete set of test structure modules for 0.25 um logic backend of line process is implemented in a test chip of 22x6.6mm2. By using the novel test structure, the yield analysis and defect tracking of BEOL process development as well as low-k FSG process optimization are demonstrated.

2:00 Fast Extraction of Killer Defect Density and Size

3.2 Distribution Using a Single layer Short Flow NEST Structure - *C. Hess, D. Stashower, B.E. Stine, G. Verma, and L.H. Weiland, PDF Solutions, San Jose,CA*

Defect inspection is required for process control and to enhance chip yield. Electrical measurements at test structures are commonly used to detect faults. To improve accuracy of electrically based measurements of defect densities and defect size distributions, we present a novel NEST test structure. There, many nested serpentine lines will be placed within a single layer only. This mask will be used as a short loop to guarantee a short turn-around time for fast process data extraction. Data analysis procedures will provide densities and size distributions of killer defects that will have an impact on product chip yield.

2:20 Use of Test Structures for Cu Interconnect

3.3 Process Development and Yield Enhancement

A. Skumanich, M.-P. Cai and J. Educato, Applied Materials, Santa Clara, CA

A critical aspect of CU interconnect process development is identifying and eliminating yield impacting defects. A methodology is described where wafers with specialized test structures are inspected with wafer metrology tools in order to help drive process development for Cu BEOL fabrication. A full-flow Cu damascene interconnect process is examined from oxide deposition to final electrical test to establish inspection strategies for defect reduction. For various test structures, the progression of defects is tracked to the final e-test point. This tracking establishes the key defect types, facilitates defect sourcing, and identifies the optimal test structure configurations for defect reduction. The results based on the test structures and the details of the test structures will be presented for advanced Cu interconnect development.

2:40 A Microelectronic Test Structure for Signal

3.4 Integrity Characterization in Deep Submicron

Technology - *F. Caignet, S. Delmas-Bendhia and E. Sicard, INSA Toulouse, Toulouse Cedex, France*

The benefits expected by the decreases of feature sizes in high-speed electronics circuits are limited by the increased parasitic effects of interconnect. This paper details the application of an on-chip time domain technique to the characterization of propagation delay, crosstalk and crosstalk-induced delay, along interconnects in deep submicron technology. The measurement system is detailed, together with the signal integrity patterns and their implementation in 0.18 CMOS technology. Measurement obtained with this technique are presented and compared

with simulations.

3:00 p.m. - 3:30 p.m. Break

SESSION 4: POSTER SESSION

3:30 p.m. - 5:00 p.m.

Co-Chairs: Anthony Walton, University of Edinburgh

Takashi Ohzone, Toyama Prefectural University

4.1 A Study on Hot-Carrier-Induced Photoemmission in n-MOSFETs Under Dynamic Operation - *T. Ohzone, M. Yuzaki, T. Matsuda and E. Kameda*, Toyama Prefectural University, Toyama, Japan, *Toyama National College of Technology, Toyama, Japan*

Hot-electron-induced TPC (Total Photon Counts) measured by a photoemission microscope are proportional to the average substrate current IB in n-MOSFETS under dynamic operation as in case of DC operation. 2-D distribution of IB along the channel width direction can be estimated by 2-D TPC profile analysis. This method is useful to analyze lifetime estimation of CMOS circuits under dynamic operation, especially to detect weak lifetime locations in a MOSFET with a long channel width.

4.2 Extraction of Effective LDMOSFET Channel Length and its Applications to the Modeling - *K. Tsuji, K. Terada, M. Minami and K. Tanaka*, Hiroshima City University, Hiroshima, Japan, *NEC Corporation, Kawasaki, Japan*

The effective channel length of LDMOSFET is accurately extracted and is applied to develop its circuit simulation model. This model is consisted of a simple MOSFET, gate-voltage dependent resistor and three resistors. It is confirmed that the errors between the measured electrical Characteristics and the calculated one are less than 5 percent.

4.3 Gate-Length Dependence of Bulk Generation Lifetime and Surface Generation Velocity Measurement in High-Resistivity Silicon Using Gated Diodes - *G.-F. Dalla Betta, G. Verzellesi, M. Boscardin, G. Pignatel*, L. Bosisio**, G. Soncini, ITC-IRST, Pante di Povo (TN), Italy, *Universita di Trento, Trento, Italy, **Universita di Trieste and INFN, Trieste, Italy*

We show that the accuracy of the gated diode method for measuring bulk generation lifetime and surface generation velocity in high resistivity silicon depends critically on the gate length of the test device, as a result of nonidealities affecting the gated diode operation. Minimization of the surface generation velocity measurement error requires the gate length to be suitably decreased, while long gate length structures are needed for accurate bulk generation lifetime extraction.

4.4 Thermo-Mechanical Structures for the Optimisation of Silicon Micromachined Gas Sensors - *A. Götz, I. Gràcia, C. Cané, M. Lozano and E. Lora-Tamayo, Centrao Nacional de Microelectrónica (IMB-CSIC), Bellaterra, Spain*

In this paper, a set of thermomechanical structures that have been used to optimize the sensor design is presented. These devices have been used to determine the best options in terms of dielectric membrane material, thickness, minimum membrane dimensions, heater layout and related processing steps. Mechanical, electrical and thermal measurements are presented on processed samples and results of yield and reliability will be discussed.

4.5 Thermal Channel Noise of Quarter and Sub-Quarter Micron NMOS FETs - *G. Knoblinger, P. Klein and U. Baumann*, Infineon Technologies AG, Munich, Germany *IMMS Ilmenau, Germany*

We present a simple and efficient method for the extraction of thermal channel noise of MOSFET's in quarter and sub-quarter micron technologies from NF50 (noise figure at 50 Ohm source resistance) measurements. For shorter channel lengths the experimental results shows a continuously rising deviation from the classical long channel theory [1]. For a 0.18 µm technology a v=6 instead of 2/3 in saturation was extracted (increase of factor 9 compared to the long channel theory.

4.6 A New Mobility Model for Circuit Simulation in Pocket Implanted MOSFET's - *P. Klein and F. Schuler, Infineon Technologies AG, Munich, Germany*

A new analytical, physical-based effective mobility model valid in all regimes of device operation from weak to strong inversion together with an extraction method and corresponding test structures is introduced. The model accounts for the influence of the electrical field as well as for the lateral non-uniform doping profile in pocket implanted MOSFET's. Measurements show that the high local channel doping in the pocket implanted regions makes the mobility degradation due to Coulomb scattering with ionized dopants no longer negligible especially for low gate bias voltage thus for low voltage circuit design.

4.7 A New Extraction Method of Retention Time from the Leakage Current in 0.23µm DRAM Memory Cell - *C.-M. Nam, S.-K. Park, S.-H. Lee, J.-B. Suh and G.-H. Yoon, Hyundai MicroElectronics, Cheongju-si, Korea*

The retention time distributions of DRAM memory cell with 0.23 µm design rule and STI (Shallow Trench Isolation) have been investigated for the several process split that are designed to increase the retention time. In this paper, a new extraction method of retention time in memory cell will be proposed from the cell leakage current behavior at the general test pattern of memory cell array structure. And, the 50% bit failure time of memory cell is calculated by proposed method and compared with measured retention time, firstly. The calculated retention time is very well matched with measured result in several process conditions of memory cell. So, this method can be used for extract the retention time of high-density DRAM memory (below 0.23 µm) from the cell leakage current.

4.8 Test Structure for Universal Estimation of MOSFET Substrate Effects at Gigahertz Frequencies - *T. Kolding, Aalborg University, Aalborg, Denmark*

This paper presents a unit test structure for investigation of bulk effects critical to scalable MOSFET models at gigahertz frequencies. The test structure is useful for evaluating the RF performance of CMOS active devices of a particular process. The gate-modified test structure is compatible with standard CMOS technology and reveals any

dependence of diffusion bias on substrate effects. Several MOSFET layout guidelines are suggested for improved consistency between simulation and actual performance. Measurement examples are provided to illustrate bulk effects as well as the applicability of the method in a modeling situation.

4.9 On-Chip Voltage Noise Monitor for Measuring Voltage Bounce in Power Supply Lines Using a Digital Tester - *H. Aoki, M. Ikeda and K. Asada, University of Tokyo, Tokyo, Japan*

In this paper, we describe a new on-chip voltage monitor circuit for measuring VLSI power supply noise. This circuit uses a sampling method and makes it possible to measure a voltage bounce noise by a digital tester and variable voltage sources. We fabricated this circuit and measured noise waves. It can potentially measure noise waves within 30 mV voltage resolution and 1.0ns time resolution.

4.10 An Electrical Technique for Determining MOSFET Gate Length Reduction Due to Process Micro-Loading Effects in Advanced CMOS Technology - *C. Liu, J. Ma and J. Choi, Integrated Device Technology, Inc., Santa Clara, CA*

A test structure was designed that enables an electrical determination of gate length reduction due to microloading effects in poly. A transistor with parallel dummy poly's and transistors with isolated poly's were compared. We propose that DIBL effects be used to extract gate length reduction without being affected by any parasitic resistance in source/drain regions. The results agreed well with cross-section SEM analysis, and were confirmed by the measured and simulated speeds of NAND/NOR ring oscillator circuits.

4.11 Rapid Evaluation of the Root Causes of BJT Mismatch - *P. Drennan, Motorola, Inc., Tempe, AZ*

This paper presents a new technique for the quick and easy evaluation of the process and geometry parameter contributions to BJT mismatch. The pinch base sheet resistance variation, the geometric variation, and the ideal component of the emitter-base current variation can be uniquely determined from the Ic, Ib and Beta mismatch variances in the ideal region. The non-ideal component of the base current can be evaluated from the Ib and Beta mismatch in low level injection region and the extrinsic resistance can be evaluated from the Ic and Ib mismatch in the high current region. The mismatch evaluation can be performed with as few as six measurements per device type per die site.

4:30 p.m. - 7:00 p.m. Poster Displays/Reception

WEDNESDAY, MARCH 15

8:00 a.m. - 9:00 a.m. Continental Breakfast

8:00 a.m. - 5:00 p.m. Registration

SESSION 5: MATCHING

9:00 a.m. - 10:40 a.m.

Co-Chairs: Willy Sansen, KU Leuven

Emilio Lora-Tamayo, Universidad Autonoma de Barcelona

9:00 Characterization of Systematic MOSFET

5.1 Transconductance Mismatch -*H. Tuinhout, Philips*

Research Laboratories, Eindhoven, The Netherlands

MOSFET Matching test structures with intentional (1%) layout offsets are used to validate a measurement technique for systematic MOSFET transconductance mismatch. The results demonstrate that the used technique is capable of characterising systematic transconductance mismatches well below 1%. This can be very relevant for high precision analogue signal processing applications.

9:20 On the Matching Behavior of MOSFET Small

5.2 Signal Parameters - *R. Thewes, C. Linnenbank,*

U. Kollmer, S. Burges, M. DiLeo, M. Clinchy, U. Schaper, R. Brederlow, R. Seibert and W. Weber, Infineon Technologies, Munich, Germany

An array test structure for precise characterization of the matching behavior of MOSFETs is presented. Besides the standard mismatch parameter drain current ID, the high resolution measurement principle allows for characterization of the small signal parameters transconductance agm and in particular differential output conductance gDS. Measured data are shown to demonstrate the performance of the method. The width and length dependence of the normalized standard deviation of gDS clearly deviates from the well known relation (WL)-1/2 found for the parameters ID and gm.

9:40 A Differential Floating Gate Capacitance MisMatch

5.3 Measurement Technique - *J. Hunter, P. Gudem and S. Winters, Cadence Design Systems, Inc., San Diego, CA*

This paper describes a differential floating gate capacitance matching measurement technique that offers a significant improvement in resolution over those previously reported. The differential floating gate circuit consists of two matched standard floating gate structures. It's smaller differential output voltage can be measured to a much higher precision than the output voltage of a standard structure. In addition, the differential technique offers superior cancellation of parasitic overlap capacitance effects over the standard floating gate technique. Our technique was successfully demonstrated on a 0.50um analog BiCMOS technology.

10:00 MOSFET Transistor Matching in 0.15um CMOS

5.4 Process - *C. Rezvani and G. Srinivasan, Philips Semiconductor, Inc., San Jose, CA*

In this paper the result of matching study in 0.15 micrin CMOS process technology is presented. Both NMOS and PMOS devices are studied and discussed. For each case three kinds of devices are studied which are low Vt, high Vt, and thick (67A) gate oxide. Both high Vt and low Vt devices are with thin (32A) gate oxide. The test structures used for this study are discussed. The matching study, which is based on three main electrical parameters, Vt, Ids, and Gm are presented and discussed.

10:20 A Novel Approach for Precise Characterization of

5.5 Long Distance Mismatch of CMOS Devices - *U. Schaper, C. Linnenbank and R. Thewes, Infineon Technologies AG, Munich Germany*

A new test structure is presented for the characterization of long distance mismatch of CMOS devices. A single circuit is used to characterize both transistors and resistors. High resolution is achieved by applying a four-terminal method with regulated reference potential to compensate for parasitic resistance effects. Measured data are presented for differenct CMOS processes to demonstrate the performance of this approach. In particular, the long distance matching behavior is compared to that of neighboring devices and examples for linear and nonlinear distance dependencies are shown.

10:40 a.m. - 11:10 a.m. Break

SESSION 6: RELIABILITY I

11:10 a.m. - 12:10 p.m.

Co-Chairs: Yoshiaki Hagiara, Sony Corp.

Toshiharu Watanabe, Toshiba Corporation

11:10 Electromigration Test Structure Designed to

6.1 Identify Via Failure Modes - *T.S. Sriram,*

Compaq Computer Corp., Shrewsbury, MA

A new type of electromigration test structure has been demonstrated, which allows detailed understanding of the electromigration behavior of inter-level vias. It is designed to test each via interface independently. It also allows easy failure analysis by constraining the failure location. An example of its application is provided, where a change in the via process led to improved electromigration behavior. The use of this test structure allowed the identification of physical mechanisms for the improved electromigration behavior.

11:30 Reliability Evaluation Method of Low Temperature

6.2 Poly-Silicon TFTs Using Dynamic Stress - *Y. Uraoka, T. Hatayama and T. Fuyuki, Nara institute of Science and Technology, Nara, Japan*

Evaluation method of reliability of low temperature polu-Si using dynamic stress is proposed. Decrease of mobility and ON current was observed under the dynamic stress. We have found that the degradation depends strongly on falling time and frequency. This degradation is dominated by hot electron and can be improved by adopting LDD structure.

11:50 Influence of Input Voltage Swing on 0.18 µm

6.3 NMOS Aging Estimated by Self-Stressing Testers *S. Chetlur, J. Zaneski, L. Mullin, A. Oates, R. Ashton, H. Chew and J. Zhou, Lucent Technologies, Bell Laboratories, Orlando, FL*

Self-stressing structures are used to study the impact of input voltage swing on the hot carrier aging behavior of 0.18 NMOS devices in inverters. The input frequency appears to be a main factor in deciding the effective aging time and for a constant stree frequency, voltage overshoot/undershoot of 0.5V does not significantly alter the aging characteristics of the NMOS devices.

12:10 p.m. - 2:10 p.m. Awards Luncheon

(Bonzai Room)

SESSION 7: PARAMETER EXTRACTION

2:10 p.m. - 3:30 p.m.

Co-Chairs: Alexander Rahm, Infineon Technologies AG

Kjell O. Jeppson, Chalmers University of

Technology

2:10 Physically-Based Effective Width Modeling of

7.1 MOSFETs and Diffused Resistors - *C. McAndrew, S. Sekine*, A. Cassagnes and Z. Wu, Morola, Inc., Tempe, AZ, *Motorola Japan, Ltd., Sendai-shi, Japan*

This paper presents effective DC electrical width models for MOSFETs and diffused resistors. The models account for the geometric width dependence on the LOCOS effect and the dog-bone (or webbing) effect, for devices defined by field oxide, and on the finite dopant source effect for lowly doped resistors. The models are physically-based, C-continuous functions of geometry, and significantly improve modeling of MOSFETs and resistors over geometry.

2:30 Characterization and Modeling of LDMOS

7.2 Transistors on a 0.6µm CMOS Technology -

E. Griffith, J. Power, S. Kelly, S. Whiston, D. Bain and M. O'Neill, Analog Devices, Limerick, Ireland

The lateral double-diffused MOS (LDMOS) transistor has recently become the power device of choice. This is due in no small part to the ease by which LDMOS transistors can be integrated into an advanced mixed-signal process in order to realize high-voltage integrated circuits (HVIC's). A family of multi voltage rated LDMOS devices has been integrated into a conventional 0.6µm mixed-signal CMOS process. In the absence of a sutable physical predictive SPICE-compatible model for the LDMOS transistor, it was decided to employ a more practical and flexible subcircuit approach based around the widely used BSIM3 MOS model. Subcircuit elements were utilized to augment the BSIM3 model and model effects such as voltage-controlled resistances, quasi-saturation, interconnect metallization, and the highly voltage dependent gate-to-drain feedback or Miller effect capacitance. In addition, the dependence of the key specific on-resistance and breakdown voltage LDMOS device parameters on some basic LDMOS device design variables will be shown with measured data.

2:50 New Method for Parameter Extraction in Deep

7.3 Submicrometer MOSFETs - *C. Mourrain, B. Cretu*, G. Ghibaudo* and P. Cottin, France Telecom CNET, Grenoble, France and *LPCS, UMR CNRS, ENSERG, Grenoble, France*

A new method for the MOSFET parameter extraction including second order mobility attenuation is proposed. The advantage of the method is to remain compatible with previously existing ones avoiding second order derivative procedure and therefore to be applicable for in line parametric test extraction in the microelectronics industry.

3:10 SPICE Sensitivity Analysis of a Bipolar Test

7.4 Structure during Process Development - *N. Rankin, A.J. Walton, J. McGinty*, and M. Fallon*, The University of Edinburgh, Edinburgh, Scotland and *National Semiconductor UK Ltd., Greenock, Scotland*

This paper presents a methodology for predicting the effect of process input parameter variation on SPICE parameters early in the development of a new process. This is achieved by using TCAD generated measurement data calibrated from test structure measurement data gathered from an initial process. This methodology enables the same extraction strategy to be performed on TCAD and physical measurement data throughout the development of a semiconductor process ensuring data integrity. This assists both the process integration engineer and the design engineer in the optimisation of a process.

3:30 p.m. - 4:00 p.m. Break

SESSION 8: PROCESS CHARACTERIZATION

4:00 p.m. - 5:20 p.m.

Co-Chairs: Bill Verzi, Hewlett-Packard

Hans Tuinhout, Philips Research

4:00 Embedded Compact Test Structure with a

8.1 Comparator for Rapid Device Characteristic Measurement - *J. Goto and S. Kuwabara, NEC Corporation, Kawasaki, Japan*

Recent development of high performance SOC requires a lot of expensive and time-consuming evaluation of device characteristics at the process development stage. This paper introduces a new test structure to measure them with drastically reduced run-time/chip-area overhead, and shows possibility to unify design for functionality/device-characteristics test.

4:20 Characterization of Trench Isolation for BiCMOS

8.2 Technologies - *J. Klootwijk, G. Muda and D. Terpstra, Philips Research Laboratories, Eindhoven, The Netherlands*

We have developed and characterized new test structures for deep and shallow trench isolation in deep submicron BiCMOS technologies, enabling accurate characterization of influences of trench isolation on device performance. In particular capacitances, breakdown mechanisms and leakage currents can be investigated, without the necessity of fully processed lots. Electrical characterization is performed by capacitance and I-V measurements. This paper discusses the test structures, measurement methods (especially separation of capacitance contributions) and some trends extracted from measurement results that were obtrained with the test structures.

4:40 Optimization of Low-k Dielectric (Flourinated

8.3 SiO2) Process and Evaluation of Yield Impact by Using BEOL Test Structures - *S. Hsieh, K. Doong, Y.-H. Ho, S.-C. Lin, B. Shen, S.-M. Tseng, Y.-H. Yang and C. Hsu*, Worldwide Semiconductor Manufacturing Corporation, Shinchu, Taiwan and *National Tsing-Hua University, Republic of China*

This work describes the optimization of low-k dielectric process and evaluation of yield impact by using back end of line (BEOL) test structures. Three splits of low-k dielectric process as compared with HDP-USG process is electrically characterized with the test structures of the BEOL unit process and integration process. The interconnect capacitance is used as the optimization criteria of low-k dielectric process and the yield impact is reviewed for the concern of manufacturing.

5:00 Characterisation of Aluminium Passivation for

8.4 TMAH Based Anisotropic Etching for MEMS Applications - *K. Liam, S. Smith, N. Rankin, A.J. Walton, A. Gundlach, and T. Stevenson, The University of Edinburgh, Edinburgh, Scotland*

A cross-bridge linewidth test structure has been used to analyse, both electrically and physically, the effect of a new anisotropic silicon etch composition that has been designed to have an increased selectivity with aluminium. To characterise the effect of the etch on aluminium tracks, electrical measurements have been made to obtain sheet resistance and linewidth. These results are presented in combination with SEM micrographs to evaluate the surface quality of the exposed aluminium.

6:00 p.m. Conference Banquet at Chateau Julien

THURSDAY, MARCH 16

8:00 a.m. - 9:00 a.m. Continental Breakfast

8:00 a.m. - 5:00 p.m. Registration

SESSION 9: RELIABILITY II

9:00 a.m. - 10:20 a.m.

Co-chairs: Giovanni Soncini, University of Trento

Timothy Turner, Keithley Instruments

9:00 Select Transistor Modulated Cell Array Structure

9.1 Test for EEPROM Reliability - *F. Pio and E. Gomiero, STMicroelectronics, Agrate Brianza, Italy*

A test structure essentially consisting of a not addressable EEPROM cell array is presented together with the measurement methodology. Accurate information on the threshold voltage distribution of the cells in the array is obtained from the transfer characteristic measured under select transistor clamping bias. We discuss in detail the working principle and the different levels of approximation, presenting several results for early process/design reliability evaluation (bake retention, control gate stress, programming pulse optimization).

9:20 Fowler Nordheim Induced Light Emmission From

9.2 MOS Diodes - *P. Bellutti, G. Betta, R. Versari*, A. Pieracci*, B. Ricco*, M. Manfredi**, G. Soncini***, ITC-IRST, Trento, Italy, *DEIS-University of Bologna, Bologna, Italy, **University of Parma, Parma, Italy, ***University of Trento, Trento, Italy*

Light emission from p- and n-type MOS tunnel diodes biased in the Fowler-Nordheim regime has been investigated by using especially designed test structures which avoid the obscuring effect of poly-Si layer, thus allowing an efficient light emission from the Si substrate. The measured photon energy distribution of the emitted light exhibits a peak at 1.6eV, never observed before. This effect has been tentatively attributed to impact ionization followed by hot carrier interband radiative recombination.

9:40 A Study of Test Structures to Detect Process

9.3 Thermal Cycle Induced "Voids" and Eliminate Them in an Oxide-Nitride-Oxide (ONO) Antifuse Based FPGA - *M. Bora, B. Cronquist, J.-J. Wang and J. McCollum, Actel Corporation, Sunnyvale, CA*

Three different test structures have been used to detect process thermal cycle induced "voids" in an oxide-nitride-oxide (ONO) antifuse cell integrated into a 0.50um standard CMOS process. Electrical and analytical studies showed that adequate test structures are necessary to detect the voids. Partition experiments were conducted to identify the process steps initiating and then propagating these voids. The appropriate test structure was then used to determine the new thermal cycle recipes necessary to resolve the cumulative thermo-mechanical voiding issue. The electrical data is discussed in detail, together with a brief overview of the analytical data.

10:00 Analysis of Hot-Carrier-Induced Degradation in

9.4 MOSFET by Capacitance Measurement at Cryogenic Temperature - *C. Hsu, M. Lau, Y. Yeow and Z. Yao*, The University of Queensland, Brisbane, Australia, *Quality Semiconductors Australia, Sydney, Australia*

In this paper we describe and demonstrate the use of gate-to-drain capacitance (Cgd) measurement at below liquid nitrogen temperature as a tool to characterize the hot carrier induced charge centers. Also a new method based on gate-to-substrate capacitance (Cgb), validated by means of two dimensional numerical simulation, is proposed to extract the spatial distribution of oxide interface fixed charges with reasonable accuracy.

10:20 a.m. - 10:50 a.m. Break

SESSION 10: RF

10:50 a.m. - 12:10 p.m.

Co-Chairs: Michael W. Cresswell, NIST

Franz Sischka, Agilent Technologies

10:50 A New Extraction Method of High Frequency

10.1 Noise Parameters in the Temperature Range-55/150 deg. For SiGe HBT in BiCMOS Process - *D. Gloria, S. Gellida and G. Morin, STMicroelectronics, Crolles, France*

High Frequency (HF) test structures for SiGe HBT and parameter extraction methodology are described to obtain HF merit figures (Ft, Fmax, minimum noise figure Nfmin, optimum source reflexion coefficient GammaOPT, and noise equivalent resistance RN) in the temperature range -55/150deg. The frequency range is 45MHz-110GHz for S parameters and 800MHz-4GHz for noise ones. Thanks to low substrate losses in these structures, a new fast de-embedding method for HF noise measurement is presented. Experimental data show an increase of base resistance, Nfmin, GammaOPT, Rn and a decrease of Ft, Fmax with increasing temperatures because of the electron mobility evolution.

11:10 Comparison Between S-Parameter Measurements

10.2 and 2D ElectroMagnetic Simulations for Microstrip Transmission Lines on BiCMOS Process - *J. Carpentier, S. Gellida, D. Gloria, G. Morin and H. Jaouen, ST Microelectronics, Crolles, France*

As the frequency increases for RF applications in silicon technology, the modeling of transmission lines is necessary. In this work, we propose to check the validity of the conventional measurement technique to extract the propagation parameters for structures in a standard BiCMOS process. To estimate this technique, the results are confronted with 2D electromagnetics simulations. On microstrip structures, the comparison shows that the conventional method is sufficient up to 18 GHz. Moreover, we highlight the effects of energy dissipation in the dielectric layers currently used in silicon process.

11:30 Comparing High-Frequency De-Embedding

10.3 Strategies: Immittance Correction and In-Situ Calibration - *R. Gillon, D. Vanhoenacker* and L. Martens**, Alcatel Microelectronics, Oudenaarde, Belgium, *Universite Catholique de Louvain,Belgium, **INTEC, Belgium*

A comparison is made between the widely used immittance correction technique (dummy de-embedding) and the newer in-situ calibration. The accuracy of the immittance correction technique is limited by the assumption that the reference structures have ideal characteristics. Using in-situ calibration the true characteristics of these structures can be measured so that the accuracy limitations of immittance corrections can be assessed exactly. In-situ calibration appears to be inherently more accurate and flexible, especially on lossy silicon substrates.

11:50 Ground-Shielded Measuring Technique for

10.4 Accurate On-Wafer Characterization of RF CMOS Devices - *T. Kolding, O. Jensen and T. Larsen, Aalborg University, Aalborg, Denmark*

This paper presents a new ground-shield based test fixture for gigahertz on-wafer device measurements over lossy substrates. Fixture features include (i) accurate common ground, (ii) effective removal of substrate carried coupling (iii) few well-defined parasitics for simplified de-embedding, and (iv) compatibility with arbitrarily large devices. Required in-fixture standards can be fabricated with very high accuracy; even in standard CMOS processes. The high applicability of the method is demonstrated with measurement data for structures fabricated in 0.25µm bulk and 0.5µm epitaxial CMOS technologies.

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