CONFERENCE PROGRAMME 1997 IEEE INTERNATIONAL CONFERENCE ON MICROELECTRONIC TEST STRUCTURES

March 17 - 20, 1997
DOUBLETREE HOTEL AT
FISHERMAN'S WHARF
MONTEREY, CALIFORNIA

Sponsored by IEEE Electron Devices Society

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Technical Program Committee

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CHAIRMAN'S LETTER

Dear Colleague,

On behalf of the Committee I would like to invite you to the 1997 International Conference on Microelectronic Test Structures. The Conference is sponsored by the IEEE Electron Devices Society and will bring together designers and users of test chips from all over the world to discuss recent developments and future directions regarding the design, measurement, and application of microelectronic test structures. This is the 10th time for ICMTS as an international conference. Before 1988 the Conference met on an every other year basis as a workshop. The Conference has been able to maintain the friendliness of a workshop by providing ample social activities to ensure that participants get the chance to meet others in their field and learn from each other's experiences.

This year's conference consists of 48 papers in 9 sessions including a poster session with 14 papers. The sessions include topics on parameter extraction, device and process characterization, reliability, dimensional measurement, and yield. Authors of the poster session will present an oral summary of their work to the general audience. There will also be an equipment exhibit. In addition to the displays of equipment, each of the exhibitors will have the opportunity to give a short presentation describing their latest products. A reception will follow the equipment exhibitor's presentation.

On Monday, March 17, preceding the Conference a short course tutorial will be held to overview the main topics comprising the field of microelectronic test structures. A wine and cheese get-together will be held following the tutorial. The Conference banquet will be held on Wednesday evening in the Monterey Bay Aquarium. The Monterey Bay Aquarium is a world-class aquarium which features the plants and animals of Monterey Bay. The aquarium has opened a major addition within the last year specializing in the nearby deep ocean.

The Conference will be held at the DoubleTree Hotel just across the street from Fisherman's Wharf in the center of Monterey. Both the DoubleTree Hotel and the charming town of Monterey will provide an excellent

site for a very rewarding technical experience.

Sincerely,

Robert Ashton

General Chairman

GENERAL INFORMATION

The 1997 IEEE ICMTS will be held at the DoubleTree Hotel at Fisherman's Wharf in Monterey, California. The Conference headquarters hotel will provide guest accommodations as well as meeting facilities for all attendees. The technical program, which will consist of nine sessions of contributed papers and a poster session, will be held March 18 through 20. A short course entitled "An Introduction to the Design, Measurement, and Analysis of Microelectronic Test Structures" will be offered on March 17.

CONFERENCE REGISTRATION

Preregistration is encouraged. To preregister, use registration form in this booklet. Please fill out all spaces completely. Note that the fees are higher for registration forms received after January 15, 1997. You may mail your registration form with a check drawn on a US bank in US funds only. To fax your registration form, you must include credit card information, and the 5% processing fees for all credit card transactions. To e-mail your registration and pay by credit card, a fax with your signature authorizing All About Meetings, Inc. to charge your credit card for registration fees must also be forwarded.

Mail your conference registration form and remittance to:

1997 IEEE ICMTS CONFERENCE
C/o ALL ABOUT MEETINGS, INC.
1650 S. Pacific Coast Hwy., Suite 209
Redondo Beach, CA 90277
(310) 316-5153 - Telephone
(310) 316-0713 - Fax
70541.1225@Compuserve.com - e-mail

Call the above telephone number for registration information only. Telephone registrations will not be accepted. Registrations should be mailed no later than March 3, 1997, or arrangements should be made to hand carry fees to on-site registration.

Payment for fees at the Conference must be in US funds and by check drawn on a US bank, cash, US dollars traveler's checks, or one of the following credit cards: American Express, Visa, or MasterCard.

CANCELLATIONS

Due to advance financial commitments, refunds of registration fees requested after March 1, 1997 cannot be guaranteed. A $25.00 processing fee will be withheld from all refunds. Consideration of requests for refunds will be processed after the Conference.

ON-SITE REGISTRATION SCHEDULE

On-site registration for the Conference will be conducted in the DoubleTree Hotel's De Anza Foyer as scheduled:

Sunday,	March 16	6:00pm - 8:00pm
Monday,	March 17	7:00am - 5:00pm
		7:00pm - 9:00pm
Tuesday,	March 18	7:30am - 5:00pm
Wednesday,	March 19	7:30am - 4:00pm
Thursday,	March 20	7:30am - 12:30pm

Registration fee includes admittance to the Technical sessions, continental breakfast on Tuesday, Wednesday, and Thursday, Exhibit Reception Tuesday at 5:30pm, banquet at the Monterey Bay Aquarium on Wednesday at 7:00pm, Lunch Tuesday and Wednesday, one copy of the proceedings, and admittance to the exhibits.

HOTEL INFORMATION

The DoubleTree Hotel at Fisherman's Wharf is a complete resort hotel located in the heart of Monterey and has 374 guest rooms, many with spectacular bay views. Dining is available in the California Grill from 6:00am to 10:00pm and is open for breakfast, lunch, and dinner. In addition, the Lobby Lounge features wide screen TV and Peter B.'s Pub. Room service is available from 6:00am to 11:00pm. It is located in downtown Monterey, which has many resturants, coffee shops, and stores and is within walking distance of Fisherman's Wharf.

Reservations can be made by completing the Hotel Registration Form. Fill out the appropriate section of this form and mail it to the DoubleTree Hotel at Fisherman's Wharf. Hotel reservations can also be made by calling the hotel or faxing your registration form.

DoubleTree Hotel at Fisherman's Wharf
2 Portola Plaza
Monterey, CA 93940
(408) 649-4511 Hotel Telephone
(408) 649-3109 Hotel Reservation Fax
(800) 222- TREE (8733) Reservations Toll Free

The hotel cut-off date for ICMTS's group reservations is February 15, 1997. After February 15, hotel accommodations will be available on a space-available basis only, at the regular, higher rate. March is a busy time in Monterey; therefore, you are urged to make reservations as soon as possible. The group rate is $110.00 per day.

Parking is available, Valet is $11.00 per day, and self parking is $9.00 per day. There is public parking available at a nominal charge located one block from the hotel.

TRANSPORTATION

By Air: Monterey Peninsula Airport is served by American Eagle, United, United Express, Skywest/Delta, Alaska, Continental, and Northwest Airlines. There are more than 100 arrivals and departures daily to and from San Francisco, San Jose, and Los Angeles, with connections to all domestic and international locations. The distance from the airport to the DoubleTree is approximately four miles.

By Car: The drive from San Jose is approximately 60 miles; San Francisco is approximately 120 miles.

Airport/Ground Transportation: Taxi service is recommended. The cost is approximately $10.00.

RENTAL CARS

The following rental car agencies are located at the Monterey Airport: Avis, Budget, Dollar, Hertz, National, and Thrifty.

MESSAGES

Messages can be left for attendees during registration and will be posted on the message board. Call the hotel direct (408) 649-4511 and ask for IEEE registration. Messages for attendees who are hotel guests can also be left for the individual in their room, or you may forward a fax to a hotel guest at the guest fax number which is 1-408-372-0620.

WEATHER

Monterey enjoys a unique weather pattern, with coastal temperatures averaging 57 degrees year-round. The average maximum temperature in March is 62 degrees, and average minimum temperature is 45 degrees. It is advisable to bring a sweater, jacket, or coat.

MONTEREY AREA ATTRACTIONS

Monterey Bay Aquarium - This fascinating, internationally acclaimed aquarium focuses on educating visitors about the mysteries and wonders of the Monterey Bay. Conference attendees will be able to purchase tickets to the Aquarium at a discount if they wish to return on Thursday after the banquet.

Big Sur - A 90-mile stretch of coastline that begins in Monterey County a few miles south of Carmel and ends in San Luis Obispo County at San Simeon (Hearst Castle).

Cannery Row - An historic area of the city of Monterey, located on the Bay between the Coast Guard wharf and the Pacific Ocean border.

Carmel-by-the-Sea* - A village in a forest setting located above a breathtaking white-sand beach 5 miles south of Monterey and 26 miles north of Big Sur just off Highway One.

Carmel Valley - Twelve miles due east of Carmel-by-the-Sea.

Fisherman's Wharf & Wharf II - Located on Monterey Bay, in the historic heart of Monterey, off of Del Monte Avenue.

Pebble Beach* - On the southern tip of the Monterey Peninsula, due west of Monterey and due north of

Carmel-by-the-Sea.

Hearst Castle - A California State Historical Monument containing 165 beautifully furnished rooms, a huge collection of art and antiques, impressive swimming pools, gardens, and terraces. Located 90 miles south of Monterey.

*See Tour for more information

MONTEREY/CARMEL TOUR

What a perfect conclusion to the Conference. A new feature this year will be a tour of Monterey's Seventeen Mile Drive (Pebble Beach), a must see, and famous Carmel. The bus will depart at 1:30pm and return at 5:30pm. Don't forget your camera. The tour is limited to 47 passengers, so sign up early to avoid disappointment.

Tour: Seventeen Mile Drive and Carmel by the Sea

Cost: $35.00 per person

Located in the Del Monte Forest, the 17-Mile Drive winds through groves of Monterey pine and Monterey cypress and along a spectacular coastline populated by seals, sea lions, and sea otters. Guests will view castle-like mansions, championship golf courses, and enjoy one of the most beautiful residential areas in the world. Stops will be made for photo opportunities. After the 17-Mile Drive we'll continue to Carmel-by-the-Sea.

The one-square-mile hamlet is a charming collection of flower-bower cottages and regal residences set in the heart of a pine forest on the edge of the Pacific Ocean. The village is full of unique shops featuring an extraordinary range of treasures. Guests will browse an array of fascinating clothing in Carmel's unique and sophisticated boutiques. In the peninsula's "art colony", they will discover the hidden treasures tucked away in its nooks and crannies. They will visit the ever-changing exhibits of rare, museum-quality hand-blown glass, fine woodworkings, original graphics, and watercolors. Guests will shop in Carmel for approximately one and one half hours.

This tour will be narrated, so the many points of interest will not be overlooked.

TECHNICAL SESSION INFORMATION

The technical session will be held in Rooms DeAnza II and III.

POSTER SESSION INFORMATION

The poster session will be held Wednesday at 2:40 pm, at which time authors will give a brief 5 minute talk describing their poster in De Anza II and III. The general session will then move to De Anza I where authors will be available at their posters for questions and discussion.

Posters will be displayed from Tuesday at 1:00pm until Thursday at 12:00 noon.

EQUIPMENT EXHIBITS

ICMTS vendor exhibits will be displyed in De Anza Ballroom I, on Tuesday, March 18, from 1:00pm, and will remain on display until noon on Thursday, March 20.

A five minute oral presentation will be held in De Anza II & III at 4:40 pm on Tuesday, March 18, 1997.

For information and an application to exhibit at the 1997 ICMTS, please contact Jim Reedholm, or Karen Kinton at Reedholm Instruments, (512) 869-1935. As of November 20, 1996, the following exhibitors have reserved exhibit space:

Sandia National Laboratories
Cascade Microtech
Hewlett Packard
QualiTau Incorporated
Lucas/Signatone Corp.
Reedholm Instruments

FOOD AND BEVERAGE FUNCTIONS

Registration Welcome Reception

The Welcome Reception will be held on Monday, March 17 from 7:00pm to 9:00pm in the De Anza Foyer and De Anza I. Wine and cheese will be served.

Continental Breakfast/Coffee Breaks

Continental breakfast will be served on Monday, March 17 from 7:00am-8:30am, and on Tuesday, Wednesday, and Thursday, March 18-20 from 7:30am-8:30am, in the De Anza Foyer (outside the exhibit area). The coffee breaks will also be held in the De Anza Foyer.

Lunch

Lunch will be served on Monday, Tuesday, and an Awards Luncheon on Wednesday, March 17-19, in the Bonsai Ballroom.

Poster & Equipment Reception

The Reception will be held on Tuesday, March 18 at 5:30pm in the De Anza Foyer and De Anza I.

Conference Banquet

The Conference Banquet will be held on Wednesday, March 19 at the Monterey Bay Aquarium. Round trip bus transportation will be provided. Buses will depart from the front of the hotel starting at 6:00pm. Attendees can visit the exhibits from 7:00pm-8:00pm, at which time dinner will be served. In addition, there will be time to walk through the aquarium after dinner until 11:00pm.

One banquet ticket is included with one Technical Session Registration. Additional guest tickets are available at the cost of $55.00.

TUTORIAL SHORT COURSE

An Introduction to the Design, Measurement, and Analysis of Microelectronic Test Structures

The ICMTS Tutorial is a one-day short course intended to provide the non-expert with the fundamentals associated with microelectronic test structures. The course strives to provide good design, test, and analysis guidelines so that superior test-structure practice will be followed, thus paving the way for improved process control, higher product yield, and rapid product introduction. The course instructors, chosen by Dr. Buehler for this year's tutorial, have many years of experience in the field of test structure design, test, and analysis. The format will be interactive with emphasis on the practical use of microelectronic test structures.

AGENDA

Monday, March 17, 1997

7:30am	Registration	Continental Breakfast
8:25am	WELCOME	Robert Ashton, Lucent Technologies, USA
8:30am	INTRODUCTION	Test Structure Fundamentals
		Martin Buehler, JPL, USA
9:15am	ALIGNMENT	Overlay, Registration, and Feature Placement Structures
		Richard Allen, NIST, USA
10:00am	Break	
10:30am	YIELD	Concepts in Yield Management
		Akella Satya, IBM Corporation, USA
11:15am	RELIABILITY	Wafer-Level Reliability Testing
		Tim Turner, Keithley Instruments, USA
12:00pm	Hosted Lunch	
1:15pm	FEMTO	Low Current Measurement Techniques
		Satoshi Habu, Hewlett Packard, Japan
2:00pm	MATCHING	Transistor Characterization
		Hans Tuinhout, Philips Research Labs., The Netherlands
2:45pm	Break	
3:15pm	MEMS	Structures for Electromechanical Devices
		Robert Puers, Katholieke Universiteit Leuven, Belgium
4:00pm	PROCESS CORNERING	Worst Case Parameter Methodology
		Ellen Piccioli, Digital, USA
4:45pm	Wrap-up	

TUTORIAL OUTLINE

1. INTRODUCTION - Test Structure Fundamentals:

Martin Buehler, JPL, Chair

- Tutorial Overiew
- Probe pad design
- The 2xN probe pad array
- Four-terminal Kelvin measurement technique
- Bridge/cross resistors for sheet and linewidth measurements
- measurements
- Design curves for linewidth measurements
- Three-terminal capacitor measurements
- Matrixed test structures

2. ALIGNMENT - Overlay, Registration, and Feature Placement:

Richard Allen, NIST, Instructor

- Introduction/background
- Optical structures
- Electrical structures
- Metrology comparisons
- Recent advances

3. YIELD - Concepts in Yield Management:

Akella Satya, IBM, Instructor

- Statistical basis of yield
- Development of yield models
- Critical areas and assessment
- Defect monitoring techniques
- Test structures and design
- Examples of applications

4. RELIABILITY - Wafer-Level Reliability Testing:

Tim Turner, Keithley, Instructor

- Traditional reliability assurance
- "Rate of degradation" measurements for process control
- Electromigration
- Time dependent dielectric breakdown
- Enhanced process control feedback
- - Short feedback loop
- - Hierarchical test techniques

- Enhanced sample selection techniques
- Test based on failure mechanisms
- - Electromigration
- - Threshold voltage instabilities

5. FEMTO - Low Current Measurement Techniques:

Satoshi Habu, HP, Japan, Instructor

- Basic knowledge for low current measurement:
- noise source, guarding techniques, shielding, reducing cable noise
- Actual problems of wafer probe station
- How to check your measurement environment
- How to use measurement instruments effectively

6. MATCHING - Transistor Characterization:

Hans Tuinhout, Philips Research Labs, Instructor

- Introduction and motivation
- Mismatch effects
- Measurement methods
- Test structures
- - Rules
- - Examples
- Modeling and matching numbers

7. MEMS - Structures for Electromechanical Devices:

Robert Puers, Katholieke Universiteit Leuven, Instructor

- Etching technologies for miniaturized mechanical structures
- Newly developed technologies for 3D structures in silicon
- Compensation structures for convex corners
- "Electrodeless" electrochemical etchstop technique
- Design strategies for mechanical stability
- Design strategies for low power consumption

8. PROCESS CORNERING - Worst Case Parameter Methodology:

Ellen Piccioli, DEC, Instructor

- History of Worst Case Files (WCF) and related test structures IP o Pessimistic worst case estimation from measured parameters
- Introduction of device simulation for WCF generation
- Empirical approximations
- Statistical WCF
- Use of process and device simulators when data is not available

- General results from an example
- Commercially available tools
- Performing chip design before data is available
- Flexibility of methodology: simple or complex

TUTORIAL INSTRUCTORS

Martin Buehler

Chairman, California Institute of Technology

Martin Buehler received his BSEE and MSEE from Duke University in 1961 and 1963, respectively, and his Ph.D. in EE from Stanford University in 1966, with the specialization in Solid State Electronics. He worked at TI and NBS (now NIST), and since 1981 has been with the Jet Propulsion Laboratory where he is a Senior Research Scientist in the Microdevices Laboratory. He was principal investigator for the Clementine RRELAX (Radiation and Reliability Assurance Experiment) and the Mars '96 MAPEX (Microelectronic and Photonic Exposure Experiment) and provided total radiation dosimetry for the Space Technology Research Vehicle spacecrafts and Telstar and Intelsat communication satellites. Currently, he is the co-lead for In situ Instruments and MEMS in the New Millennium Program. He has authored over 70 papers and holds seven patents on novel microelectronic devices and test structures. He is co-founder of the IEEE ICMTS and has served as its General Chairman, Technical Chairman and Finance Chairman. Martin is a member of the IEEE Electron Devices Society and the Nuclear Science Society.

Richard Allen

National Institute of Standards and Technology

Richard Allen received his B.S. and M.S. degrees in Physics from Rensselaer Polytechnic Institute, Troy, New York, in 1982 and 1984, respectively. From 1984-1989 he was with the VLSI Technology Group at the Jet Propulsion Laboratory, Pasadena, California. At JPL he developed test structures for in-situ monitoring of space radiation effects on VLSI devices and circuits. From 1989-1990 he was with College Park Software in Altadena, California, an AI development company specializing in LISP-based expert systems tools. Since June 1990 he has been with the Integrated Circuits Technology Group of the National Institute of Standards and Technology in Gaithersburg, Maryland. His present interests include developing electrical test structures for submicrometer metrology of VLSI devices. Mr. Allen is a member of the American Physical Society and the IEEE.

Akella Satya

IBM Corporation

Akella Satya received his B. Tech. (Hons) and M.Tech. (Metal Physics) degrees from the Indian Institute of Technology, Kharagpur, India, where he served as an Associate Lecturer through 1962. He was the chief metallurgist at the Midwest Machine Co., Marysville, Michigan through 1966, received the Ph.D. in Materials Science from the Michigan State University in 1969, then joined the IBM Corporation as a Staff Engineer and is now retired. Dr. Satya's contributions are in process development, device, design, and yield management and used in sub-0.5um CMOS Fab. Dr. Satya is a member of Sigma Xi, IEEE, ASM, ECS, and a Founder-Life-Member of the Indian Society for the Advancement of Materials and Process Engineering. He

holds several patents, authored many papers, and served as a mentor for SRC/Canegie-Mellon University on yield modeling. He has been a member of the Technical Program Committee of IEEE ICMTS.

Timothy Turner

Keithley Instruments

Timothy Turner has more than 23 years of experience in the field of semiconductor reliability. He has worked for semiconductor manufacturers such as Mostek Corporation and SGS-Thomson. For the past 10 years he has owned Turner Engineering Technology (TET), a consulting company specializing in the field of Wafer Level Reliability Testing. Mr. Turner is now Director of Test Structures for Keithley Instruments following their acquisition of TET in 1996. Mr. Turner has published many papers in the field of Wafer Level Reliability Testing and semiconductor reliability. He has several patents on semiconductor processing techniques and has lectured on this topic through the UCLA extension center.

Satoshi Habu

Hewlett-Packard, Japan

Satoshi Habu received his B.S. and M.S. degree in Electrical Engineering from Ibaraki University in 1981 and 1983, respectively. In 1983 he joined Hewlett-Packard Japan, Ltd. as R&D engineer. He has been responsible for developing instruments for semiconductor parameter measurements. He is currently heading projects which develop instrumentation for wafer level testing.

Hans Tuinhout

Philips Research

Hans Tuinhout received his MSEE degree from the University of Technology of Delft (NL), in 1980. Since then Hans worked at Philips Research Laboratories in Eindhoven (NL), interrupted by a sabbatical year at the ECE Department of Carnegie-Mellon University, Pittsburgh, Pennsylvania. During his professional career, Hans has always been involved with device characterization for CMOS and BiCMOS processes. Currently Hans works as Senior Scientist in the Semiconductor Device Architectures group at Philips Research. His research activities are focused on very accurate DC device measurements for matching characterization. Hans is a member of the IEEE Electron Devices Society and member of the ICMTS Technical Program Committee. He served as Technical Program Chairman for the ICMTS 1989. Hans is a part-time instructor for the Philips Centre for Technical Training where he teaches IC-technology and Bipolar and MOS device characterization.

Robert Puers

Katholieke Universiteit Leuven

Robert Puers recieved his B.S. degree in electrical engineering in Ghent in 1974, and his M.S. degree at the Katholieke Universiteit Leuven in 1977, where he obtained his Ph.D. in 1986. He is Professor at the Katholieke Universiteit Leuven, Belgium, and is director of the clean room facilities for silicon wafer processing and for hybrid circuit technology at the ESAT-MICAS laboratories. Since 1987 he established a group working on mechanical sensors and silicon micromachining, and on packaging techniques, for

biomedical implant systems as well as for high performance industrial devices. In addition, his general interest is in low power telemetry systems, with the emphasis on intelligent interface circuits and inductive power and data links. He is involved in the organization, reviewing, and publishing activities of many conferences, journals, and workshops in the field of biotelemetry, sensors, actuators, micromachining, and microsystems. Professor Puers is teaching courses in 'Production Techniques for Electronic Circuit Manufacturing,' and in 'Biomedical Instrumentation and Stimulation.' He is the author of more then 130 papers on biotelemetry, sensors, or packaging in journals or international conferences. He is a senior member of the IEEE, council member of the International Society on Biotelemetry, and member of the International Society for Hybrid Microelectronics and the Electron Device Society.

Ellen Piccioli

Digital Equipment Corporation

Ellen Grant Piccioli received her B.S. in Electrical Engineering from Cornell University in 1986, and the M.S. in Electrical Engineering from the University of Michigan in 1991. After working at Digital Equipment Corporation from 1986 to 1989 as a Yield Enhancement Engineer, Ellen received a fellowship from Digital to pursue a graduate education. Ellen returned to Digital's Advanced Semiconductor Development Group as a Device Engineer from 1991 to 1994. Currently, Ellen is the team leader of the Test Chip Group in the CMOS Process Integration area at Digital Semiconductor. Ellen is a member of IEEE and SWE.

TECHNICAL SESSIONS

The technical program consists of 34 oral and 14 poster papers. The Technical Sessions and Session Chairs are:

Session 1: Process Characterization

Kjell Jeppson, Co-Chair, Al Ipri, Co-Chair

Session 2: Linewidth and Overlay

Emilio Lora-Tamayo, Co-Chair Akella Satya, Co-Chair

Session 3: Bipolar and High Frequency

Hans Tuinhout, Co-Chair, Yoichi Tamaki, Co-Chair

Session 4: Reliability

Loren Linholm, Co-Chair, Edward Hakim, Co-Chair

Session 5: Interconnects and Capacitance

Yoshiaki Hagiwara, Co-Chair, Michael Cresswell, Co-Chair

Session 6: Dielectric Characterization

Dieter Schroeder, Co-Chair, Martin Buehler, Co-Chair

Session 7: Posters

Anthony Walton, Co-Chair, Takashi Ohzone, Co-Chair

Session 8: Parameter Extraction and Matching

Lawrence Bair, Co-Chair, Gerard Ghibaudo, Co-Chair

Session 9: Sensors and Micromachining

Giovanni Soncini, Co-Chair, Alfred Papp, Co-Chair

PROGRAM SCHEDULE

Monday, March 17, 1997

7:00 - 9:00 PM REGISTRATION RECEPTION

TECHNICAL PROGRAM

Tuesday, March 18, 1997

7:00am CONTINENTAL BREAKFAST
7:30am REGISTRATION
8:50am WELCOME
Robert Ashton, General Chair
Larry Bair, Technical Program Chair
Loren Linholm, Local Arrangements Chair

SESSION 1 PROCESS CHARACTERIZATION

Co-Chairs: Kjell Jeppson, Chalmers University of Technology, Sweden and Al Ipri, David Sarnoff Research Center, USA

9:00am
Determination of Defect Size Distributions Based on Electrical Measurements at a Novel Harp Test Structure
C. Hess and L.H. Weiland, University of Karlsruhe,Germany

9:20am

Yield Prediction Using Calibrated Critical Area Modelling
G.J. Gaston, G.E.C. Plessey Semiconductors, UK

9:40am

Test Structures for Hillock Growth, via Filling and for Measuring the Quality of Thin Films
D.J. Bennett, A. O'Hara, I. Underwood, and A.J. Walton, University of Edinburgh, UK

10:00am

BREAK

SESSION 2 LINEWIDTH AND OVERLAY

Co-Chairs: Emilio Lora-Tamayo, Campus Universidad Autonoma de Barcelona, Spain and Akella Satya, IBM Corporation, USA

10:40am

Single-Crystal Test Structures for Electrical Linewidth Certification
M.W. Cresswell, L.W. Linholm, J.J. Sniegowski*, R.N. Ghoshtagore, and R.A. Allen, National Institute of Standards and Technology, and *Sandia National Laboratories, USA

11:00am

A Digital Test Structure for Simultaneous Bird's Beak Length and Misalignment Measurement in Polysilicon Emitter Bipolar Technologies
M. Ullan, M. Lozano, J. Santander, E. Lora-Tamayo, S. Nigrin*, J.E. Pohl*, P.H. Osborne*, and N. Morris*, Campus Universidad Autonoma de Barcelona, Spain and *GEC Plessey Semiconductors, UK

11:20am

Lateral Power MOSFET Low-Doped Drain (LDD) Misalignment Test Structures
I.M. Vitomirov, S.N. Seabridge, A.D. Raisanen, and T. Tellier, Xerox Corporation, USA

11:40am

Comparison of Modeled and Measured Kelvin Voltage Taps in Test Structures for CD and O/L Reference Materials
W.E. Lee, M.W. Cresswell*, R.A. Allen*, S.N. Jones*, J.J. Sniegowski**, W.F. Guthrie*, and L.W. Linholm*, Renishaw Tranducer Systems, UK, *National Institute of Standards and Technology, and **Sandia National Laboratories, USA

12:00pm

LUNCH

SESSION 3 BIPOLAR AND HIGH FREQUENCY

Co-Chairs: Hans Tuinhout, Philips Research, Netherlands and Yoichi Tamaki, Hitachi Corporation, Japan

1:40pm

Optical Signal Injection for High-Speed Wafer Level Function Test of Integrated Circuits
H.H. Berger, J. Sturm, F. Esfahani, A. Benedix, and K.O. Hofacker*, Technical University Berlin, and *Thesys GmbH, Germany

2:00pm

On Wafer Noise Measurement Using Bipolar Transistor RF Test Structures
S.D. Connor, GEC Plessey Semiconductors, UK

2:20pm

Flicker Noise Characterization of Polysilicon Resistors in Submicron BICMOS Technologies
O. Roux dit Buisson and G. Morin, SGA-Thomson, France

2:40pm

A Proposal for Modeling Substrate Coupling in Si-MMICs and its Experimental Verification up to 40 GHz

M. Pfost and H.-M. Rein, Ruhr-University Bochum, Germany

3:00pm

BREAK

SESSION 4: RELIABILITY

Co-Chairs: Loren Linholm, National Institute of Standards & Technology, USA and Edward Hakim, US Army LABCOM, USA

3:20pm

Digital Test Circuit Design and Optimization for AC Hot-Carrier Reliability Characterization and Model Calibration under Realistic High Frequency Stress Conditions

W. Jiang, H. Le, S.A. Kim, J.E. Chung, Y-J. Wu*, P. Bendix*, J. Jensen*, R. Ardans*, S. Prasad*, A. Kapor*, T.E. Kopley**, T. Dungan**, P. Marcoux**, Massachusetts Institute of Technology, *LSI Logic Corporation, **Hewlett-Packard Company, USA

3:40pm

New Method for the Parameter Extraction in Si MOSFETs After Hot Carrier Injection

S. Hardillier, C. Mourrain, M.J. Bouzid, and G. Ghibaudo*, CNET Grenoble and *LPCS ENSERG, France

4:00pm

Optimization of Via Contact Test Structure for Electro-Migration

S. Yamamoto, J. Komori, Y. Takata, M. Sekine, and H. Koyama, Mitsubishi Electric Corporation, Japan

4:20pm

A Compact Monitoring Circuit for Real-Time On-Chip Diagnosis of Hot-Carrier Induced Degradation

H. Oner, B. Bayrakci, and Y. Leblebici*, Istanbul Technical University, Turkey, and *Swiss Federal Institute of Technology, Switzerland

4:40pm

Equipment Presentation

5:30pm

RECEPTION

Wednesday, March 19, 1997

7:00am

CONTINENTAL BREAKFAST

7:30am

REGISTRATION

9:00am

ICMTS '98, Kanazawa, Japan Overview - Takashi Ohzone

SESSION 5 INTERCONNECTS AND CAPACITANCE

Co-Chairs: Yoshiaki Hagiwara, Sony Corporation, Japan and Michael Cresswell, National Institute of Standards & Technology, USA

9:10am

An On-Chip, Interconnect Capacitance Characterization Method with Sub-Femto-Farad Resolution
J.C. Chen, D. Sylvester, B. McGaughy, C. Hu, H. Aoki*, S. Nakagawa*, and S-Y. Oh, University of California Berkeley and *Hewlett-Packard Laboratories, USA

9:30am

A New Test Structure for Interconnect Capacitance Monitoring
P. Nouet and A. Toulouse, LIRMM, France

9:50am

Electrical Assessment of Planarisation for CMP and SOG Technologies
J.P. Elliott, M. Fallon*, A.J. Walton, J.T.M. Stevenson, A. O'Hara, M. Redford, A. Shaffi*, University of Edinburgh and *National Semiconductor, UK

10:10am

Measurement and Characterization of Multi-Layered Interconnect Capacitances for Deep-Submicron VLSI Technology D.H. Cho, M.H. Seung, N.H. Kim, and H.S. Park, Hyundai Electronics Industries Co., Korea

10:30am

Error Correction for Finite Semiconductor Resistivity in Kelvin Test Structures
A.S. Holland, G.K. Reeves and H.B. Harrison*, Royal Melbourne Institute of Technology and *Griffith University, Australia

10:50am

BREAK

SESSION 6 DIELECTRIC CHARACTERIZATION

Co-Chairs: Dieter Schroeder, Arizona State University, USA and Martin Buehler, Jet Propulsion Laboratory, USA

11:20am

GIDL-Induced Charge Injection for Characterization of Plasma Edge Damage in CMOS Devices
T. Brozek, A. Sridharan, J. Werking*, S.R. Andersen*, Y.D. Chan*, and C.R. Viswanathan, University of California at Los Angeles, and *SEMATECH, USA

11:40am

On the Oxide Thickness Extraction in Deep-Submicron Technologies
E. Vincent, G. Ghibaudo, G. Morin, and C. Papadas, SGS-Thomson Microelectronics, France

12:00pm

Improved Method for the Extraction of Oxide Charge Density and Centroid from the Current-Voltage Characteristic Shifts in a MOS Structure After Uniform Gate Stress
R. Kies, G. Ghibaudo, G. Pananakakis, and C. Papadas*, URA CNRS, ENSERG, and *SGS-Thomson Microelectronics, France

12:20pm

An Integrated Test Circuit to Measure Polarization Characteristics of Ferroelectric Capacitors for Development of Mega-Bit Class FeRAM
M. Takeo, M. Azuma*, T. Sumi, and K. Tatsuuma, Matsushita Electronics Corporation and *Kyoto Research Laboratory, Japan

12:40pm

AWARDS LUNCHEON

SESSION 7: POSTERS

Co-Chairs: Anthony Walton, University of Edinburgh, UK and Takashi Ohzone, Toyama Prefectural University, Japan

2:40pm

Holographic Test Structures for the Measurement of Linewidth and its Statistical Variation
S. AbuGhazaleh, J.T.M. Stevenson*, P. Christie, and A.J. Walton*, University of Delaware, USA and *University of Edinburgh, UK

2:45pm

A New Technique and a Test Structure for Evaluating Vth Distribution of Flash Memory Cells
K. Hakozaki, S-I. Sato, K. Iguchi, and K. Sakiyama, SHARP Corporation, Japan

2:50pm

Performance Evaluation of CMOS Ring-Oscillators with Source/Drain Regions Fabricated by Asymmetric/Symmetric Ion-Implantation
T. Ohzone, T. Miyakawa, T. Matsuda, T. Yabu*, and S. Odanaka*, Toyama Prefectural University and *Matsushita Electric Industry Co., Ltd., Japan

2:55pm

A Statistical Method for the Analysis of CMOS Process Fluctuations on Dynamic Performance
M. DeAlmeida, X. Regnier, M. Data*, M. Robert*, and M. Auvergne*, AEROSPATIALE, Louis Bleriot Joint Research Center, and *LIRMM, UMR CNRS, France

3:00pm

Design and Characterization of SiGe TFT Devices and Process using Stanford's Test Chip Design Environment
M.V.Kumar, V. Subramanian, K. Saraswat, J.D. Plummer, and W. Lukaszek, Center for Integrated Systems, Stanford University, USA

3:05pm

Issues on Short Circuits in Large On-Chip Power MOS-Transistors Using a Modified Checkerboard Test Structure
C. Hess, L.H. Weiland, and R. Bornefeld*, University of Karlsruhe and *ELMOS, Germany

3:10pm

Test Structures for Characterising a Damascene CMP Interconnect Process
A. O'Hara, A.J. Walton, M. Fallon*, J.T.M. Stevenson, J.P. Elliott, and C.M. Peyne, University of Edinburgh and *National Semiconductor, UK

3:15pm

Monitoring of Subquartermicron Polysilicon Line Patterns by Ellipsometry
H. Arimoto, Fujitsu Laboratories Ltd., Japan

3:20pm

Test Structure for Electrical Measurement of Emitter-Base Misalignment
M. Fallon, M. Redford, K. Findlater*, and M. Newsam*, National Semiconductor and *University of Edinburgh, UK

3:25pm

Test Chip and Data Considerations for MOS Parameter Extraction
P.R. Karlsson and K.O. Jeppson, Chalmers University of Technology, Sweden

3:30pm

Test Structure and Methodology for Experimental Extraction of Threshold Voltage Shifts due to Quantum Mechanical Effects in MOS Inversion Layers
G. Chindalore, S.A. Hareland, A-F. Tasch, V. Chia*, and S. Smith, The University of Texas at Austin and *Charles Evans and Associates, USA

3:35pm

Characterisation of the Threshold Voltage Variation: A Test Chip and the Results
M. Niewczas, Warsaw University of Technology, Poland

3:40pm

Automated Optical Extraction from Line Arrays of the Alignment between Microelectronic and Micromechanic Layers
U. Lieneweg, Jet Propulsion Laboratory, USA

3:45pm
Test Structure for Mismatch Characterization of MOS Transistors
M. Conti, S. Orcioni, G. Soncini*, and C. Turchetti, University of Ancona and *University of Trento, Italy

3:50pm
Poster Presentation

6:00pm
BANQUET

Thursday, March 20, 1997

7:00am
CONTINENTAL BREAKFAST

7:30am
REGISTRATION

SESSION 8 PARAMETER EXTRACTION AND MATCHING

Co-Chairs: Lawrence Bair, Digital Equipment Corporation, USA and Gerard Ghibaudo, LPCS/ENSERG, France

9:00am
Test Structures for Investigation of Metal Coverage Effects on MOSFET Matching
H. Tuinhout and M. Vertregt, Philips Research, The Netherlands

9:20am
Evaluation of hFE fluctuation of High-Performance IDP Emitter Transistors by Using Test Structures
Y. Tamaki, T. Hashimoto, K. Watanabe, and T. Shiba, Hitachi Ltd., Japan

9:40am
New Approach for the Extraction of Gate Voltage Dependent Series Resistance and Channel Length Reduction in CMOS Transistors
H. Brut, A. Juge, and G. Ghibaudo*, SGS-Thomson Microelectronics and *LPCS/URA CNRS-ENSERG, France

10:00am
A DC Voltage Capacitance Matching Tester
B.W. McNeill and C. Hanle, Lucent Technologies, Bell Labs, USA

10:20am
Separation of Intrinsic and Parasitic MOSFET Parameters Using a Multiple Built-In Kelvin Test Structure
N. Kasai, H. Mori, T. Matsuki, I. Yamamoto, and K. Koyama, NEC Corporation, Japan

10:40am
BREAK

SESSION 9 SENSORS AND MICROMACHINING

Co-Chairs: Giovanni Soncini, University of Trento/IRST, Italy and Alfred Papp, Siemens AG, Germany

11:10am

Test Structures to Measure the Heat Capacity of CMOS IC Sandwiches
M. von Arx, O. Paul, and H. Baltes, ETH Zurich, Switzerland

11:30am

Study of "On-chip" Measurement Methods of Thin Film Mechanical Properties for Micromachining
Q. Zou, Z.Li, and L. Liu, Tsinghua University, P.R. China

11:50am

Test Structures Applied to the Rapid Prototyping of Sensors
M. Buehler, L-J. Cheng, and D. Martin*, Jet Propulsion Laboratory and *Halcyon Microelectronics, USA

12:10pm

Test Structures for the Evaluation of Air-Bridge Interconnection in GaAs IC's Fabrication Process
M. Nakanishi, M. Noda, H. Nakano, T. Sonoda, and M. Otsubo, Mitsubishi Electric Corporation, Japan

12:30pm

END OF CONFERENCE

1:30pm

Tour of Monterey/Carmel

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