ICMTS 1996 INTERNATIONAL CONFERENCE ON MICROELECTRONICS TEST STRUCTURES

For information please refer to:

ICMTS '96 Secretariat Maddalena Bassetti, IRST- Microsensors and System Integration Division Povo 38100 Trento - Italy Phone: +39-461-314548/Fax: +39-461-314591/ e-mail:bassetti@ irst.itc.it

---

TUTORIAL AND TECHNICAL PROGRAM

CONTENTS

- Conference Committee
- Technical Program Committee
- ICMTS Steering Committee

ICMTS 1996 CHAIRMAN'S WELCOME LETTER

On behalf of all the Committee Members I welcome you to the 1996 International Conference on Microelectronics Test Structures ICMTS 1996 in Trento, Italy.

The Conference is sponsored by the IEEE Electron Devices Society in cooperation with the local University and ITC, the Istituto Trentino di Cultura, and brings together designers and users of test structures from all over the world to discuss recent developments and future directions. The Conference covers a broad spectrum of test structures related activities from process and materials characterisation to production monitoring and data analysis. The focus will continue to be on advanced ICs on Si and III-V semiconductors, but also emerging new technologies and devices including physical/chemical sensors and micromachined devices will be covered. The technical program consists of 58 papers including 21 Posters, the details of which are to be found in this program booklet.

Preceding the Conference on March 25 a full day Tutorial provides educational sessions presented by leading Lecturers from major Industries or Universities with acknowledged experience in the field. The Tutorial is intended to provide the non-expert with a critical overview on the fundamentals associated with the efficient design and use of microelectronics test structures A small but highly qualified equipment exhibition is planned in conjunction with the Conference. This complements the technical programme giving the attendees an opportunity to see the operation of both hardware and software which is related to the subject matter covered by the Conference. Along with the technical program, social events are planned to help expand on the personal friendship that has been the trademark of the Conference.

Situated on the river Adige and surrounded by majestic mountains in the alpine region near the Austrian border, the town of Trento lies between several valleys at the point where the roads from lake Garda, Verona and Venice cross those to the nearby Dolomites and the Brenner pass. The Centro Congressi at Grand Hotel Trento which hosts the ICMTS 1996 Conference is located in the city center at a short walking distance from the Railway Station and the medieval area, where churches and other historical monuments are to be found together with elegant shops and traditional restaurants. Thus participants will have opportunities to get out and about on relaxing walks through winding streets and beautiful piazzas.

I surely believe that the ICMTS 1996 will be a professionally rewarding as well as an enjoyable experience and I look forward to your active participation.

Yours sincerely

Giovanni Soncini

General Chairman ICMTS 1996

GENERAL INFORMATION

Conference Information

The IEEE Electron Devices Society is sponsoring the 1996 International Conference on Microelectronics Test Structures ICMTS 1996 to be held in cooperation with the Istituto Trentino di Cultura and the University of Trento. The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The Conference will be preceded by a one-day Tutorial Short Course on Microelectronics Test Structures.

Presentation

The official language of the Conference is English and it will be used for all presentations, printed materials, slides and OHP transparencies. An overhead projector and a 35mm slide projector for 50mm x 50mm mount will be available for use at the presentation. The ICMTS 1996 will reserve a Speaker's Preparation Room for speakers to arrange their slides in the carousels and preview them.

Best Paper Award

One paper will be selected for the ICMTS 1996 Best Paper Award. Presentation of the award will be made at the ICMTS 1997.

Conference Proceedings

The IEEE ICMTS 1996 will publish a proceedings. One copy of the proceedings is included in the registration fee. Additional copies will be available at the Conference for 100.000 Italian lire per copy for Members of the IEEE, 120.000 per copy for non-Members, or from the IEEE after the conference.

On-site Registration Schedule

On-site registration for the conference will be conducted in the Lobby at the Grand Hotel Trento as follows:

Sunday	March 24 5:00 pm - 8:00 pm
Monday	March 25 8:30 am - 5:00 pm
Tuesday	March 26 8:30 am - 5:00 pm
Wednesday	March 27 8:30 am - 5:00 pm
Thursday	March 28 8:30 am - 12:00 pm

Conference Registration Fees

A Registration Form is included in the center of this booklet. Below are the Conference Fees for early, late, and on-site Registrants:

Early Registration (postmarked before February 10, 1996)

	IEEE-Member	Non-Member	Students(*)
Tutorial	200.000 it. lire	250.000 it. lire	100.000 it. lire
Technical sessions	500.000 it.lire	600.000 it. lire	300.000 it. lire

Late Registration (postmarked after February 10, 1996)

	IEEE-Member	Non-Member	Students(*)
Tutorial	250.000 it. lire	300.000 it. lire	150.000 it. lire
Technical sessions	600.000 it.lire	700.000 it. lire	400.000 it. lire

On-site Registration (registration at the Conference)

	IEEE-Member	Non-Member	Students(*)
Tutorial	300.000 it. lire	350.000 it. lire	200.000 it. lire
Technical sessions	650.000 it.lire	750.000 it. lire	450.000 it. lire

(*) to qualify for reduced students rates, you must be an IEEE- Member full-time student, and not be employed part or full time

Registration fees include admittance to technical sessions, equipment exhibition, morning and afternoon coffee breaks, Conference welcome cocktail and banquet, one copy of the Conference Proceedings.

Payment of the Registration Fees

Registration Fees should be made payable to the ICMTS 1996 and must be in Italian lire only. Advanced payments are to be made as follows:

- Bank Transfer in Italian lire to: CARITRO, Cassa di Risparmio di Trento e Rovereto, Sede diTrento, Via Galilei no. 1, 38100 Trento (Italy) Account No. 6190/TES (Istituto Trentino di Cultura) Caritro Bank swift code...CRTNIT 2T...
- Bank Check in Italian lire payable to the order of Istituto Trentino Cultura(IEEE-ICMTS 1996). Personal Checks are not acceptable.
- Cash in Italian lire at the Conference Registration Desk only.

PLEASE NOTE:CREDIT CARDS WILL NOT BE ACCEPTED FOR CONFERENCE REGISTRATION FEES.

Cancellation and Refunds

Due to advanced financial commitments, refunds of registration fees requested after March 1, 1996 cannot be guaranteed. A 50.000 it.lire processing fee will be withheld from all refunds. Request for refunds of registrations cancelled after March 1st will be considered after the Conference

Messages

If you need to be contacted during the Conference, please refer to the Reception of Grand Hotel Trento: phone: 0461-271 000 national ++39-461-271 000 international fax : 0461-271 001 national ++39-461-271 001 international

Messages to the ICMTS 1996 attendees will be placed on the ICMTS 1996 Message Board in the Lobby

Welcome Cocktail

A Welcome Cocktail will be organised at the Palazzo Geremia, Via Belenzani in the historical town center, on Monday 25th at 6 p.m. All the Tutorial and Conference Attendees are cordially invited.

Conference Banquet

The Conference Banquet will be held at Grand Hotel Trento on Wednesday evening March 27th at 8.30 p.m. Conference Registration Fee includes one Banquet ticket. Guest Banquet tickets will be available for sale at the Conference Registration Desk - Reservation Banquet cut-off time is Wednesday March 27th at 12,00 a.m.

ICMTS 1995 Best Paper Award

The ICMTS 1995 Best Paper Award will be presented at the Tuesday March 26th lunch.

Information on Trento

Trento (100.000 inhabitants) is situated 190 m. above the sea level on the flat ground of the Adige river Valley on the Verona-Brennero-Munich motorway and railway. It is dominated by the nearby Mounts Bondone (2.170 m.) and Paganella (2.125 m.). It was a Roman town of some importance (Tridentum) and after Goth, Lombard and Carolingian rule it passed in year 1027 from Emperor Conrad the Salic to the Bishop Princes. Though established as a satellite state of the Germanic Empire, it always had a certain independence. The "Council of Trento" was held here from the year 1545 to year 1563 by the Catholic Church in a attempt to curb the rapid progress of Martin Luther's Reformation. The Bishop Princes rule lasted until year 1801 when, following the Luneville treaty, Trento joined the Austrian Hapsburg empire, of which it remained part until1918, i.e. at the end of the First World War, when it became part of Italy. Monuments include the Duomo, built in 12th-13th Century and seat of the "Council of Trento", and the Castello del Buon Consiglio, an imposing building dating to various periods (original nucleus 13th Century) seat of the Bishop Princes. The Centro Congressi at Grand Hotel Trento which hosts the ICMTS 1996 Conference is located in the city center at a short walking distance from the Railway Station and the medieval area, where churches and other historical monuments are to be found together with elegant shops and traditional restaurants. Thus participants will have opportunities to get out and about on relaxing walks through winding streets and beautiful piazzas. Pictures of Trento are available.

Climate and Clothing

The temperature in Trento during the Conference period will range between 8o C at night to 18o C during the day. The weather is, however, often unpredictable during this season. A sweater and a light coat is recommended.

Transportation

Trento is located in the North Italy Alpine Region, on the freeway/railway that connects Verona to Innsbruck and Munich. Verona is the nearest airport. It is connected by daily flights with London, Paris and Frankfurt. Milano International Airport or Venezia Airport are alternative possibilities. Buses connect Airports directly to Verona, Milano, Venezia (Mestre) Railway Station at very reasonable cost (much less than Taxi). Frequent

trains connect Milano or Venezia to Verona, where normally you have to change train to proceed to Trento. Please note that train tickets can be purchased directly at the railway station and must be stamped with the yellow machines available at the platform (binario) entrance before getting on the train. In buying your ticket you should notify the arrival station (Trento), the train you are planning to take (some InterCity trains require a supplement that is more expensive if purchased on the train) and the class: 1st(prima) or 2nd (seconda). First class is more comfortable and about 50% more expensive. An alternative possibility is to fly to Munchen International Airport and to proceed to Trento by train. The following trains are recommended:

Munchen Hauptbanhof	Trento
7:30 a.m.	12:00 a.m.
9:30 a.m.	2:00 p.m.
11:30 a.m.	4:00 p.m.
1:30 p.m.	6:00 p.m.
3:30 p.m.	8:00 p.m.

For any further information please refer your Travel Agent or to ICMTS 1996 Secretariat.

Hotel Accommodation

Hotel accommodations will be handled directly by: Grand Hotel Trento, Via Alfieri no. 1, 38100 Trento phone: 0461-271 000 national ++39-461-271 000 international fax; 0461-271 001 national ++39-461-271 001international

Please contact the Hotel directly for reservation Please enclose one night's room deposit or complete credit card information to secure your room reservation. The deposit will be deducted when setting the bill with the Hotel. Deposits are refundable if reservation is cancelled 5 days in advance of arrival date.

Equipment Exhibition

An equipment exhibition will be organised during the Conference to display equipments and software products, closely paralleling the nature of this meeting. The equipment exhibition will permit one-to-one discussions between Exhibitors and conference Attendees. Exhibit will be open as follows:

Tuesday	March 26th 2:00 p.m. - 7:00 p.m.
Wednesday	March 27th 9:00 a.m. - 7:00 p.m.

The exhibitors list will be made available to all Attendees at the Conference. Exhibitors representing highly qualified Companies will be selected.

ICMTS 1996 TUTORIAL SHORT COURSE

"An Introduction to the Design, Measurements and Analysis of Microelectronic Test Structures" Dr. Martin G. Buehler, Jet Propulsion Laboratory, USA

The ICMTS Tutorial is one-day short course that is intended to provide the non-expert with the fundamentals associated with microelectronics test structures. The course strives to provide good design, test, and analysis

guidelines so that superior test-structure practice will be followed, thus paying the way for improved process control and higher yield microelectronic products. The course instructors chosen by Dr. Buehler for this year's tutorial have many years of experience in the field of test structures. The format will be interactive with emphasis on the practical use of microelectronic test structures.

TUTORIAL SCHEDULE

The ICMTS 1996 tutorial Short Course will be held at IRST (Istituto per la Ricerca Scientifica e Tecnologica) in Povo,Trento. Busses will leave Monday March 25th at 8:30 a.m. in front of the Grand Hotel Trento to transfer Tutorial Attendees to IRST. At the end of the Tutorial buses will be provided to transfer Attendees to the ICMTS 1996 Welcome Cocktail to be organised at 6 p.m. c/o Palazzo Geremia, Via Belenzani in Trento historical center.

	Sunday March 24, 1996
5:00 p.m. to 8:00 p.m.	REGISTRATION c/o Grand Hotel Trento
	Monday March 25, 1996
8:00 am. to 9:00 a.m.	REGISTRATION c/o Grand Hotel and IRST
9:00 am	WELCOME
	Giorgio Musso, IRST Director
9:05 am	1. INTRODUCTION -Fundamentals
	Martin Buehler, JPL
9:45 am	2.ALIGNMENT- Overlay and Registration
	Loren Linholm, NIST
10:30 am	COFFEE BREAK
11:00 am	3. RELIABILITY - Electromigration
	Fausto Fantini, University of Parma
11:45 am	4. WLR - Wafer-Level Reliability
	Eric Snyder, Sandia National Labs
12:30 pm	HOSTED LUNCH
1:45 pm	5. TRANSISTORS-MOSFETs Parameter Extraction
	Bruno Ricco, University of Bologna
2:30 pm	6.FEMTO -Low Current Measurement Techniques
	Satoshi Habu, Hewlett Packard Japan
3:15 pm	COFFEE BREAK
3:45 pm	7. YIELD - Worst-Case Simulation
	Rory Clancy, NMRC
4:30 pm	8. DATA - Database Design
	Paul Vandeloo, IMEC
5:15 pm	WRAP-UP AND CONCLUSIONS
	Martin Buehler, JPL
5:30 pm	HOSTED RECEPTION:
	bus transport to ICMTS 1996 Welcome Cocktail

TUTORIAL OUTLINE

1. INTRODUCTION - Fundamentals: Martin Buehler, JPL

- Tutorial Overview.
- Probe pad design.
- The 2xn probe pad array.
- Four-terminal Kelvin measurement techniques.
- Bridge and cross resistors for sheet and linewidth measurements.
- Design curves for linewidth measurements.
- Three-terminal capacitance measurements.
- Matrixed test structures.

2. OVERLAY,Overlay, Registration, Feature Placement: Loren Linholm, NIST

- Introduction and Industrial Requirements.
- Optical Structures:
- Box-in-box, Frame-in-frame, Bar-in-bar.
- Electrical Structures: Differential, vdP, Sliding Wire, MOATS. Null Detection.
- Metrology Comparison: Electrical to Optical to Line Scale Interferometer.
- New Techniques: Vertical Sidewall, Scanning Probe.

3. RELIABILITY - Electromigration: Fausto Fantini, Univ. of Parma

- Electromigration physics.
- Physics of atomic motion in metals.
- Stress factors: Temp., current, mech., geom., materials.
- Models and simulation.
- Electromigration tests.
- Destructive and non-destructive techniques.
- Accelerated tests in packages or at wafer level.
- Data analysis failure distribution - The MTF test.
- Resistometric and noise techniques.
- Highly accelerated techniques (BEM, SWEAT).
- Electromigration test patterns - The reproducibility problem.
- Test structures for stripes, vias and contacts.

4. WLR - Wafer-Level Reliability:Eric Snyder, Sandia National Labs

- Introduction and Motivation
- Importance of IC reliability.
- Advantages of physics-based reliability approach
- Reliability benchmarking
- Fast electromigration measurements
- Wafer-level versus package-level.
- Frequency corelation (DC to 500 Mhz)
- Quantitative parameter extraction
- High frequency test structure design
- Hot Carrier Degradation
- Physical damage mechanisms in nMOS and pMOS
- Test Strategies: IV versus charge pumping

- Statistical variations
- Test structure for DC and AC tests

5. TRANSISTORS - MOSFET Parameter Extr.: Bruno Ricco, Univ. of Bologna

- Extraction of parasitic resistances from I-V characteristics.
- Review of existing methods.
- Extracted resistances versus effective channel length.
- Limitation in the use of arrays of scaled transistors.
- Effects of hot-carrier degradation on parameter values.
- Extraction of parasitic capacitances.
- Review of existing methods.
- Contribution of (gate) polysilicon depletion.
- Effects of hot carrier degradation.

6. FEMTO - Femto Measurement Techn.: Satoshi Habu, Hewlett Packard

- Guarding techniques.
- Correct probe-box design.
- Low-leakage wafer-level current measurements.
- Stray capacitance elimination techniques.
- Electrostatic interference elimination.

7. YIELD - Worst-Case Simulation: Rory Clancy, NMRC

- Overview of Statistical Worst-Case Simulation.
- Process fluctuations characterisation.
- Methodologies which predict circuit performance spreads.
- Requirements for Statistical Worst-Case Simulation.
- MOS model requirements and parameter extraction.
- Data acquisition and analysis.
- Statistical Analysis.
- Principal Component Analysis (PCA)and Varimax Rotation.
- Reduction of large databases to a few parameters.
- Parameters can be described by linear expressions.
- Worst-Case Design.
- +/- 3 Sigma Design.
- High/low current design and high/low factor design.
- Conclusions.
- Realistic prediction of statistical circuit performance.
- Robust worst-case simulation technique.

8. DATA - Database Design: Paul Vandeloo, IMEC

- Databases: overview of different types of databases.
- Relational database structure.
- Entities & relations - S/W methodologies & database design.
- Application development with 4GL's (4th Generation Languages).
- Data warehouses : data becomes information.
- Object databases: the future ???

TUTORIAL INSTRUCTORS

1. Martin Buehler: INTRODUCTION

Martin Buehler received the BSEE and MS in Electrical Engineering from Duke University in 1961 and 1963, respectively and the Ph.D degree in Electrical Engineering from Stanford University in 1966. Martin spent six years at Texas Instruments, eight years at the National Bureau of Standards and in 1981 joined the Jet Propulsion Laboratory (JPL). At JPL he is a Senior Research Scientist in the Microdevices Laboratory where he developed numerous test structures for integrated circuit reliability and process control. He is currently engaged in the development of radiation detectors, pressure sensors, and gas sensors. Martin is a member of the IEEE Electron Devices Society, the Nuclear and Plasma Society, and is co-founder of the International Conference on Microelectronic Test Structures.

2. Loren Linholm: OVERLAY

Loren Linholm received the B.S. in Electrical Engineering from the University of California, Berkeley in 1968 and the M.S. In Electrical Engineering from the University of Maryland, College Park in 1973. Loren has been employed by the Naval Missile Center, Point Mugu, CA, the Department of Defence, Ft. Meade, MD, and since 1978, by the Semiconductor Electronics Division at the National Institute of Standards and Technology, Gaithersburg, MD. Loren currently heads the Integrated Circuits Technology Group which is responsible for designing, developing, and evaluating measurement methods for silicon integrated circuits with emphasis on test structures, associated data analysis techniques, novel sensors, and advanced microelectromechanical systems. Loren is a member of the IEEE Electron Devices Society and co- founder of the International Conference on Microelectronic Test Structures.

3. Fausto Fantini: RELIABILITY

Fausto Fantini graduated in Electronic Engineering in 1971 from the University of Bologna, Bologna, Italy. In 1973 he joined Telettra S.p.A. in Vimercate where he worked on reliability of semiconductor devices. From 1987 until 1990 he has been Associate Professor of Electronics at S.S.S.U.P of Pisa. In 1990 he joined the University of Parma as Full Professor of Microelectronics. His research interests cover various aspects of semiconductor-device physics and reliability, including corrosion, electromigration and metal/semiconductor interaction, both on Silicon and compound semiconductor devices. He has published three books and over 100 papers. He organised various summer schools on reliability and the first ESREF. He is a member of IEEE, AEI and AICQ.

4 . Eric Snyder: WLR

Eric Snyder received the B.S. and M.S. Degree in Electrical Engineering from the Georgia Institute of Technology in 1985 and 1988, respectively. His work experience includes IBM and Intel and now Sandia National Laboratories where he is a senior member of the technical staff in the Electronics Quality/Reliability Center. He is co-inventor of the self- stressing reliability test-lab-on-a-chip for which received a 1994 R&D 100 award. He is the Hot Carrier chairman of JEDEC 14.2 and has received three best paper awards including the ICMTS award in 1994.

5. Bruno Ricco: TRANSISTORS

Bruno Ricco graduated in electrical engineering at the University of Bologna (Italy) in 1971 and in 1975 received a Ph. D. from the University of Cambridge (U.K.) In 1986 he became Life Member of the Wolfson College of the University of Cambridge (U.K.). In 1980 he became Full Professor of Applied Electronics at the University of Padua (Italy) and in 1983 he joined the Department of Electronics of the University of Bologna (Italy). In 1981 he was a Visiting Scholar at the University of Stanford and from 1983 to 1986 he spent two years at the IBM Thomas J. Watson Research Center (Yorktown Heights). In 1986, he was nominated European Editor of the IEEE Transaction on Electron Devices and Coordinator of Device Physics and Modelling of the CNR Program on Microelectronics. In 1995 he has received the G. Marconi Award by the Italian Association of Electrical and Electronics Engineers for his research in electronics. He has worked in the field of solid state devices and integrated circuits and has made contributions to the understanding and modelling of electron transport in polycrystalline silicon, tunnelling in heterostructures, silicon dioxide physics, hot electron effects in MOSFETs, latch-up in C-MOS structures and Monte Carlo device simulation. He is currently working also in the field of IC design, evaluation and testing. Prof. Ricco is co-author of over 200 publications and is a Senior Member of the IEEE.

6. Satoshi Habu: FEMTO

Satoshi Habu received the B.S. and M.S. degrees in Electrical Engineering from Ibaraki University in 1981 and 1983, respectively. In 1983 he joined Hewlett Packard, Japan and has been working in the R&D department to develop instruments for semiconductor parameter measurements.

7. Rory Clancy: YIELD

Rory Clancy received the BE in Electrical Engineering from University College Cork in 1990, and completed a Masters degree in Engineering Science (M.Eng.Sc) at the National Microelectronics Research Centre, Cork, Ireland in 1992. Rory joined the National Microelectronics Research Centre following the completion of his M.Eng.Sc and has worked for the last 3 years as a Device Characterisation Engineer within the Silicon Group. His areas of research work are in MOS models, model parameter extraction and statistical worst- case analysis techniques for CMOS technology.

8. Paul Vandeloo: DATA

Paul Vandeloo received the engineer degree in electrical and mechanical engineering in 1981 and his Ph.D degree in 1987 from Katholieke University Leuven, Belgium. He Ph.D thesis topic was "Modelling of the MOS Transistor for High Frequency Analog Design." In 1985, Paul joined IMEC where he is currently heading a group working in the field of electrical characterisation of submicrometer devices and parametric test. In addition, he is working on projects related to Information Management System.

ICMTS 1996 TECHNICAL PROGRAM

The technical program consists of nine Sessions of contributed papers plus the equipment exhibition. Papers that have been judged by the reviewers to be more appropriate for visual presentation will be displayed as Posters. A dedicated Poster Session will be held in which Authors will be given four minutes for oral presentation of their poster content to the general Audience. The Equipment Exhibition will immediately follows the Poster Session. All Sessions will be held in the Centro Congressi Tridentino at the Grand Hotel Trento.

TUESDAY, MARCH 26, 1996

9.00 a.m.

Opening Remarks:

- Giovanni Soncini, General Chairman
- Fabio Ferrari, Presidente Istituto Trentino di Cultura
- Kjell O. Jeppson, Technical Chairman
- Fulvio Zuelli, Rettore Universita' di Trento

SESSION I: DIMENSIONAL MEASUREMENTS

Co-Chairmen: Alfred Ipri, David Sarnoff Research Center Princeton, U.S.A,

Akella Satya, IBM Hopewell Junction, NY, U.S.A

9.20 a.m

A Test Structure for Monitoring Micro-Loading Effect of MOSFET Gate Length
Joo-Sun Choi and In-Sool Chung Hyundai Electronics Industries , Kyungki-do, Korea

The etch-rate ratio is strongly sensitive to the pattern density on the wafer surface: micro-loading effect. Etch rate data should therefore be obtained from monitoring wafers with a pattern density similar to that of product wafers. This paper presents the test structures which easily incorporate the micro-loading effect of a MOSFET gate length into electrical measurement. Experimental results also will be shown.

9.40 a.m

Hybrid Optical-Electrical Overlay Test Structure
M. W. Cresswell, R. A. Allen, L. W. Linholm, W. B. Penzes W. F. Guthrie, oJ. C. Fouere and oA. W. Gurnell National Institute of Standards and Technology Gaithersburg Maryland , USA
oBio-Rad Semiconductor, Mountain View California USA

The purpose of this work is to explore the use of electrical test structures for calibrating optical overlay instruments with respect to certain application-dependent errors. A new electrical test structure, which provides for the direct cross-comparison of overlay measurements that are made electrically with those made by optical instruments used for inspecting production wafers, has been designed and fabricated and preliminary tests have been made on a sample of these structures patterned in a single conducting film. Electrical overlay parameters extracted from a multiple step- and-repeat exposure-site measurement data-base generally match the corresponding average optical measurements to within several nanometers. This paper focuses on the analysis of electrical measurements and their comparison with the corresponding measurements made by two different optical instruments.

10.00 a.m.

Narrow Width Effects in CMOS n(p)-well Resistors
Chantal Auricchio, R. Bez and A. Grossi SGS Thomson Microelectronics, Milano, Italy

As the CMOS processes scale down till half submicron, even the use of n(p)-well resistors may become critical due to the interaction between the small geometry and the depletion width. In this work we present a model for n(p)-well resistor that takes into account the effects of temperature variation and resistor biases on narrow width structures. The model is obviously based on free parameters that become characteristics of the particular used CMOS technology and it can be implemented in advanced circuit simulators.

10.20 a.m.

Lithography Variability Tuning Using Statistical Metrology
Crid Yu and Costas J. Spanos University of California, Department of Electrical Engineering & Computer Sciences, Berkeley California, USA

The combined use of statistical error decomposition and designed experiments provides a novel metric which quantifies spatial and causal process and equipment variability. This information can be used in process design and accurate error budget generation. Data collected from a is used to demonstrate the calculation of equipment error contributions from raw electrical CD measurements. The isolated stepper CD error is used as a metric for lithography process design

10.40 a.m. - 11.10 a.m.

COFFEE BREAK

SESSION II: MATCHING

Co-Chairmen: Hans Tuinhout, Philips Research Laboratories Eindhoven - The Netherlands

Yoshiaki Hagiwara, Sony Corporation, Atsugi, JAPAN

11.10 a.m.

Matching Properties of MOS Transistors and Delay Line Chains with Self-Aligned Source/Drain Contacts
M. Bolt, E. Cantatore, M. Socha, C. Aussems and J. Solo Philips Semiconductors, Zurich, Switzerland

This work has shown for the first time that the matched parameter spreads for MOSFETs with and without self-aligned source/drain contacts are identical. From these observations it can be concluded that source/drain series resistance variations do not contribute significantly to MOS transistor mismatch. An example has been given which shows how to apply matching data to circuits. A similar circuit mismatch methodology could be used to analyse yield problems in clock systems of fast digital logic.

11.30 a.m.

Influence of Die Attachment on MOS Transistor Matching
J. Bastos, M. Steyaert, oB. Graindourze and W. Sansen Katholieke Universiteit Leuven, Department of Electrical Engineering, Heverlee Belgium oAlcatel Mietec, Belgium

A test chip is described which allows the experimental study of the influence of die residual stresses on MOS transistor matching, in a standard 0.7 um CMOS technology. The influence of eutectic die bonding on transistor matching is found to be a major degradation factor. Polymide bonded dies do not significantly affect the matching performance of MOS transistors.

11.50 a.m.

Automated Extraction of Matching Parameters for Bipolar Transistor Technologies
S. D. Connor and D. Evans G.E.C. Plessey Semiconductors, Oldham, Lancashire United Kingdom

We present here a technique for automatically producing statistical data for bias and resistor mis-match on bipolar transistor technologies by use of a nulled differential amplifier. The method has been to enable automatic wafer probe and the generation of distributions and wafer maps. The data is analysed using software from the SAS Institute and the method allows extraction of both resistor and VBE mis-match from a single circuit.

12.10 a.m.
Characterising the Mismatch of Submicron MOS Transistors
Simon J. Lovett, M. Welten, A. Mathewson and oB.Mason National Microelectronics Research Centre, University College Cork, Ireland oGEC Plessey Semiconductors, Plymouth Devon,United Kingdom

A test structure is presented to characterise submicron MOS transistor mismatch. The structure reveals the potential to improve matching by up to 300% without changing layout area. An expression is derive and verified by experiment which predicts the W/L geometry that gives optimum mismatch.

12.30 a.m.
On Matching Properties and Process factors for Submicron CMOS
oS. C. Wong, ooK. H. Pan, oooD. J. Ma, oooM. S. Liang and ooooN. Tseng
oFeng-chia University, Department of Elctronics Engineering, Taichung, Taiwan
ooNational Chiao-tung University, Institute of Electronics, Hsinchu, Taiwan
oooNational Chung-Hsing University Department of Electrical Engineering.Taichung, Taiwan
ooooTaiwan Semiconductor Manufacturing Company Hsinchu, Taiwan

We analyse the matching properties of a 0.5 um CMOS technology incorporating short channel effects. Source resistance is found to attribute significantly to short Channel mismatch. Long-spacing mismatch, due to process gradients, significantly differs from the short-spacing mismatch. Threshold mismatch varies with (WL)-0.75 due to edge roughness. A /n -law model is further developed to model the stripe-layout mismatch.

12.50 p.m.- 2.40 p.m.
LUNCH

SESSION III:INTERCONNECTS AND CAPACITANCE MEASUREMENTS

Co-Chairmen: G. Ghibaudo, URA CNRS-ENSERG, France

Michael Cresswell, NIST, USA

2.30 p.m
Test Structure to Measure the Gate-Drain Capacitor Using Accelerated Coupling Techniques
T. Manku Technical University of Nova Scotia, Halifax Canada

In this paper, we present a test structure to measure the gate-drain coupling capacitance. The test structure has been implemented within a standard CMOS process. The structure uses charge coupling as a means to measure the gate-drain capacitance. Furthermore, the test structure can measure the gate-

drain capacitance in less than 10 ms. The basic structure consists of two MOS transistors connected by their gates.

2.50 p.m.

Control of Application Specific Interconnection on Gate Arrays Using an Active Checkerboard Test Structure

C. Hess, L. H. Weiland, oG. Lau and oP. Simoneit University of Karlsruhe, Institute of Computer Design and Fault Tolerance, Karlsruhe, Germany
oThesys Gesellschaft Fur Mikroelektronik, Erfurt Germany

To control interconnection layers' integrity on application specific gate arrays, a novel active checkerboard test structure (ACTS) is presented. Here, the total gate array area will be divided into distinguishable small subchips, each containing basic layout elements like different sized serpentine lines or via strings. The precise separation and localisation of these test structure elements inside the subchips facilitate versatile classification of interconnection faults, additional defect parameter extraction, and defect statistics.

3.10 p.m.

A Test Chip for Interconnect Capacitance Modelling in a CMOS Process

P. Nouet and A. Toulouse University of Montpellier, Montpellier, France

Based on our previous works on On-Chip measurement of small capacitances, we present a Test Chip designed to provide experimental data for the modelling of interconnect capacitances. Patterns include line to line capacitance (for the two metal layers and the polysilicon layer), inter-layer capacitance (extraction of area and perimeter related capacitance for each couple of layer), matching (relative scattering between two similar capacitances), cross-over (capacitance between two crossing lines) and other parameters generally used when extracting parasitic from a design.

3.30 p.m.

Universal surfaces for the accurate contact resistivity extraction on Kelvin structures with upper and lower resistive layers

J. Santander, M. Lozano, A. Gotz, C. Cane and E. Lora-Tamayo Centro National de Microelectronica, Barcelona, Spain

An accurate procedure to extract contact resistivity from contact resistance measurements made on D-resistor-type Kelvin cross test structures with both upper and lower resistive layers. The method is based on the obtention of "Universal Surfaces" through computer simulation. Using adimensional variables these surfaces can be employed in all experimental conditions, eliminating the need of further simulations.

3.50 p.m. - 4.20 p.m.

COFFEE BREAK

SESSION IV:MATERIALS AND DEVICES CHARACTERISATION

Co-Chairmen: Emilio Lora-Tamayo, Centro National de Microelectronica, Universidad Autonoma de Barcelona,Spain

Bruno Ricco', DEIS, University of Bologna, Italy

4.20 p.m.

A New Test Structure for the Evaluation of the Injection- Level Dependence of Carrier Mobilities
oS. Bellone and ooG. V. Persiano oUniversity of di Salerno, Department of Information and Electrical Engineering, Salerno Italy
ooUniversity of Naples, Department of Electronics, Italy

By using a new three-terminal test structure and a simple apparatus, we describe the first electrical method separately measure the injection-level dependence (and, hence, the effects of carrier-carrier scattering) of the electron and hole mobilities. Numerical simulation is used to check the accuracy of the method and carefully design the test structure. Experimental result both in n-type and in p- type silicon regions are presented and compared to major analytical models.

4.40 p.m.

An Improved Test Structure to Characterise Ultra- Low Hot Carrier Injection in Homogeneous Conditions
L. Selmi, oR. Bez and ooE. Sangiorgi
University of Bologna, Department of Electronics, Bologna, Italy
oSGS Thomson Microelectronics,Milano, Italy
oo DIEGM, University of Udine, Italy

This paper describes an improved test structure to characterise homogeneous hot-carrier injection from silicon to silicon dioxide at very low applied voltages. The device allows to separate the interface and oxide trapped charges from the total charge injected through the interface. Results on the injection probability of substrate hot electrons and holes are presented, covering an extended range of bias conditions with respect to previous reports.

5.10 p.m.

Measurement of Interface States in the LDD Region of a MOS Transistor Using a Modified Charge Pumping Technique V. Prabhakar, T. Brozek, oY. D. Chan and C. R. Viswanathan University of California, Electrical Engineering Department Los Angeles, USA
oSEMATECH, Austin, Texas, USA

In this work, an LDD NMOS transistor is used as a test structure for a modified charge pumping technique (LDD charge pumping) to directly measure the interface state density in the LDD region. The technique is validated by measurements on virgin samples and samples subjected to hot carrier stress and Fowler-Nordheim stress, which are known to cause a different degradation of the interface over the LDD region as compared to that over region the channel region. GIDL current measurements are shown to be in agreement with the charge pumping results.

5.30 p.m.

Analysis of charge storage in the base of bipolar transistors ant its influence on the parasitic base resistance adopting eight terminal Kelvin test structure
S. Asti, A. Neviani, oP. Pavan, L. Vendrame and E. Zanoni University of Padova, Department of Electronics and Informatics, taly
oUniversity of Modena, Department of Engineering Science, Italy

This paper compares two different methods previously described in literature for the extraction of the intrinsic and extrinsic base parasitic resistance based on a eight- terminal BJT Kelvin test structure and proof that the effect of charge storage in the base of silicon bipolar transistors has to be taken into

account to evaluate the parasitic base resistance correctly even at high injection levels. A new technique for extrinsic base resistance measurement has been developed and compared to previously reported extraction techniques. Differently from literature, no fitting is required and results agree with the value obtained from calculations based on the process parameters.

WEDNESDAY, MARCH 27, 1996

SESSION V: SENSORS

Co-Chairmen: Willy Sansen, Katholieke Universiteir, Leuven, Belgium

Mario Zen, IRST, Trento, Italy

9.00 a.m.

Electrical Characterisation and Reliability Studies of Thick Film Gas Sensor Structures.
oJ. Czech, oJ. Manca, ooJ. Roggen, ooG. Huyberechts, oL. Stals and oL. De Schepper oLimburgs University, Material Physics Division Diepenbeek, Belgium
oo IMEC, Leuven, Belgium

In order to produce a stable gas sensing device by screen printing technology it is important to characterise the different layers from which the gas sensor is built up. For this purpose an adequate layout has been developed, so that each layer can be characterised and also the influence of the top layer on underlaying layers can be investigated. With the help of in-situ conductance measurements as function of temperature the properties of the layers are investigated over the temperature range of the gas sensor.

9.20 a.m.

GAS Sensor Test Chip
M. G. Buehler and M. A. Ryan Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California, USA

A new test chip is being developed to characterise conducting polymers used in gas sensors. The chip, a seven layer cofired alumina substrate with gold electrodes, contains 11 comb and U-bend test structures. The structures are designed to measure the sheet resistance, conduction anisotrophy, and peripheral conduction of spin coated films that are not subsequently patterned.

9.40 a.m

Test Structure for Thermal Monitoring
V. Szekeli, Z. Kohari, Cs. Marta, M. Rencz and oB. Courtois Technical University Budapest, Department of Electronics Devices Budapest, Hungary
oTIMA LABORATORY, Grenoble, France

In this paper a new principle thermal test structure will be presented: the Thermal Feedback Oscillator (TFO). This circuit is suitable for different purposes - on-line thermal monitoring or thermal mapping of an IC - depending on the sensor arrangements. It can be realised with most of the standard CMOS processes without any additional steps. The TFO measures the absolute temperature - no need for calibration. It provides digital output signal assuring easy signal processing.

10.00 a.m.

Test Structures to Measure the Seebeck Coefficient of CMOS IC Polysilicon
M. von Arx, O. Paul and H. Baltes Physical Electronics Laboratory, ETH, Zurich Switzerland

We report a novel thermal characterisation structure to measure the Seebeck coefficient a of CMOS IC polysilicon thin films relevant for integrated thermal micro transducers. The test structure was fabricated using the commercial 2 um CMOS process of Austria Mikro Systeme AMS. In contrast with earlier devices it is fully CMOS compatible and requires no micromachining. The temperature dependent a of the two poly layers of the AMS process were measured with both new test structures and previous micromachined devices. The agreement between the two data sets validates the new structure.

10.20 a.m.
A Test Chip for ISFET/CMNOS Technology Development oA. Lui, oB. Margesin, oM. Zen, ooG. Soncini and oooS. Martinoia
oIRST ,Trento, Italy
ooUniversity of Trento, Materials Engineering Department, Italy
oooUniversity of Genova, Department of Biophysical and Electronics Engineering Italy

The design, fabrication and preliminary characterisation of a test chip aimed at the development of Ion Sensitive Field Effect Transistors coupled with CMNOS (Complementary Metal gate Nitride Oxide Silicon) circuitry is reported. By this technology inexpensive single chemical sensors or arrays and multi-sensors with on-board signal conditioning for environmental and biomedical applications are being developed. The test chip contains three sets of test structures in order to evaluate the chemical sensor performance, to extract the CMNOS process parameters (e.g. SPICE parameters) and to the test basic analogue circuit blocks to be used for the on chip interface electronics.

10.40 a.m. - 11.10 a.m.
COFFEE BREAK

SESSION VI: MOSFET PARAMETERS EXTRACTION

Co-Chairmen: Bair Lawrence, Digital Equipment Corporation, U.S.A

Martin Buehler, Jet Propulsion Laboratories, Pasadena, CA, U.S.A

11.10 a.m.
Simultaneous Determination of Threshold Voltage Mobility and Parasitic Resistance for Short-Channel MOSFETs
Y. Mita, M.Fujishima and K. Hoh University of Tokyo,Department of Information and Communication Engineering, Tokyo, Japan

A novel method of simultaneous extraction of mobility, threshold voltage, and source/drain parasitic resistances are presented. It takes parasitic resistances into account and effective on short-channel MOSFETs. In addition to the effectiveness, it is quite simple and easy method to handle because on well known multi-variable least squares method. Curves calculated by using these parameters were compared with the measures ones for PMOSFETs with channel length down to 0.25 um and the excellent agreement was obtained.

11.30 a.m.
Gate Delay Time Evaluation Structure for Deep- submicron CMOS LSIs

K. Nishimura, M. Urano, M. Ino, K. Takeya, T. Ishihara, Y. Kado and H. Inokawa NTT LSI Laboratories, Kanagawa, Japan

A new test structure for gate delay time measurement has been developed. The delay times of over several tens of gate chain circuits can be measured efficiently. This structure has common input buffers, output buffers, and a selector to avoid signal skew between each gate chain circuit. The performance of a quarter-micron SIMOX CMOS and BULK CMOS device were measured and compared with this structure.

11.50 a.m.
A New Method to Determine Effective Channel Length, Series Resistance and Threshold Voltage
M. Sasaki, H. Ito and T. Horiuchi NEC Corporation, ULSI Device Development Laboratories, Kanagawa, Japan

This paper describes a new method to determine the parameters of MOSFET having deep-submicron channel length. The model shows that threshold voltage defined by Id//gm - Vg plot is consistent with the extracted effective channel length and series resistance. The experimental data result in a good linearity for the parameter extraction down to 0.24 um transistor. Further, the model is found to be in good agreement for reproducing Id - Vg curves.

12.10 p.m.
An Efficient Parameter Extraction Methodology for the EKV MOST Model
M. Bucher, C. Lallement and C. C. Enz Swiss Federal Institute of Technology Electronics Laboratory, Lausanne, Switzerland

Based on an accurate and continuous MOST model dedicated to low-voltage and low-current analog circuit design and simulation, a new methodology is presented to obtain key parameters from the pinch-off voltage characteristic measured at constant current bias in moderate inversion. This efficient and simple method is shown to be accurate for submicron bulk CMOS as well as fully depleted SOI processes. Unique parameter sets, suitable for statistical analysis, describe device behaviour in all operating regions and over all device geometries.

12.30 p.m.
A New Method of Determining the MOSFET Effective Channel Width and Its Gate Voltage Dependence
K. O. Jeppson, A. W. Bogren and P. R. Karlsson Chalmers University of Technology, Department of Solid State Electronics, Gotenborg Sweden

This paper presents a new method for determining the gate voltage dependence of the MOSFET effective channel width. Contrary to existing methods the new method does not rely for its validity on an assumptions concerning the width dependence or the gate voltage dependence of the series resistance. This improvement has been obtained by a new technique for separating the series resistance from the channel resistance from which the channel width is extracted.

12.50 p.m. - 2.30 p.m.
LUNCH

SESSION VII: POSTERS

Co-Chairmen: Antony Walton, University of Edinburgh, Scotland, UK

Takashi Ohzone, Toyama Pref. University, Japan

2.30 p.m.

Heating due to bias in GaAs MOSFET's
J. Rodriguez Tellez and R.W. Clarke University of Bradford, Department of Electronic and Electrical Engineering, Bradford, UK

Liquid crystal are employed to measure the average temperature of GaAs MESFETs under a wide range of bias conditions. The measurements are performed to determine whether localised heat spots are formed and whether the self bias heating is the main mechanism responsible for negative output conductance.

2.34 p.m.

Spatial Contribution of Recombination Centres in Electron Irradiated Silicon Epitaxial Layers
S. Daliento, A. Sanseverino, P. Spirito and L. Zeni University of Napoli, Department of Electronics Engineering, Napoli, Italy

Taking advantage of a suitable three terminals test structure we analyse the effects of electron irradiation in silicon epitaxial layers, through the measurement of the recombination lifetime profile. Furthermore, by means of an appropriate temperature scanning we measure the energy levels of the recombination centres induced by the irradiation itself.

2.38 p.m.

Asymmetry and Mismatch in CMOSFETs with Source/Drain Regions Fabricated by Various Ion-Implantation Methods
oT. Ohzone, oT. Miyakawa, ooT. Yabu and ooS. Odanaka
oToyama Prefectural University,Department of Electronics and Informatics, Toyama, Japan
ooMatsushita Semiconductors Research Center, Osaka, Japan

Experimental results on asymmetry and mismatch characteristics are discussed for 0.5 um CMOS devices with LDD- and EPS-regions fabricated by four ion-implantation methods and designed by a conventional and a side-by-side layout. The surface channel n-MOSFETs fabricated by 7o x 4-implantation with the conventional layout, those the side-by- side layout, and n- and p- MOSFETs with 0o- and 7o- implantation are recommended for minimising asymmetry and mismatch in (ID and b), (VT and S) and IB, respectively.

2.42 p.m.

On the Impact of Spatial Parametric Variations on MOS Transistor Mismatch
H. Elzinga CNET SGS-Thomson, Crolles France

Quite often it is observed that for matched-pair MOS transistors with large device dimensions the general mismatch law "s(DP) = AP//area" (or its derivates) does not always hold. This paper demonstrates that an explanation for this effect can be found in the presence of non-random parameter distributions, over a wafer (spatial parametric variations).

2.46 p.m.

Test Structures for HF Characterisation of Fully Differential Building Blocks
E. Peeters, M. Steyaert and W. Sansen Katholieke Universiteit Leuven, Belgium

A procedure is described which allows to characterise fully differential building blocks as a linear 4-port. A new set of linear differential hybrid parameters is presented which are well sited to describe fully differential amplifiers. A measurement set-up is described which allows to determine the

differential h-parameters from measured s-parameters obtained with a 2-port test set. Measurement results of a 400 MHz fully differential amplifier are presented which demonstrate the new measurement procedure.

2.50 p.m.

Parametric Test Engineering Optimisation: Methodology and Software System
oT. Ternisien d'Ouville, oF. Mendez, oJ. Bruines ooL. Zangara and ooG. Durieu
oCNET SGS THOMSON Crolles, France
ooDolphin Integration, Meylan Cedex, France

To improve drastically the productivity and the quality of parametric test we have defined a new design methodology based on a global and concurrent approach. A CAD system has been developed allowing the automatic generation of all the parametric test tools and the secured transfer of all information about test chip to parametric tester. This CAD solution has been progressively implemented in the Centre Common CNET SGS-Thomson to design the test chip of CMOS 0.5 um, CMOS 0.35 um and BiCMOS technologies. Global indicators confirm the productivity and quality improvement of the parametric test design process.

2.54 p.m.

Direct Extraction Method of SOI MOSFET Transistors Parameters
J. P. Raskin, R. Gillon, D. Vanhoenacker and J. P. Colinge Universite Catholique de Louvain, Microwaves Laboratory, Louvain-La-Neuve Belgium

An extraction method for small signal model parameters of Silicon-on-Insulator (SOI) MOS transistors is presented. This technique allows to obtain the intrinsic and extrinsic parameter values for high frequency small-signal model directly from scattering parameter measurements.

2.58 p.m.

A Quick Address Detection of an Anomalous Memory Cell for Flash EEPROM
T. Himeno, H. Hazama, K. Sakui, K. Kanda and Y. Itoh, J. Miyamoto
Toshiba Corporation, Kawasaki , Japan

A simple technique for quickly detecting an address of an anomalous memory cell is described. A proposed Multi-Address Selection Scheme (MASS) can drastically reduce measurement cycles for searching an address of an anomalous memory cell, such as an erratic erased cell, which has an abnormally high or low threshold voltage. A systematic evaluation for a reliability of flash EEPROM has been realised by this quick address detection technology.

3.02 p.m.

Matching of MOS Transistors with Different Layout Styles
J. Bastos, M. Steyaert, oB. Graindourze and W. Sansen
Katholieke Universiteit Leuven, Department of Electrical Engineering, Heverlee, Belgium o ALCATEL Mietec, , Belgium

A test chip with NMOS transistor pairs with different layout styles is presented to study its influence on matching. Common centroid structures are found to have much better matching performance than finger style structures. They show no systematic mismatch, and have a matching dependence on the channel area which is in agreement with measurement results on simple rectangle structures. Under induced die stress due to packaging, finger style transistor pairs show a fluctuation on transistor matching up to 5 times higher than the predicted by only considering random fluctuation of the channel area.

3.06 p.m.

A Test Structure Advisor and a Coupled, Library- Based Test Structure Layout and Testing Environment

Madan V. Kumar, J.D. Plummer and W. Lukaszek Center for Integrated Systems, Stanford University, California, USA

We have developed a new test chip design environment, based on commercial tools, containing a test structure advisor and a coupled, library-based layout and testing environment that results in a tenfold increase in productivity. It recommends diagnostic test structures for new devices, which can be retrieved from a library of parameterised structures and customised to rapidly generate test chips. With this environment, we designed a new test chip, which would normally have taken over 1.5 weeks, in 6 hours.

3.10 p.m.

A Quasi-Three-Dimensional Analysis of ESD Failure Mechanism and a New ESD Structure with Rounded Drain Corner

J. H. Choi, H. S. Bong, Y. H. Koh, G. Y. Lee, H. G. Kim and H. S.Yoon
Hyundai Electronics, Korea

A new quasi-three-dimensional analysis technique to verify the ESD failure mechanism in I/O circuits and an optimised ESD structures with rounded drain corner are proposed and also verified by electrothermal simulations and experiment. The new ESD structure eliminates the current crowding at the drain corner resulting in the dramatic reduction of the peak lattice temperature by more than 20%.

3.14 p.m.

Microwave Frequency Measurements and Modelling of MOSFET's on Low Resistivity Silicon Substrates

C. Biber, T. Morf, H. Benedickter, U. Lott and W. Bachtold
Swiss Federal Institute of Technology, Zurich, Switzerland

Microwave frequency performance of silicon MOSFETs depends not only on the process but also on gate resistance and parasitic capacitances which are layout dependent. MOSFET transistors with different finger widths on a silicon epi- wafer have been measured from 50 MHz to 10 GHz. An equivalent circuit model of an optimum transistor layout for high frequency performance up to 10 GHz is presented.

3.18 p.m.

Test Structure for Investigating Activated Doping Concentrations in Polycrystalline Silicon

S. Moran, P.K. Hurley and A. Mathewson
National Microelectronics Research Centre Row Cork, Ireland

A new method for evaluating the active doping concentration in polycrystalline silicon (polysilicon) using a double polysilicon capacitor test structure is described. The technique is based upon a combination of both experimental and simulated characteristics. The results provide further insight into the effect of depletion into the polysilicon gate of MOSFETs, as well as dopant redistribution in polysilicon/silicide bilayers.

3.22 p.m.

Automatic Test Chip Documentation Synthesis

W. Nagorski, W. McGee, E. G. Piccioli and L. A. Bair
Digital Equipment Corporation, Hudson, MA USA

We describe a new test chip documentation methodology which simultaneously generates inputs for layout design and test chip documentation. On-line test chip documentation is generated based on specifications from the test structure requester/designer. This specification is used as input for both the layout designer and also for software which generates on-line test structure documentation. In addition, results from layout and circuit verification tools are compared with specifications to ensure that layout, specification, and documentation agree.

3.26 p.m.

A Test Chip for the Development of Porous Silicon Light Emitting Diodes
oL. Pavesi, oR. Guardini, oO. Bisi, ooP.L. Bellutti, ooM. Zen and oooG. Soncini
oUniversity of Trento, Italy
ooIRST - Microsensors and Systems Integration Division, Trento, Italy
oooUniversity of Trento, Materials Engineering Department, Italy

A test device to implement room temperature visible resonant cavity light emitting diodes based on porous silicon planar microcavities is reported. The device is based on a post processing anodisation of n+ stripes implanted into p-doped Si wafers.

3.30 p.m.

Radiation Detectors
oG. F. Dalla Betta, ooM. Boscardin, oG. Verzellesi, oG. U. Pignatel, +A. Fazzi and oG. Soncini
oUniversity of Trento, Materials Engineering Department, Italy;
ooIRST - Microsensors and Systems Integration Division, IRST, Trento, Italy
+Dipartimento di Ingegneria Nucleare Politecnico di Milano, Italy

PIN radiation detectors and other test-structures have been fabricated on a FZ, high-resistivity (2 kO cm), n-type silicon substrate by a planar process that features three different alternative extrinsic-gettering techniques. Results from the electrical and optical characterisation of such devices are reported and discussed. X-ray detection testing is under way.

3.34 p.m.

Electrical Determination of the Phosphorus Content in Thin Phosphosilicate Glass Films
O. Popa, C. Cobianu and D. Dascalau
Institute of Microtechnology, Bucharest, Romania

A new method for the determination of phosphorus content in thin phosphosilicate glass films (PSG) is presented. This method is based on recording the time dependence of the current flow through a thin PSG film. A discussion on the physical background of the method is provided and experimental results are presented.

3.38 p.m.

Kelvin Test Structure for Measuring Contact Resistance of Shallow Junctions
L.K. Nanver, E. J. G. Goudena and J. Slabbekoorn
Delft Institute of Microelectronics and Submicron Technology, Delft University of Technology, The Netherlands

A Kelvin contact resistance test structure has been developed for accurate and direct measurement of highly- doped, shallow n+ and p+ junctions, which may be self- aligned to the contact window. The structure is easily integrated in many IC-processes. Results are presented for high-dose arsenic implantation, where for example excimer laser annealing of the contact windows yields contact resistivities below 10-7 Ocm2.

3.42 p.m.

Test Circuit Strategies Aimed Towards Concurrent Technology and Circuit Design for an In-House 60 GHz Silicon Bipolar Technology
M. Allaskog, T. Juhola, M. Mokhtari and H. Tenhunen
Royal Institute of Technology, Kista, Sweden

The concurrent development of a novel bipolar technology and the design of a number of high speed circuits results in both faster technology introduction as well as increase in the total quality. A test circuit strategy, developed for KTH's In-House 60 GHz silicon bipolar process, is to aid such a concurrent development and will be presented in this paper.

3.46 p.m.

Numerical Analysis of the Effect of Geometry on the Performance of the Greek Cross Structure
M. I. Newsam, A. J. Walton and M. Fallon
Edinburgh Microfabrication Facility, Department of Electrical Engineering University of Edinburgh, UK

This paper examines the effect that geometry has upon the value of resistivity that is extracted from Greek cross type structures. This work suggests that structure to structure variability of the Greek cross can be reduced through the choice of the appropriate layout.

3.50

CMOS IC's Transient Radiation Effects Investigations, Models Verification and Parameter Extraction with the Test Structures Laser Simulation Tests
A. Y. Nikiforov, A. I. Chumakov and P. K. Skorobogatov
Specialised Electronic Systems, Moscow, Russia

The specialised test chip is designed and investigated for CMOS RAMs dose rate and single event upsets prediction, models verification and parameter extraction. The laser simulation methods are analysed. The original laser simulation source and experiments procedure are designed and used as an effective tool in IC' design process.

3.54 p.m. - 4.20 p.m.

COFFE BREAK

4.20 p.m. - 7.00 p.m.

Poster Session and Equipment Exhibition

8.30 p.m.

Conference Banquet at Grand Hotel Trento

THURSDAY MARCH 28, 1996

SESSION VIII: RELIABILITY

Co-Chairmen: Hakim Edward, US Army Labcom Fort Monmouth NJ - U.S.A

Fausto Fantini, University of Parma, Italy

9.00 a.m.

A New Test Structure Methodology for MOS Hot Carrier Reliability
oM. M. O.Lee and ooK. Asada
oDongshin University, Faculty of Information & Communication Engineering, Chonnam, Korea
ooUniversity of Tokyo, Department of Electronics Engineering, Japan

Source bus resistance from a test structure can not be negligible, which causes body effect. The body effect on test structure is closely related to transistor parameters for ULSI design. So the new test structure is built to minimise the body effect and extends the deep submicron MOS device lifetime. It was promising to evaluate the HCI effective lifetime and was proved to be useful to characterise MOS more accurately.

9.20 a.m.

Use of Test Structures for a Wafer-Level- Reliability Monitoring
A. Papp, F. Bieringer, D. Koch, H. Kammer, H. Pohle, A. Schlemm, M. Schneegans and H. Vogt
Siemens, Munich, Germany

A short loop to bring reliability data into the waferfab gets growing importance. Wafer-level-reliability programs on test-structures with highly accelerated stress to reach very short test-periods are necessary. A concept with a variable drop-in test chip is described. By means of two examples, gate oxide integrity and electro-migration, challenges and solutions are presented. The charge to breakdown distribution offers a way to characterise rapidly early oxide fails. The wafer-level EM-test allows lifetime predictions to remain useful.

9.40 a.m.

A Wafer Level Monitoring Method for Plasma Charging Damage Using Antenna PMOSFET Test Structure
H. Watanabe, J. Komori, K. Higashitani Y. Mashiko and H. Koyama
Mitsubishi Electric Corp.,ULSI Laboratory Japan

We propose a novel monitoring method for plasma charging damage using various antenna test structures. The method performs a quick and accurate evaluation antenna PMOSFET. It was found that initial gate current and substrate current indicates plasma damage. Furthermore the present work suggest that the monitoring shift of drain current after a few seconds of HC stress is a more accurate method to indicate plasma charging damage. The monitoring method using the present test structure is demonstrated to be useful for realising highly reliable devices.

10.00 a.m.

Observation of Light Emission from Hot Electron and Latch-up at the Cleaved Surface of CMOS Structures
T. Aoki
NTT LSI Laboratories, Kanagawa-Pref., Japan

Hot-electron-induced and latchup-induced photon emissions can be directly observed from the cleaved surface of CMOS test structures using the two-dimensional photon counting system. this observation enables an accurate photon analysis with a high spatial resolution because, unlike in conventional top surface observation, there is no masking by the aluminium electrode.

10.40

Test Patterns for Electromigration Evaluation in Submicron Technology
oS. Morgan, oI. de Munari, ooA. Scorzoni, F. Fantini, oooG. Magri, oooC. Zuccherini and oooC.

Caprile
oUniversity of Parma, Parma, Italy
ooCNR Istituto LAMEL, Bologna, Italy
oooSGS Thomson Microelectronics, Milano Italy

A new set of test structures based on the single level stripe, the multilevel Kelvin contact and via chain structures, are proposed to investigate electromigration in submicron technology devices. The new test structures overcome the problems which have previously been associated with conventional ASTM test structures. The use of multi- finger Babel Tower structure ensures that the microstructure of the end-segment is consistent with the test stripe and the use of tungsten via plugs in multilevel systems eliminates the reservoir effect. These modifications will allow the reliability of the test structures to be evaluated in a manner which is representative of actual VLSI device structures. As submicron lines are not the critical element of an IC metallisation, a number of test structures sets using different line width were designed to enable a comparison to be made between bamboo and multigrain structures.

10.40 a.m. - 11.00 a.m.
COFFEE BREAK

SESSION IX: PROCESSING

Co-Chairmen: Robert Ashton, AT & T Bell Laboratories Orlando, Florida, USA

Alfred Papp, SIEMENS, Munchen, GERMANY

11.10 a.m.
A New Approach to Determine Active Doping Profiles of Bipolar Transistors Using Electrical Measurements and a Physical Device Simulator
J. Hachicha, P. Fouillat, T. Zimmer and J.P. Dom
University of Bordeaux, France

This paper describes a new methodology to extract active profiles in a bipolar technological process. It consists in running minimisation techniques between electrical measurements and computed simulations with a device simulator on a bipolar transistor. The influence of doping profile models, physical and statistical models and how to drive convenient experiments on the device under test is discussed.

11.30 a.m.
Optimum Test Structure Design for CMOS Parasitic Transistor Characterisation
G. J. Gaston and P. Myler
GEC Plessey Semiconductors, Plymouth Devon, UK

This paper details the optimum test structures required to properly established field transistor characteristics. The structures are used to assess leakage due to punch through and also poor isolation as a result of low field threshold voltages. Particular emphasis is placed on the gated structures, with different gate polysilicon layout being investigated. Also described is how the magnitude of the different current components can be used to predict the leakage mechanism as part of an automated test.

11.50 a.m.
A Test Structure for the Measurement of Planarisation

J. P. Elliott, M. Fallon, A. J. Walton, J.T.M. Stevenson and A. O'Hara
University of Edinburgh, Department of Electrical Engineering, Scotland, UK

A test structure for the electrical measurement of planarisation is described. Planarisation is becoming increasingly important as IC interconnect density and the use of multilayer metal increase. The test circuit comprises 16 sets of 2 identical combs, one each in metal 1 and metal 2, with the upper comb being progressively offset from the lower one. Simulation results show that a graph of capacitance between the combs vs the amount of offset of the combs ca be used to determine the degree of planarisation of the inter-metal dielectric.

12.10 p.m.
An Electrical Test Structure to Evaluate Substrate Compatibility with Wafer Cleaning
oC. M. Peyne, M. Fallon, J.T.M. Stevenson, A. J. Walton
Department of Electrical Engineering, University of Edinburgh, Scotland, UK
oEKC Technology Ltd, East Kilbride, Scotland

Every new wet chemical process requires evaluation to assess its compatibility wit the wafer substrates. A novel application of the standard Greek cross used in conjunction with an electrical line width test structure allows vertical and lateral etch rates to be determined. A new test structure is presented to allow in situ real-time measurements to be made. Preliminary results using the Greek cross and line width structures are presented.

12.30 p.m.
Test Structures for Automated Contactless Inline Wafer Inspection
A. V.S. Satya
IBM Microelectronics, Hopewell Junction, NY USA

Unique microelectronics test structures were designed to enable automated rapid inline contactless wafer inspection in a Scanning Electron Microscope Voltage-Contrast (SEM-VC) mode, for routine defect-monitoring, and in situ defect- isolation and characterisation. Such an automated technique can support accelerated yield learning on sub-0.5 um-rule designs as the defects get below the optical resolutions.

12.50 p.m.
Nomination of ICMTS 1996 Best Paper and Closing of the Conference
K. O. Jeppson, ICMTS 1996 Technical Chairman
G. Soncini , ICMTS 1996 General Chairman

ICMTS 1996 CONFERENCE COMMITTEE

General Chairman: Giovanni Soncini,

Univ. of Trento and IRST-Istituto

per laRicerca Scientifica e Tecnologica, 38050 Povo (Trento) - Italy

Phone: +39-461-314537/Fax: +39-461-314591/

e-mail:soncini@irst.itc.it

Technical Chairman: Kjell O. Jeppson,

Chalmers University of Technology

Dept. of Solid St. Electronics, S.412 96 Goeteborg - Sweden

Phone: +46-31-7721856/Fax: +46-31-7723622/

e-mail:kjellj@ic.chalmers.se

Publication Chairman: Mario Zen,

IRST-Istituto per la Ricerca Scientifica e Tecnologica, 38050 Povo (Trento) - Italy

Phone: +39-461-314546/Fax: +39-461-314591/

e-mail:zen@irst.itc.it

European Representative: Anthony J. Walton, EE Dept.,

University of Edinburgh, Kings Bldg., Edinburgh, EH9 3JL, UK

Phone: +44-131-650-5620/Fax: +44-131-650-6554

e-mail: ajw@ee.ed.ac.uk

USA Representative: Loren W. Linholm,

National Institute of Standards & Technology, B-360 Tech. Bldg., Gaithersburg, MD 20899, USA

Phone: +1-301-975-2052/Fax: +1-301-948-4081

e-mail: linholm@apollo.eeel.nist.gov

Asian Representative: Takashi Ohzone,

Toyama Prefectural University, Kurokawa, kosugi-Machi, Imizu-Gun, Toyama 939-03, Japan

Phone: +81-776-56-7500 Ext.501/Fax: +81-766-56-6172

e-mail: ohzone@tpusv.pu-toyama.ac.jp

Tutorial Chairman: Martin Buehler, Jet Propulsion Laboratory

California Institute of Tech., Pasadena, CA91109, USA

Phone: +1-818-354-4368/Fax: +1-818-393-4820

e-mail: martin.G.Buehler@Jpl.nasa.gov

Treasurer: Carlo Bonamini, IRST-Istituto per la Ricerca

Scientifica e Tecnologica, 38050 Povo (Trento) - Italy

Phone: +39-461-314792/Fax: +39-461-314591/e-mail:

bonamini@irst.itc.it

Equipment Exhibition: Giampietro Carlevaro,

IRST-Istituto per la Ricerca Scientifica e Tecnologica, 38050 Povo (Trento) -Italy

Phone: +39-461-314359/Fax: +39-461-314588/

e- mail:carlevaro@itc.it

Local Arrangements: Morena Carli, ITC, IstitutoTrentino di Cultura, 38100

Trento - Italy

Phone: +39-461-210216 Fax: +39-461-314588

e-mail:carli@itc.it

ICMTS '96 Secretariat: Maddalena Bassetti,

IRST- Microsensors and System Integration Division Povo

38100 Trento - Italy

Phone: +39-461-314548/Fax: +39-461-314591/e-mail:

bassetti@ irst.itc.it

ICMTS'96 Technical Program Committee:

Tsuneo Ajioka	Oki	Japan
Charles Alcorn	IBM	USA
Kunihiro Asada	Univ. of Tokyo Japan	
Robert Ashton	AT&T	USA
Lawrence Bair	DEC	USA
Bernard Baylac	SGS-Thomson	France
Martin Buehler	JPL	USA
Gordon Claudius	Rockwell	USA
Michael Cresswell	NIST	USA
Kazunari Honma	Sanyo	Japan
Yoshiaki Hagiwara	Sony	Japan

Edward Hakim	US Army	USA
Alfred Ipri	David Sarnoff Res.	USA
Hiroshi Koyama	Misubishi	Japan
Jun Kudo	Sharp	Japan
Yukinori Kuroki	Kyushu Univ.	Japan
Loren Linholm	NIST	USA
Emilio Lora-Tamayo	CNM	Spain
Michael Mitchell	Honeywell	USA
Takashi Ohzone	Toyama Pref. Univ.	Japan
Alfred Papp	Siemens	Germany
Harold Parks	Univ. Of Arizona	USA
Mitsuchika Saito	Hewlett Packard	Japan
Willy Sansen	Katholieke Univ. Leuven	Belgium
Nobuo Sasaki	Fujitsu	Japan
Akella Satya	IBM	USA
Dieter Schroder	Arizona State Univ.	USA
Noboru Shiono	NITT	Japan
Giovanni Soncini	IRST:Univ. of Trento	Italy
Yoichi Tamaki	Hitachi	Japan
Hans Tuinhout	Philips	The Netherlands
Vance Tyree	USC/ISI	USA
Anthony Walton	Univ. of Edinburgh	UK
Toshiharu Watanabe	Toshiba	Japan
He Yie	Southeast Univ.	PRC

ICMTS 1996 Steering Committee

Martin G. Buehler	JPL	USA
Michael Cresswell	NIST	USA
Loren W. Linholm	NIST	USA
Michael Mitchell	Honeywell	USA
Takashi Ohzone	Toyama University	Japan
Anthony J. Walton	Edinburgh University	U.K.