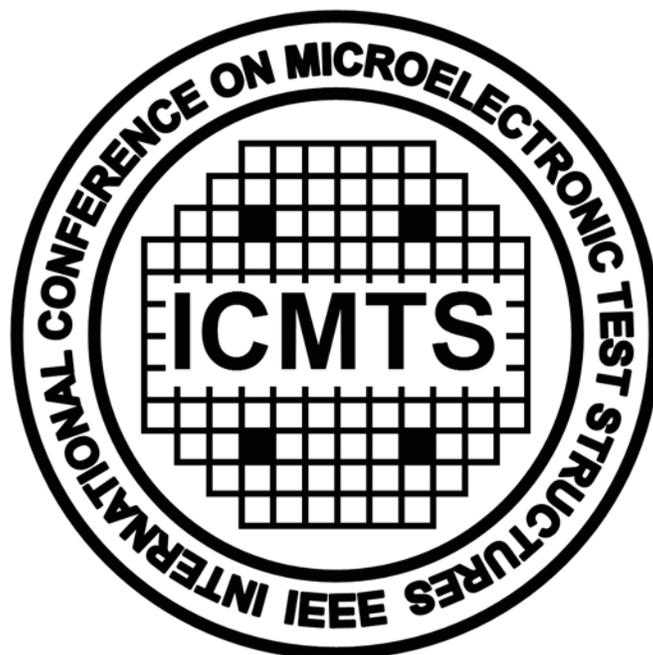


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# Session 1 - Reliability and Array Structures

## 1-1 14nm BEOL TDDDB Reliability Testing and Defect Analysis

T. Kane



## 1-2 A Novel Structure of MOSFET Array to Measure Ioff-Ion with High Accuracy and Density

T. Suzuki, A. Anchlia, V. Cherman, H. Oishi, S. Mori, J. Ryckaert, K. Ogawa, G. Van der Plas, E. Beyne, Y. Fukuzaki, D. Verkest, and H. Ohnuma



## 1-3 Circuit Architecture and Measurement Technique to Reduce the Leakage Current Stemming from Peripheral Circuits with an Array Structure in Examining the Resistive Element

S. Sato, T. Ito, and Y. Omura



## 1-4 A Proposal for Early Warning Indicators to Detect Impending Metallization Failure of DMOS Transistors in Cyclic Operation

M. Ritter and M. Pfof



# Session 2 - Modeling

## **2-1 SPICE Modeling of 55nm Embedded Superflash® Memory Cells**

S. Martinie, O. Rozeau, M. Tadayoni, C. Raynaud, E. Nowak, S. Hariharan, and N. Do



## **2-2 Compact Modeling and Parameter Extraction Strategy of Normally-on MOSFET**

T. Umeda, Y. Hirano, D. Suzuki, A. Tone, T. Inoue, H. Kikuchihara, M. Muira-Mattausch, H. J. Mattausch



## **2-3 A Simple T-Model for On-Chip Spiral Inductors**

J.-W. Jeong, S.-K. Kwon, J.-N. Yu, S.-Y. Jang, S.-H. Oh, C.-Y. Kim, G.-W. Lee, and H.-D. Lee



## **2-4 A Four-Terminal JFET Compact Model for High-Voltage Power Applications**

W. Wu, S. Banerjee, and K. Joardar



# Session 3 - Process Evaluation

## **3-1 Accelerating 14nm Device Learning and Yield Ramp Using Parallel Test Structures as Part of a New Inline Parametric Test Strategy**

G. Moore, V. Liao, S. McDade, and B. Verzi



## **3-2 Employing an On-Die Test Chip for Maximizing Parametric Yields of 28 nm Parts**

J. Mueller, S. Jallepalli, R. Mooraka, and S. Hector



## **3-3 Robust Process Capability Index Tracking for Process Qualification**

C. Gu and C. C. McAndrew



## **3-4 New Compact Model for Performance and Process Variability Assessment in 1 4nm FDSOI CMOS Technology**

Y. Denis, F. Monsieur, G. Ghibaudo, J. Mazurier, E. Josse, D. Rideau, C. Charbuilet, C. Tavernier, and H. Jaouen



## **3-5 Silicon Thickness Monitoring Strategy for FD-SOI 28 nm Technology**

A. Cros, F. Monsieur, Y Carminati, P. Normandon, D. Petit, F. Arnaud , and J. Rosa



# Session 4 plus Exhibitor Presentations - Discussion Session

## **4-1 A Test Cell for Characterizing Wheat Using Dielectric Spectroscopy**

M. Buehler



## **4-2 Development of a Compacted Doubly Nesting Array in Narrow Scribe Line Aimed at Detecting Soft Failures of Interconnect Via**

H. Shinkawata, N. Tsuboi, A. Tsuda, S. Sato, and Y. Yamaguchi



## **4-3 The Impact of Deep Trench and Well Proximity on MOSFET Performance**

H. Sheng, T. Bettinger, and J. Bates



## **4-4 Contact Engineering for Nanocarbon Interconnect Test Devices**

Y. Abe, A. Vyas, R. Senegor, P. Wilhite, and C. Y. Yang



## **4-5 A Test Structure for Reliability Analysis of CMOS Devices and DC and High Frequency AC Stress**

T. Matsuda, K. Ichihashi, H. Iwata, and T. Ohzone



## **4-6 Measurement and Modeling of IC Self-Heating Including Cooling System Properties**

T. Nishimura, H. Tanoue, Y. Odate, H. J. Mattausch, and M. Miura-Mattausch



**4-7 Large Surface Strain Sensing Structures based on Elastic Instabilities**

Y. Li, G. McHale, J. G. Terry, S. Smith, A. J. Walton, and B. Xu



**4-8 Cross-Correlation of Electrical Measurements via Physics-Based Device Simulations: Linking Electrical and Structural Characteristics**

A. Padovani, L. Larcher, L. Vandelli, M. Bertocchi, R. Cavicchioli, D. Veskler, and G. Bersuker



**4-9 NPN CML Ring Oscillators for Model Verification and Process Monitoring**

C. Compton



**4-10 Driving Increased Yield, Quality and Throughput With An Integrated Enterprise Monitoring System**

G. Raines, R. Hierbaum, D. Park, and G. Levy



# Session 5 - Parameter Extraction

## **5-1 Compact Modeling Solution of Layout Dependent Effect for FinFET Technology**

D. C. Chen, R. Lee, G. S. Lin, T. H. Lee, M. F. Wang, and D. Y. Wu



## **5-2 A Simple Method for Characterization of MOSFET Serial Resistance Asymmetry**

D. Tomaszewski, G. Gluszko, J. Malesinska, K. Domanski, M. Zaborowski, K. Kucharski, D. Szmigiel, and A. Sierakowski



## **5-3 Threshold Voltage Extraction Method in 2D Devices having a mobility with Power-Law Dependence of Carrier Density**

V. Mosser, D. Seron, and Y. Haddab



## **5-4 Measurement of $V_{th}$ due to STI Stress and Inverse Narrow Channel Effect at Ultra-Low Voltage in a Variability-Suppressed Process**

Y. Ogasahara, M. Hioki, T. Nakagawa, T. Sekigawa, T. Tsutsumi, and H. Koike



# Session 6 - Capacitance

## **6-1 Monitoring Test Structure for Plasma Process Induced Charging Damage Using Charge-Based Capacitance Measurement (PID-CBCM)**

S. Mori, K. Ogawa, H. Oishi, T. Suzuki, M. Tomita, M. Bairo, Y. Fukuzaki, and H. Ohnuma



## **6-2 A Novel Gate Charge Measurement Method**

A, Mikatam H. Kakitani, R. Takeda, and A. Wadsworth



## **6-3 Area and Performance Study of FinFET with Detailed Parasitic Capacitance Analysis in 16 nm Process Node**

T. Okagaki, K. Shibutani, H. Matsushita, H. Ojio, M. Morimoto, Y. Tsukamoto, K. Nii, and K. Onozawa



## **6-4 In-line Monitoring Test Structure for Charge-Based Capacitance Measurement (CBCM) with a Start-Stop Self-Pulsing Circuit**

K. Sawada, G. Van der Plas, S. Mori, V. Cherman, A. Mercha, V. Diederik, Y. Fukuzaki, and H. Ammo



# Session 7 - Resistance

## **7-1 Design and Evaluation of a SiCr ThinFilm Resistor Matching Test Structure**

H. Tuinhout, N. Wils, P. Huiskamp, E. de Koning



## **7-2 Characterization of Recessed Ohmic Contacts to AlGaIn/GaN**

M. Hajlasz, J. J. T. M. Donkers, S. J. Sque, S. B. S. Heil, D. J. Gravesteijn, F. J. R. Rietveld, and J. Schmitz



## **7-3 Novel Sheet Resistance Measurement of AlGaIn/GaN HEMT Wafer Adapted from Four-Point Probe Technique**

J. Lehmann, C. Leroux, G. Reibold, M. Charles, A. Torres, E. Morvan, Y. Baines, G. Ghibaudo, and E. Bano



## **7-4 Sheet Resistance Measurement for Process Monitoring of 400° C PureB Deposition on Si**

L. Qi and L. K. Nanver



## **7-5 Combined Transmission Line Measurement Structures to Study Thin Film Resistive Sensor Fabrication**

A. Tabasnikov, A.J. Walton and S. Smith



# Session 8 - Emerging Technologies

**8-1 Test Structures for the Wafer Mapping and Correlation of Electrical, Mechanical, High Frequency Magnetic, and Composition of Electroplated Ferromagnetic Alloys**



E. Sirotkin, S. Smith, R. Walker, J. G. Terry, and A. J. Walton

**8-2 A Fully-Automated Methodology and System for Printed Electronics Foil Characterization**



F. Vila, J. Pallares, A. Conde, and Lluís Teres

**8-3 A Capacitive Based Piezoelectric AlN Film Quality Test Structure**



N. Jackson, Z. Olszewski, L. Keeney, A. Blake, and A. Mathewson

# Session 9 - Circuits

## **9-1 Silicon Measurements of Characteristics for Pass-gate/Pull-down/Pull-up MOSs and Search MOS in a 28 nm TCAM Bitcell**



K. Nii, K. Yamaguchi, M. Yabuuchi, N. Watanabe, T. Hasegawa, S. Yoshida, T. Okagaki, M. Yokota, and K. Onozawa

## **9-2 Test circuit for Accurate Measurement of Setup/Hold and Access Time of Memories**



N. Agarwal

## **9-3 Reduction of Overhead in Adaptive Body Bias Technology due to Triple-well Structure based on Measurement and Simulation**



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## **9-4 Sensitivity-Independent Extraction of $V_{th}$ Variation Utilizing Log-normal Delay Distribution**



A. K. M. M. Islam and H. Onodera

# Session 10 - RF

## **10-1 Characterization of Wideband Decoupling Power Line with Extremely Low Characteristic Impedance for Millimeter-Wave CMOS Circuits**

R. Goda, S. Amakawa, K. Katayama, K. Takano, T. Yoshida, and M. Fujishima



## **10-2 Observations on Substrate Characterisation through Coplanar Transmission Line Impedance Measurements**

L. Floyd and J. Pike



## **10-3 Systematic Calibration Procedure of Process Parameters for Electromagnetic Field Analysis of Millimeter-Wave CMOS Devices**

K. Takano, K. Katayama, S. Mizukusa, S. Amakawa, T. Yoshida, and M. Fujishima



## **10-4 Electromagnetic Field Test Structure Chip for Back End of the Line Metrology**

L. You, Y. Obeng, and J. Kopanski

