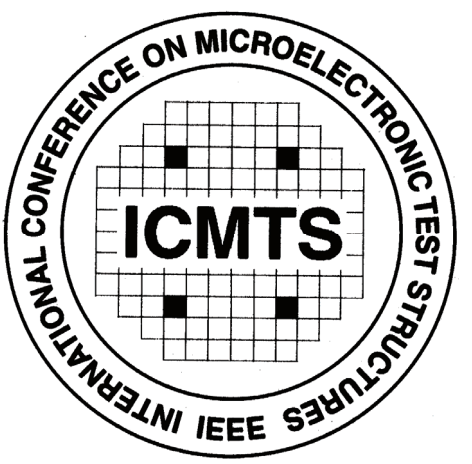
23rd IEEE ICMTS

2010 IEEE
International Conference on
Microelectronic Test Structures



FINAL PROGRAM

March 22-25
Hiroshima International
Conference Center, Japan

http://www.if.t.u-tokyo.ac.jp/ICMTS10/
icmts2010@if.t.u-tokyo.ac.jp

Sponsored by:
Association for Promotion of Electrical,
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The Institute of Electronics, Information and
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The Japan Society of Applied Physics
VLSI Design and Education Center

23rd IEEE ICMTS
2010 International Conference on Microelectronic Test Structures

Tutorial and Technical Program

2010 March 22-25
International Conference Center Hiroshima,
1-5, Nakajima-cho, Naka-Ku, Hiroshima Japan

http://www.if.t.u-tokyo.ac.jp/ICMTS10/
http://www.see.ed.ac.uk/ICMTS/

ICMTS 2010 CHAIRMAN'S LETTER

Dear Colleagues,

The 2010 International Conference on Microelectronic Test Structures (ICMTS 2010) will be held at the International Conference Center Hiroshima in Japan. This is the 23rd anniversary of the ICMTS and the 7th conference to be held in Japan.

Test structure is key characterization vehicle for process development, device development, circuit design and its production and its importance is increasing. ICMTS has brought engineers and researchers to discuss recent development and future directions of test structure over the past two decades. Topics of ICMTS have been expanded as semiconductor technologies and application advance. They include material and process characterization, replicated feature metrology, manufacturing of integrated circuits, reliability and product failure analysis, characterization of display, MEMS, sensors, RF IC , device & circuit modeling, yield enhancement, production process control, etc.

The ICMTS 2010 will consists of 44 papers in 9 oral sessions and 1 poster session. Detail of the sessions are described in this program. I believe all papers and posters turn on your interest and help your work. The sessions will be preceded by a one-day Tutorial Short Course on microelectronic test structure and there will be a equipment exhibition in parallel with the sessions.

Hiroshima is the largest city in the Chugoku region of western main land Japan and known as city of the world's first atomic bomb attack. Today it is modern, industrial and wonderful city with a lot of nice foods and historical legacy such as Miyajima. The International Conference Center Hiroshima is located at the center of the Hiroshima and it is within the Hiroshima Peace Memorial Park. It is very easy access from hotels and you can easily visit most of historical place, shopping and food area. I'm sure that everyone will get benefit by attending the various sessions and also enjoy Hiroshima. For further information, please visit the ICMTS web site at http://www.see.ed.ac.uk/ICMTS/

I look forward seeing you at the ICMTS 2010 in Hiroshima.

Sincerely,

Satoshi Habu
General Chairman

GENERAL INFORMATION

Conference Information

The International Conference on Microelectronic Test Strucuture (ICMTS) 2010 is technically sponsored by the IEEE Electron Devices Society and sponsored by the Association for Promotion of Electrical, Electronic and Information Engineering in cooperation with the Institute of Electronics, Information and Communication Engineers, the Japan Society of Applied Physics, and in collaboration with the University of Tokyo.

The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The Conference will be preceded by a one-day Tutorial Short Course covering a variety of technical areas related to Microelectronic Test Structures.

ICMTS homepage :
http//:www.see.ed.ac.uk/ICMTS/

Presentation

The official language of the conference is English.
The ICMTS considers oral and poster sessions equally, so does not classify oral presentations and poster sessions by the score of evaluation at the paper selection. Oral presentation time is 15 minutes plus 5 minutes for discussion. All poster presenters have also 3-minutes' 3-slides' flash presentation. For presentation, Windows laptop PC installed with Microsoft Powerpoint 2003 and Adobe Acrobat 7 will be available in the conference hall. It is highly recommended to use this PC so as to remove time loss in PC switching. Before March 21, send all presentation materials to icmts2010@if.t.u-tokyo.ac.jp. Also remember to bring original files as backup. There will be no slide projector available. All speakers are requested to report to registration desk located in front of the conference room before the session begins. Poster board for A0 size will be available for poster session.

Best Paper Award

One paper will be selected for the Best Paper Award by technical committee members. Papers can be selected from both oral sessions and poster session. The best paper will be announced at the end of the conference. Presentation of the award will be made at the ICMTS 2010.

Conference Proceedings

The IEEE ICMTS 2010 will publish proceedings and USB-Memory. One copy of the proceedings and one USB-Memory are included in the registration fee. Additional copies will be available at the Conference for 5,000 yen per copy for members of the IEEE or IEICE or JSAP, 7,000 yen per copy for non-members,

or from the IEEE after the conference.

Equipment Exhibition

An equipment exhibition will be held besides the conference room during the Conference to display equipment closely paralleling the nature of this meeting. This equipment exhibition will permit one-on-one discussions between exhibitors and conference attendees on the latest test equipment. Exhibits will be open as follows.

March 22 13:00 – 17:00
March 23, 24 9:00 – 17:00

The exhibitors list will be distributed on the day of the conference.

On-Line Conference Registration

JTB Corporate Solutions Co., Ltd. has been appointed as the official registration office for the conference and will handle registration. Please visit the ICMTS WEB page (http://www.else.k.u-tokyo.ac.jp/ICMTS10/) to make on-site registration.

Conference registration fees

Below are the conference fees for early, late, and on-site registrants.

Early Registration: (Registered by February 15, 2010)
Member* Non Member Student**
Tutorial ¥18,000 ¥21,000 ¥8,000
Technical ¥35,000 ¥43,000 ¥25,000
Sessions
Late Registration: (Registered after February 16, 2010)
Tutorial ¥25,000 ¥28,000 ¥10,000
Technical ¥38,000¥46,000 ¥26,000
Sessions
On-site Registration: (Registration at the Conference)
Tutorial ¥31,000 ¥34,000 ¥13,000
Technical ¥40,000 ¥48,000 ¥28,000
Sessions

* Must be a member of the IEEE or IEICE or JSAP.

**To qualify for reduced conference rates, you must be a Student Member, a full time student, not be self-employed, nor working part or full time at a facility or corporation.

Registration fees include admittance to technical sessions, equipment exhibits, morning and afternoon coffee breaks, reception, conference banquet, one copy of the proceedings and USB memory.

On-site registration schedule

On-site registration for the conference will be conducted at the Registration Counter (Conference room “Dahlia” on B2F, the 2nd floor below ground) at Hiroshima International Convention Center:
Monday, March 22* 8:30 – 19:00

Tuesday, March 23 8:30 – 17:00
Wednesday, March 24 8:30 – 16:00
Thursday, March 25 8:30 – 11:00
* Monday, March 22 is national holiday in Japan. Traffic timetable is a little different from that for weekday.

Payment of the registration fees

Registration fees should be payable to the IEEE ICMTS 2010 and must be in Japanese Yen only.
(1) Bank Check in Yen payable to the order of IEEE ICMTS 2010. Personal Checks are not acceptable.
(2) Credit Card in Yen: Master Card, VISA, Diners Club, American Express are available.
(3) Cash in Yen at the conference registration desk.

Cancellation

Due to advance financial commitments, refunds of registration fees requested after March 1, 2010, cannot be guaranteed. 5,000 yen processing fee will be withheld from all refunds. Requests for refunds of registrations cancelled after March 1 will be considered after the conference.
On or before February 28, 2010 ---------JPY5,000 of processing fee
On and after March 1, 2010 ----------100% of the registration fee

Messages

If you need to be contacted during the Conference Sessions, a message can be left at the Registration Counter (Conference room "Dahlia" on B2F, the 2nd floor below ground at Hiroshima International Convention Center) between the hours of 9:00 and 17:00, March 22, 23, 24, and of 9:00 to 12:00 on March 25. Messages will be placed on a Message Board beside the registration desk.

Banquet

The conference banquet will be held on Wednesday evening, March 24, on the boat cruising in Hiroshima bay which goes to Miyajima-island. Detailed information to how to access the Ujina Port will be announced at the conference site so please be careful. Conference registration fees include one banquet ticket. Guest ticket will be available for sale at the registration desk.
Japanese Traditional Music Concert on the Sea

The ICMTS 2010 is organizing a special music concert. The selection includes one of the most famous pieces of *Koto* Harp "*Haru-no-umi"*, and sounds from northern and southern parts of Japan.

- *Hokkai Min-yo-Cho*, Sound of North-Sea Ballad
- *Haru-no-umi*, Spring Sea scene
- Concerto of Ryukyu South Islands Ballad

The team is leaded by Ms. Miho Todoroki, a professor diplomated from Tokyo University of Arts. Ms Todoroki was appointed for the ICMTS 2007 banquet and got an excellent appreciation there. For the ICMTS 2010 team talented members who are active in Hiroshima area are nominated.

***Koto* Harp**	***Juchitigen* 17-codes lute**	***Shakuhachi* bamboo flute**
Miho Todoroki Ayumi Nakamura Fusako Watanabe Nobuko Kubo Satoko Osaki	Youko Kamizono	Meizan Iwaki

Sightseeng – *Miyajima island*

We recommend the participants to visit Miyajima-island and see Itsukushima-jinja Shrine. We can go there by tram and ferry. It takes about 70min to go there. It costs ¥840 One-day-trip-card and ¥300 Admission fee. It is difficult to arrange a bus to go there, because a bus cannot cross the sea. So, we decide to help you to visit there, instead of arranging an excursion. Please feel free to ask the local staffs at the registration desk.

Hiroshima Information

Hiroshima is on the seashore of Setonaikai, Japanese Mediterranean Sea. The city is placed at 700km in the west of Tokyo, capital of Japan. It has two famous tourist spots, Peace Memorial Park (A-Bomb Dome) and Miyajima-island (Itsukushima-jinja shrine). These are UNESCO's world heritage. Miyajima-island is also known as one of Japan's three great sites to visit. Hiroshima is also known as one of the richest city of popular foods such as «*Okonomiyaki*», Japanese tortilla-style food. The area is also rich in sea foods such as cultivated oysters «*kaki*» and sea breams «*tai*».

Climate and Clothing

The temperature in Hiroshima during the conference period will range between 5ºC and 15ºC. The weather is, however, often unpredictable during this season. So, light clothing and a sweater or light coat is recommended. Hiroshima International Convention Center is fully air-conditioned.

Hotel Accommodations

A block of rooms at Hotel Sunroute Hiroshima has been reserved for ICMTS10 to qualify for a room under our special rates. This hotel is the nearest hotel to Hiroshima International Convention Center.

http://www.sunroute.jp/HotelInfoSVE

Single room: ¥5,250 without breakfast/ ¥6,405 with breakfast

More information about hotel accommodations can be obtained at Web page:
http://www.hcvb.city.hiroshima.jp/e_navigator/
The hotels near Hiroshima International Convention Center are:
ANA Crown Plaza Hotel: http://www.anacrowneplaza-hiroshima.jp/en/index.html
Comfort Hotel Hiroshima: http://www.comfortinn.com/hotel-hiroshima-japan-JP027
Hokke Club Hiroshima: http://www.hokke.co.jp/3401/ (Japanese)

Transportation

General information how to access Hiroshima is obtained at Web page:
http://www.hcvb.city.hiroshima.jp/e_navigator/
We recommend you to use one of three airports below:
Tokyo Narita Airport: http://www.narita-airport.jp/en/
Kansai International Airport: http://www.kansai-airport.or.jp/en/index.asp
Hiroshima Airport: http://www.hij.airport.jp/english/
When you use Narita Airport, you need to take "Shinkansen" bullet train or a domestic flight to Hiroshima Airport. When you use Kansai Airport, you'd better take "Shinkansen" bullet train. Detailed access instruction from Kansai Airport is available at the ICMTS 2010 official WEB page:
(http://www.else.k.u-tokyo.ac.jp/ICMTS10/)
When you use Hiroshima Airport, you need to transfer at Narita Airport or Soul Airport. It is necessary to take a bus form Hiroshima Airport to the downtown.

TUTORIAL SHORT COURSE

Monday, March 22

8:10 – 17:00 Registration
8:50 – 9:00 Welcome address

9:00
1. Introduction to Microelectronic Test Structures
– Stewart Smith, *University of Edinburgh, Scotland*

This presentation will begin with a review of test structures detailing their history and hot topics over the past 20 years. The presentation will include the development of test structures for measuring sheet resistance, line width and contact resistance. Measurement and equipment developments will also be addressed focusing on procedures for obtaining accurate and repeatable measurements.

10:10
2. Origin of Advanced MOSFET Characteristics Important for Circuit Design
– Mitiko Miura-Mattausch, *Hiroshima University, Japan*

High performance of CMOS circuits can only be achieved if the basic MOSFET devices are able to support this performance. The physical origins which limit the performance of advanced MOSFETs are therefore discussed in detail. In particular, it is demonstrated that all MOSFET characteristics are caused by the carrier dynamics according to the potential distribution between source to drain terminal.

11:20
3. Variability in Scaled MOS Devices
– Kiyoshi Takeuchi, *NEC Electronics , Japan*

In this tutorial, various kinds of variability in MOS devices will be first reviewed. Then, the tutorial will focus on ``random fluctuation'', which is a kind of variability that exhibits no spatial correlation, and is rapidly increasing as FETs are scaled down. Current understanding of its root causes, and possible counter measures will be discussed. Finally, random telegraph noise, which is emerging as a new concern, will be briefly covered.

12:30 Lunch

14:00

4. Test Structures for Millimeter-Wave CMOS Circuit Design

– Kenichi Okada, *Tokyo Institute of Technology, Japan*

This tutorial will review high-frequency measurement and characterization of CMOS passive and active devices for designing millimeter-wave circuits. Recently, millimeter-wave circuits, e.g. 60GHz for Gbps wireless communication and 77GHz automotive radar, have been developed by using miniaturized CMOS processes. This presentation will show test structures of high frequency characterization up to 110GHz, and a de-embedding method using only two transmission lines instead of SOLT and Thru only methods will be introduced.

The tutorial also provides a detailed device characterization with some practical techniques. As an example, a 60GHz power amplifier implemented by using a 65nm CMOS process is demonstrated, and measurement and simulation results will be presented.

15:10

5. MEMS test structures and methods

– Anthony J. Walton, *University of Edinburgh, UK*

Micro Electro Mechanical Systems (MEMS) technology is a continuously emerging "non-standard" CMOS technology and it provides more and more functionalities to electronics. For the MEMS device to be used as an electron device, device and process engineers must be capable of extracting key parameters such as sacrificial layer etching speed and mechanical property to reliably produce the devices. This tutorial will review reported test structures and test methods for MEMS process and systems.

16:20

6. Wafer Test: 'Pumping Up The Volume' Precisely!

– Bill Verzi, *Agilent Technologies, USA*

In this tutorial, the "must-know" issues and methods for wafer-level VLSI testing will be presented. It is without question that reliable data comes from appropriate measurement as well as test structure. Although recent VLSI technology requires extremely high speed, low current, low voltage measurement, an engineer can relatively easily cope with these those extreme values, only by knowing the correct way of measurements. The aim of this talk is to refresh the basic knowledge, and the talk will be useful for both newcomer and experts.

17:30 Wrap-Up and Conclusion

Continues to welcome Reception

ICMTS 2010 Tutorial Lecturer Biography

Stewart Smith

Received the B.Eng. (hons) degree in electronics and electrical engineering in 1997 and the Ph.D. degree in 2003 from the University of Edinburgh, Scotland, UK. He has presented papers at every ICMTS conference from 1999 onwards and received the best paper award at ICMTS 2004 (Awaji, Japan). Stewart is currently an RCUK Academic Fellow with the School of Engineering at the University of Edinburgh. His research interests include the design and fabrication of biological and medical microsystems, test structures for microsystem fabrication processes and the electrical characterization of advanced photomasks and lithographic technologies.

Mitiko Miura-Mattausch

Professor Mitiko Miura-Mattausch received the Dr. Sc. Degree from Hiroshima University. She joined the Max-Planck-Institute for solid-state physics in Stuttgart, Germany as a researcher from 1981 to 1984. From 1984 to 1996, she was with Corporate Research and Developement, Siemens AG, Munich, Germany, working on hot-electron problems in MOSFETs, the development of bipolar transistors, and analytical modeling of deep submicron MOSFETs for circuit simulation. Since 1996, she has been a professor in Department of Electrical Engineering, Graduate School of Advanced Sciences of Matter at Hiroshima University, leading the ultra-scaled devices laboratory. She is a distinguished lecturer and a fellow of IEEE EDS.

Kiyoshi Takeuchi

Dr. Kiyoshi Takeuchi received the B.S., M.S., and Ph.D. degrees from the University of Tokyo, Tokyo, Japan, in 1984, 1986, and 1989, respectively. In 1989, he joined NEC Corporation and is currently with NEC Electronics Corporation, where he has been engaged in research activities on high performance CMOS device/circuit design, modeling, and related device physics. Currently, his major research interest is in MOS device variability and variability-aware circuit design. Since 2006, he is also with Semiconductor Leading Edge Technologies Inc., Tsukuba, Japan to join a MIRAI project, to study the physics of variability.

Kenichi Okada

Dr. Kenichi Okada received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively. He has been studying measurement and characterization of CMOS process fluctuation, and statistical static timing analysis (SSTA) for his Ph.D. thesis. From 2003 to 2007, he worked as an Assistant Professor for the Department of Integrated Research Institute in

Tokyo Institute of Technology, Japan. Since 2007, he has been an Associate Professor in the Department of Physical Electronics in Tokyo Institute of Technology, Japan. He has authored or co-authored more than 150 journal and conference papers. His current research interests include reconfigurable RF CMOS circuits for cognitive radios, 60GHz-40Gbps RF frontends, and 0.5V-supply clock generation.

Anthony J. Walton

Professor Anthony J. Walton received the B.Sc. degree in electrical and electronic engineering from the University of Newcastle upon Tyne, Newcastle, U.K., in 1974 and the M.Sc. and Ph.D. degrees from Manchester Polytechnic (now Manchester Metropolitan University), Manchester, U.K., in 1976. He is a Professor of microelectronic manufacturing with the School of Engineering and Electronics, The University of Edinburgh, Edinburgh, U.K. His present interests also include applications of micro and nanotechnology to biotechnology, sensors, and interconnect technology. He leads the technology research activities at the Institute for Integrated Micro and Nano Systems and was instrumental in setting up the Scottish Microelectronics Centre, The University of Edinburgh. This is a purpose-built facility for R&D and company incubation consisting of approximately 350 m^2 of class-ten clean rooms. Mr. Walton has published over 200 papers and is an Associate Editor of the IEEE Transactions on Semiconductor Manufacturing.

Bill Verzi

Bill Verzi (IEEE Member 1986) received a degree in electronics technology from West Valley College, Saratoga, CA, in 1981, supplemented with additional work in physics, mathematics, and computer science at San Jose State University, San Jose, CA. He joined the Intel Corporation in 1978 where he was initially involved in the production and quality assurance of memories. From 1979, he participated in the research and development of NMOS and CMOS processes used to make static/logic devices such as the first 8086 microprocessor. He joined Hewlett Packard in 1988, supporting applications of process evaluation through electrical test. Representing HP, he accepted an assignment to SEMATECH in 1990, as parametric test engineer to design and support electrical test methods for process characterization with a focus in plasma damage evaluation. He returned to Hewlett Packard, Austin, TX, in 1992, where he continued to support the application of process evaluation through electrical test methods. Now with Agilent Technologies, Austin, TX, his responsibilities include the support of process evaluation at the high volume systems level as well as the bench instrument level. He has served on the technical committee of the International Conference on Microelectronic Test Structures (ICMTS) since 1998. He was the technical chairman for the 2003 ICMTS in Monterey, California.

TECHNICAL PROGRAM SCHEDULE

Tuesday, March 23

8:30 – 17:00 Registration

9:00 Opening Remarks

Satoshi Habu, General Chairman

Tatsuya Ohguro, Technical Program Chairman

SESSION 1: Sensors

9:10 – 10:30

Co-Chairs: Emilio Lora-Tamayo,
Universitat Autonoma de Barcelona, Spain
Yoshio Mita, *The University of Tokyo*

9:10 1.1 Small embedded sensors for accurate temperature measurements in DMOS power transistor ……. 2

Martin Pfost[1], Dragoş Costachescu[1], Alja Podgaynaya[2], Matthias Stecher[2], Sergey Bychikhin[3], Dionyz Pogany[3], and Erich Gornik[3],

[1] *Infineon Technologies Romania, Romania,*
[2] *Infineon Technologies AG, Germany,*
[3] *Vienna University of Technology, Austria*

Device temperature is one of the most important limits for the safe operating area and the reliability of power DMOS transistors. Therefore, accurate measurements of their intrinsic device temperature are required. However, standard methods such as IR thermography usually cannot be applied to advanced smart power technologies where a thick power metal layer obscures the – often significantly hotter – active device area.

Thus, we propose to embed very small temperature sensors in the active DMOS cell array. These sensors allow for an accurate reading of the intrinsic device temperature while not influencing the DMOS behavior noticeably. The sensors are calibrated up to 600°C, validated by comparison to TIM measurements up to 400°C, and used to investigate thermal runaway. Results from 60 sensors embedded in one large power DMOS with on-chip analog multiplexing are also presented.

9:30 1.2 Fabrication of Test Structures to Monitor Stress in SU-8 Films used for MEMS Application ..…….. 8

S. Smith[1], N.L. Brockie[1], J. Murray[1], C.J. Wilson[2], A.B. Horsfall[2], J.G. Terry[1], J.T.M. Stevenson[1], A. R. Mount[1], and A.J. Walton[1],

[1]*The University of Edinburgh,* [2] *Newcastle University*

SU-8, an epoxy based negative photoresist, is widely used in the manufacture of micromechanical systems but can exhibit significant levels of stress build-up during

processing. This paper describes micromechanical test structures that provide the opportunity to spatially characterise stress the in SU-8 at different stages of the process. The structures are fabricated in a thick layer of SU-8 and are subsequently released from the underlying substrate using a dry chemical vapour etch process.

The initial results indicate that there is significant tensile stress in the SU-8, and that this demonstrates a radial variation along with a dependence on the process conditions.

9:50 1.3 A bulk micromachined vertical nano-gap Pirani wide-range pressure test structure for packaged MEMS performance monitoring ……14

Masanori Kubota, Toshihiro Okada, Yoshio Mita, Masakazu Sugiyama, Yoshiaki Nakano,
The University of Tokyo, Japan

A nano-gap Pirani gauge for integration with bulk MEMS sensors and actuators was fabricated by cutting-edge high aspect ratio bulk micromachining. The 150nm-wide, 5000nm-deep vertical trench enables wide-range pressure measurement; the device showed sensitity in all the tested range from 6.3 to 101.3kPa. ±0.27% of power variation around 35 mW was measured for ±1 kPa of pressure change from atmospheric pressure.

10:10 1.4 A Test Structure for Statistical Evaluation of pn Junction Leakage Current Based on CMOS Image SensorTechnology ……..18

Kenichi Abe, Takafumi Fujisawa, Hiroyoshi Suzuki, Shunichi Watabe, Rihito Kuroda, Shigetoshi Sugawa, Akinobu Teramoto, and Tadahiro Ohmi,
Tohoku University, Japan

We propose a test structure to enable us to evaluate statistical distributions of small pn junction leakage currents of numerous samples in a very short time (0.1 – 10 fA, 28,672 n+/p diodes in 0.77s). This test structure is based on CMOS active pixel image sensor, which contains a current-to-voltage conversion function by a capacitor and amplifiers of voltage signals in each pixel. The test structure can be designed easily because of a small number of mask layer requirements (at least one metal layer). Its simplicity has considerable benefits such as an easy fabrication for various processes without exceptional cares and also produces usefulness of statistical evaluation for anomalous pn junction leakage phenomena such as extremely large currents or dynamic and quantum fluctuations which show more and more as the device dimension shrinks.

10:30 – 10:40 Exhibition Presentations

10:40 – 11:00 Break

SESSION 2: Process Characterization I

11:00 – 12:20

Co-Chairs: Richard Allen, *National Institute of Standard and Technology, USA*
Mark Poulter, *National Semiconductor, USA*

11:00 2.1 Kelvin Resistor Structures for the Investigation of Corner Serif Proximity Correction ….…… 24

S. Smith[1], A. Tsiamis[1], M. McCallum[2], A.C. Hourd[3], J.T.M. Stevenson[1], and A.J. Walton[1],
[1]*The University of Edinburgh, Scotland,* [2]*Nikon Precision Europe,* [3]*The University of Dundee, Scotland*

Electrical test structures for the characterisation of Optical Proximity Correction (OPC) have been fabricated in thin aluminium using i-line lithography and reactive ion etching. Initial electrical measurements are presented which show an increase in the resistance of a right angled section of Al track as the level of OPC on the inside corner is increased. Structures with OPC applied to the outer corner do not show the same change in resistance. SEM images of similar Al test structures clearly show the effects of applying OPC and suggest that inner corner serif OPC leads to a narrowing of the conducting track.

11:20 2.2 Novel test structures for temperature budget determination during wafer processing …….. 30

E. J. Faber[1], R.A.M. Wolters[1,2], and J.Schmitz[1]
[1]*University of Twente, Netherlands,*
[2]*NXP Semiconductors, Netherlands*

Temperature is a crucial parameter in many planar technology processing steps. However, the determination of the actual temperature history at the device side of the substrate is not straightforward. We present a novel method for determining the temperature history of the process side of silicon wafers and chips, which is based on well-known silicide formation reactions of metal-Si systems and is determined via (4 point probe) resistance measurements. In this case we explored the Pd-Si system which has a suitable operating range from 100 – 200 °C. We propose a method based on metal layers patterned in different line configurations (using the width and number of the lines as parameters) and anticipate that silicide developments at these structures is geometrically dependent and hence can provide a way for obtaining a refined temperature information. First experiments on bulk Si wafers show that the proposed method yields predictable and stable results.

11:40 2.3 Efficient Characterization and Suppression Methodology of Edge Effects for Leakage Current Reduction of Sub-40nm DRAM Device ……. 34

Soo Han Choi[1,2], Young Hee Park[1], Chul Hong Park[1], Sang Hoon Lee[1], Moon Hyun Yoo[1], and Gyu Tae Kim[2],
[1]*Samsung Electronics, Korea,* [2]*Korea University, Korea*

With the process scaling, the leakage current reduction has been the primary design concerns in a nanometer-era VLSI circuit. In this paper, we propose a new lithography process-aware edge effects correction method to reduce the leakage current in the shallow trench isolation (STI).

We construct the various test structures to model Ileakage and Ileakage_fringe which represent the leakage currents at the center and edge of the transistor, respectively. The layout near the active edge is modified using the look-up table generated by the calibrated analytic model. On average, the proposed edge effects correction method reduces the leakage current by 18% with the negligible decrease of the drive current at sub-40nm DRAM device.

12:00 2.4 Highly automated sequence for Phase Change Memory test structure characterization ……..…….. 38

A. Toffoli[1], A. Fantini[1], G. Betti Beneventi[1,3]. L. Perniola[1], R. Kies[1], V. Vidal[2], J.F. Nodin[1], V. Sousa[1], A. Persico[1], J. Cluzel[1], C. Jahan[1], S. Maitrejean[1], G. Reimbold[1], B. DeSalvo[1], and F. Boulanger[1]
[1]*CEA LETI-Minatec France,* [2]*ST-Microelectronics, France,* [3]*Universita degli Studi di Modena e Reggio Emilia,*

The Phase Change Memory (PCM), is one of the most promising concepts, as a replacement of Flash memories that should be put in production in next years. However, even if the robustness of such technology is demonstrated for consumer stand-alone applications with typically GST as phase-change chalcogenide material, data retention at high temperature remains an issue, and seemingly even GST based alloys are not able to respect requirements of automotive embedded applications. That is why material research on alternative chalcogenide materials is still lacking, and thorough electrical characterization at analytical cell level is necessary to evaluate the performances of the integrated material. In this work we introduce this concept and the tests to evaluate new technological steps. In particular, we describe the test system optimization and we examine the full automated sequences used for statistic data collection. First step consist in acquiring the SET-to-RESET and RESET-to-SET programming characteristics; then data retention tests follow and eventually the cycling experiment close the run. Several characteristics and graphs illustrate this work displaying the key parameters.

12:20 – 13:50 Lunch

SESSION 3: Nano/MEMS

13:50 - 15:10

Co-Chairs: Jurriaan Schmitz,
University of Twente, Netherlands
Kelvin Yih-Yuh Doong,
TSMC, Taiwan

13:50 3.1 Pulsed measurement method for characterizing chemical solutions using nanowire FETs ..…….. 44

Marleen Mescher[1,2,3], Bout Marcelis[2], Marco de Wild[2], Johan Klootwijk[2], [1]*Materials innovation institute M2i, Netherlands* [2]*Philips Research, Netherlands,*
[3]*Delft University of Technology, Netherlands*

This paper presents a method for characterizing chemical solutions using nanowire field effect transistors. A pulsed gate potential method is used to prevent instabilities related to the dynamics of ions and other charged species present in the solution. Applying this method realizes a significant increase of the stability of the drain current versus gate potential characteristics of the devices, enabling reproducible characterization of chemical solutions with nanowire field effect transistors in aqueous environments.

14:10 3.2 A test vehicle and a two step procedure to evaluate a massive number of single-walled carbon nanotube field effect transistors ….……48

I.Martin-Fernandez,M.Sansa, F.Perez-Murano, P. Godignon, E. Lora-Tamayo,
Instituto de Microelectrónica de Barcelona, Spain

We present an automatic testing procedure to evaluate massive amounts of CNT-FETs that have been fabricated as a test vehicle. The procedure has been used to evaluate almost 140,000 CNT-FET devices that had been batch fabricated in a 4 inch wafer. The possibility of using data obtained from the automatic testing to achieve statistical analyses on device fabrication and on device electric characteristic is also analyzed.

14:30 3.3 Test structures for characterising the integration of EWOD and SAW technologies for microfluidics ….. 52

Y. Li[1], Y.Q. Fu[2], B.W. Flynn[1], W. Parkes[1], Y. Liu[2], S.D. Brodie[2], J.G. Terry[1], L.I. Haworth[1], A. Bunting[1], J.T.M. Stevenson[1], S. Smith[1], and A.J. Walton[1], [1]*The University of Edinburgh,* [2]*Heriot-Watt University, UK*

This paper presents details of the design and fabrication of test structures specifically designed for the characterisation of two distinct digital microfluidic technologies: Electro-Wetting On Dielectric (EWOD) and Surface Acoustic Wave (SAW). A test chip has been fabricated that includes structures with a wide range of

dimensions and provides the capability to characterise enhanced droplet manipulation as well as other integrated functions. In particular, we detail the use of EWOD to anchor droplets while SAW excitation is applied to perform mixing.

14:50 3.4 A Balanced-SeeSaw MEMS Swing Probe for Vertical Profilometry of Deep Micro Structures ….…… 58

Yoshio Mita[1], Jean-Bernard Pourciel[2], Masanori Kubota[1], Shaojun Ma[1], Satoshi Morishita, Agnès Tixier-Mita[1], and Takahisa Masuzawa[1], [1]*The University of Tokyo, Japan,* [2]*LAAS-CNRS, Université de Toulouse, France*

An actuator-integrated MEMS needle probe is improved to measure vertical surface profile of narrow and deep test structures such as microholes and trenches. A newly developed surface scanning method, called "swing probing", can reduce the measurable feature size by factor of up to eight (i.e. from 40 μm down to 5 μm for 50μm-deep trenches, and down to 25 μm for 1mm-deep ones) as compared to traditional "slide probing". The improvement is due to the new "Balanced-SeeSaw" probe design that guarantees rotational movement without wobbling as well as sensitivity increase. Since the design is highly scalable, the probe can further reduce target feature size as well as measurement resolution thus may enlarge the application field of such surface quality assessment technology to MEMS process test structure monitoring.

15:10 – 15:40 Break

SESSION 4: Poster

15:40 – 18:20

Co-Chairs: Anthony J. Walton, *University of Edinburgh, UK*
Takashi Ohzone*, Dawn Enterprise, Japan*

15:40 4.1 On the validity of bisection-based thru-only de-embedding …… 66

T. Sekiguchi, S. Amakawa, N. Ishihara, and K. Masu, *Tokyo Institute of Technology, Japan*

The validity of the thru-only de-embedding method that uses mathematically bisected halves of a left-right symmetric THRU pattern is assessed in this paper. The popularly used Π-equivalent representation of a THRU and the bisection thereof is neither unique nor its validity firmly established. It is shown that an equally simple T-equivalent-based bisection gives better results than the Π-equivalent-based bisection by comparing the two bisecting methods with a result obtained from an independent method. The thru-only de-embedding method is also compared with the

conventional open-short and short-open methods, and the interrelationship among them expected from the assumed equivalent circuit representations of the relevant dummy patterns is confirmed. This is made possible by using the odd-mode responses of symmetric 4-port devices as the 2-ports under study. This way, nonidealities associated with ordinary 2-port dummy patterns is avoided.

15:43 4.2 Orientation Dependence and Asymmetry of Subthreshold Characteristics in CMOSFETs ……..... 72

T. Matsuda[1], Y. Matsumura[1], H. Iwata[1] and T. Ohzone[2]
[1]*Toyama Prefectural University, Japan*
[2]*Dawn Enterprise, Japan*

Orientation dependence and asymmetry of VT (threshold voltage), gm (transconductance), S (subthreshold slope), and Ioff (off-state current at VG = 0 V) in 0.18 μm n-MOSFETs were measured and analyzed. The test structure contains 8 different channel orientation angles of 0°/45°/90° and three kinds of process conditions. Although VT, gm and S scarcely show particular anisotropy except for the variation of MOSFET structure and/or impurity profile, the orientation dependence of GIDL characteristics is observed in the wafer with the higher extension dose.

15:46 4.3 MOSFET-Array for Extracting Parameters Expressing SPICE-Parameter Variation ……..……. 76

Kazuo Terada[1], Naoya Ekida[1], Katsuhiro Tsuji[1], Takaaki Tsunomura[2] and Akio Nishida[2], [1]*Hiroshima City University, Japan,* [2]*MIRAI-Selete, Japan*

Parameters in Pelgrom's model, which express SPICE-model parameter variations, are evaluated using MOSFET array which has 16K DUTs and is made using 65-nm technology. It is found that the parameters expressing the random component of the variation are dominant, and that the parameters expressing the systematic component are mainly determined by the gate-insulator thickness.

15:49 4.4 Analysis of the Performance of a Micromechanical Test Structure to Measure Stress in Thick Electroplated Metal Films ……..……. 80

S. Smith[1], N.L. Brockie[1], J. Murray[1], C.J. Wilson[2] A.B. Horsfall[2], J.G. Terry[1], J.T.M. Stevenson[1], A. R. Mount, and A.J. Walton[1]
[1]*The University of Edinburgh,* [2]*Newcastle University, UK*

Previously reported suspended microrotating test structures designed to measure the stress in thick layers of electroplated Permalloy (NiFe alloy) have been analysed using finite element modelling and compared with

experimental measurements. These results have been used to optimise a stress sensor test structure and design a new mask, with an array of test structures specifically designed to wafer map the stress of thick nickel and Permalloy films. This is the first time these structures have been employed for determining spatial variation in film stress and the results of this characterisation are reported for nickel.

15:52 4.5 New RF Intrinsic Parameters Extraction Procedure for advanced MOS Transistors ……..…… 86

J. C. Tinoco[1], A. G. Martinez-Lopez[2], M. Emam[3], and J.-P. Raskin[3],
[1]*Universidad Nacional Autónoma de México,* [2]*Universidad Politécnica de la Región Ribereña, Mexico,* [3]*Université catholique de Louvain, Belgium*

A new extraction method of the intrinsic parameters of the small-signal equivalent circuit model of SOI MOS transistors (MOSFET) is presented. This new method does not need the previous knowledge of the extrinsic series resistances, moreover, it is possible to directly determine the intrinsic parameters at the bias point of interest. Floating-Body SOI MOSFETs are analyzed using this method.

15:55 4.6 *SIS* Wide-Band Model Extraction Methodology for SOI On-Chip Inductor ..…… 90

Rasit Onur Topaloglu[1], Jung-Suk Goo[1], Alvin L. S. Loke[2], Michael M. Oshima[2], and Sam Wonsae Sim[2],
[1]*GLOBALFOUNDRIES Inc, USA,* [2]*Advanced Micro Devices, USA*

On-chip inductors are recently in high demand even for digital applications due to strict jitter and phase noise requirements in oscillators. Accurate and fast modeling techniques are needed to enable low-cost and fast silicon turnaround. We present a fast and accurate methodology named scaled, iterative, and sampled (*SIS*) non-linear least squares optimization to extract wide-band model parameters suitable up to 20 GHz for inductor. To test our methodology, we implement a silicon-on-insulator (SOI) inductor in a 45 nm technology. The inductor is suitable for 8 to 20 GHz operation with 1.45 nH inductance and a quality factor of 17 at 10 GHz. We correlate our results to silicon measurements and achieve a very good fit between our models and silicon data. With our methodology, we achieve model turnaround time of a few hours.

15:58 4.7 Direct Probing of Trapped Charge Dynamics in SiN by Kelvin Force Micrscopy ..…….. 94

E. Vianello[1], E. Nowak[2], D. Mariolle[2], N. Chevalier[2], L. Perniola[2], G. Molas[2], J.P. Colonna[2], F. Driussi[1] and L. Selmi[1], [1]*DIEGM, Italy,* [2]*CEA–LETI MINATEC, France*

The growing importance of nitride–based non–volatile memories has increased the interest in the characterization of the physical properties of silicon nitride (SiN). In this work, we explore the potential of Kelvin Force Microscopy (KFM) measurements to investigate the lateral charge transport in SiN layers with two different compositions (standard, *std*, and Silicon rich, *Si–rich*). The dynamics of the lateral spread of the trapped charge is analyzed with the help of three dimensional numerical device simulations.

16:01 4.8 Electrical Characterization of Novel PMNT Thin-films …….. 98

Wenbin Chen[1], Kevin G. McCarthy[2], Mehmet Çopuroğlu[1], Shane O'Brien[1], Richard Winfield[1], and Alan Mathewson[1],
[1]*Tyndall National Institute, Ireland*
[2]*University College Cork, Ireland*

This paper presents the systematic investigation by electrical characterization of PMNT (lead magnesium niobate - lead titanate, $Pb(Mg_{0.33}Nb_{0.67})_{0.65}Ti_{0.35}O_3$) thin-films with different fabrication parameters. The PMNT thin-films are processed under different conditions including annealing at various temperatures. Capacitance-voltage (C-V), current-voltage (I-V), capacitance-frequency (C-F), dissipation factor-frequency (D-F) and complex impedance-frequency (Z-F) measurements are presented.

16:04 4.9 Investigation on the Field Leakage Current in 0.35µm CMOS Technology at High Temperature ……. 102

Soon Tat Kong, Paul Stribley, and Chris Lee,
X-FAB Semiconductor Foundries, UK

For the first time, this paper demonstrates the experimental results for two types of test structures of field transistors up to 200°C. The field transistor structures which are stripe (conventional) and square ring (new) structures were measured and investigated in term of field leakage current and onstate characterization at high temperature.

Wednesday, March 24

8:30 – 16:00 Registration

SESSION 5: Circuit

9:00 – 10:20

Co-Chairs: Satoshi Habu, *Agilent Technologies, Inc., Japan*
Kazuo Terada, *Hiroshima City University, Japan*

9:00 5.1 Generation, Elimination and Utilization of Harmonics in Ring Oscillators 108

Manjul Bhushan and Mark B. Ketchen, *IBM, USA*

Higher frequency harmonics in ring oscillators are problematic in both data acquisition and analysis. The origin of these undesirable harmonics and a circuit scheme for effectively eliminating them are described. Controlled generation of higher harmonics, on the other hand, enables unique applications in determining circuit power performance trade-offs.

9:20 5.2 Test Circuit for Measuring Single-Event-Induced Charge Sharing in Deep-Submicron Technologies ... 114

Oluwole A. Amusan[1], Bharat L. Bhuva[1], Megan C. Casey[1], Matthew J. Gadlage[1], Dale McMorrow[2], L. W. Massengill[2], [1]*Vanderbilt University,* [2]*Naval Research Laboratory,USA*

A novel on-chip test circuit to measure single-event induced charge sharing has been developed and implemented in an IBM 90 nm process. Test measurements with Two-Photon Absorption (TPA) backside laser irradiation helps demonstrate the effectiveness of the test circuit in characterizing charge sharing effects for sub-100 nm bulk CMOS processes.

9:40 5.3 Ring Oscillator Based Embedded Structure for Decoupling PMOS/NMOS Degradation with Switching Activity Replication 118

Fahad Ahmed and Linda Milor,
Georgia Institute of Technology, USA,

Until recently, negative bias temperature instability (NBTI) has been regarded as the primary reliability concern. However, with the introduction of high-k metal gate stacks, positive bias temperature instability (PBTI) has gradually become equally important. Conventional ring oscillator based structures monitor the delay/frequency through an inverter chain to track the PMOS threshold voltage (Vt) degradation due to NBTI, with the assumption of zero degradation in the NMOS device. Therefore these structures lose their effectiveness in the presence of PBTI. In this work, we propose a ring oscillator based test structure that

isolates the Vt degradation in the PMOS device and the NMOS device, hence permitting simultaneous monitoring of both. We also introduce a switching activity replication scheme for more accurate prediction of degradation in actual data paths.

10:00 5.4 An Embedded Process Monitoring Test Chip Architecture 122

Sachin Idgunji, Vikas Chandra, Cezary Pietrzyk, Imran Iqbal, Rob Aitken, and Greg Yeric, *ARM Inc., USA*

We present a test chip architecture which embeds a thorough set of process characterization ring oscillators into a synthesized processor core. We discuss the motivation, implementation, and results from sub-40nm technology silicon.

10:20 – 10:50 Break

SESSION 6: Process Characterization II

10:50 – 12:10

Co-Chairs: Christopher Hess, *PDF Solutions, USA*
Yoichi Tamaki, *CASMAT, Japan*

10:50 6.1 Test Structures for Characterization of Through Silicon Vias 130

Michele Stucchi, Daniel Perry, Guruprasad Katti, and Wim Dehaene, *IMEC, Belgium*

As silicon technology reaches extreme sub-um dimensions, the industry has reached for "more than Moore" solutions to enable advancements in integration, lower system cost, and improve packaging footprints. Probably the best known of the more-than-Moore solutions is 3D chip stacking using through silicon vias (TSVs). This technology requires accurate characterization of the TSV, the thinned silicon, and the stacked die. Our paper deals with TSV characterization by means of specially designed test structures.

11:10 6.2 On-Wafer Inductance and Resistance Characterization of Sub-5pH Deep Substrate Ground Vias 136

Volker Blaschke and Robert Zwingman, *TowerJazz, USA*

A low parasitic inductance ground for SiGe power amplifiers has been realized using a deep silicon via (DSV). The inductance of the DSV is approximately one order of magnitude smaller than the thru-wafer-via (TWV) inductance of ~21 pH enabling a ground path for power amplifiers in common emitter configuration with literally no parasitic inductance. In this paper we compare two on-wafer measurement approaches, a single port and a two

port shunt resonator test structure to characterize such a small inductance. The resistive component in the DSV is dominating and required careful consideration in the two approaches to yield accurate characterization results.

11:30 6.3 Characterization of Thermal-Mechanical Stress in 3D Stacked IC for Analog Design 140

Nikolaos Minas[1], Geert Van der Plaas[1], Herman Oprins[1], Yu Yang[2], Okoro Chuckwudi[2], Abdelkarim Mercha[1], Vladimir Cherman[1], Cristina Torregiani[1], Dan Perry[3], Miro Cupac[1], Michael Rakowski[1] ,Pol Marchal[1],
[1]*IMEC, Belgium,* [2]*K.U.Leuven, Belgium,* [3]*Qualcomm CDMA Technologies, Belgium*

In this paper we present test structures and measurement techniques that enable extraction of significance of effects expected in 3D TSV technologies. The DAC test structure is optimized to detect Ion changes down to 0.5 % due to TSV proximity, TSV orientation, thermal hotspots and wafer thinning/stacking process. The results obtained from the stand-alone MOS devices and the DAC structure that clearly indicate the impact of TSV proximity and TSV orientation on the carrier mobility of nearby transistors.

11:50 6.4 Fully Understanding the Mechanism of Misalignment-Induced Narrow-Transistor Failure and Carefully Evaluating the Misalignment-Tolerant SRAM-Cell Layout 146

Satoshi Nakai[1], Yasumori Miyazaki[1], Ryo Nakamura[1], Masato Suga[1], Tomoya Tsuruta[1], Makoto Yasuda[2], Takamitsu Kashiwagi[1] and Yasuhiko Maki[1],
[1]*Fujitsu Microelectronics Japan,* [2]*Fujitsu VLSI, Japan*

We have demonstrated a misalignment-tolerant SRAM cell successfully, whose layout has been created from consideration of narrow-transistor failure through physical and electrical analyses. To evaluate an advantage of the layout, we have performed an intentionally misaligned experiment using a test structure with each SRAM block featuring a neighbor alignment-inspection mark.

12:10 – 13:30 Lunch

13:30 – 13:40 ICMTS 2011 Presentation

SESSION 7: Capacitance

13:40 – 15:00

Co-Chairs: Hans P. Tuinhout, *NXP Semiconductor, Netherlands*
Stewart Smith, *University of Edinburgh, UK*

13:40 7.1 A Test Structure for Integrated Capacitor Array Matching Characterization ……152

Werner Posch, Gilbert Promitzer, and Ehrenfried Seebacher,
Austriamicrosystems AG., Austria

A novel characterization setup for integrated capacitor array mismatch determination is presented. The biasing of twenty capacitor units and the selection of a specific array are controlled by externally generated digital signals. Information about the spatial matching behavior is provided for an entire MIM capacitor array, where the relevant parameters are the standard deviations σ (ΔCi / C) and the offsets μ(ΔCi / C) of units i. Furthermore, the measurement repeatability is determined and an advanced derivation to consider the correlations introduced by the circuit structure and the extraction method is presented. The corresponding test chips were successfully realized in 0.35μm and 0.18μm standard CMOS technologies.

14:00 7.2 Correlation between Direct Charge Measurement (DCM) and LCR Meter on Deep Submicron CMOS Test Structure Capacitance Measurement ……158

Yasuhiro Miyake, Masaharu Goto, Shunsuke Fujii,
Hidetoshi Nishimura,
Agilent Technology International Japan

This paper reports capacitance measurement correlation between Direct Charge Measurement (DCM) and conventional LCR meter on 0.18μm CMOS test structure. Measurement results of interconnect and MOSCAP test structures are presented. Mathematical analysis shows that DCM and LCR meter results correlate very well for MOSCAP as well. Amplitude Adjustment Method and Amplitude Extrapolation Methods are proposed to calibrate nonlinear C-V measurement errors. Theoretical discussion can also be applied to Charge-Based Capacitance Measurement (CBCM) because it uses similar stimulus.

14:20 7.3 An Efficient Method of Calibrating MOSFET Capacitances by way of Excluding Intra-DUT Parasitic Contributions …… 164

Yasuhisa Naruta, Rishou Koh, and Takahiro Iizuka,
NEC Electronics , Japan

An efficient exclusion of intra-DUT parasitic capacitances has been enabled by a combination of capacitance measurement and 3D capacitance simulation on structures with varying number of contacts per side for a MOSFET structure. Accounted for is the capacitance shift due to the presence of contact plugs, the physical shapes of which are not necessarily the same as their geometrical representations in design space.

14:40 7.4 Fast RF-CV Characterization Through High-Speed 1-port S-parameter Measurements 170

R. W. Herfst[1], P. G. Steenekeny[2], M. P. J. Tiggelman[1], J. Stulemeijerz[3], and J. Schmitz[1],
[1]University of Twente, *Netherlands,* [2]NXP Semiconductors, *Netherlands,* [3]*EPCOS Netherlands*

We present a novel method to measure the capacitance-voltage relation of an electronic device. The approach is accurate, very fast, and cost-effective compared to the existing off-the-shelf solutions. Capacitances are determined using a single-frequency 1-port S-parameter setup constructed from discrete components. We introduce a new way to correct for non-linearities of the used components, which greatly increases the accuracy with which the phase and magnitude of the reflected signal is measured. The measurement technique is validated on an RF-MEMS capacitive switch and a BST tunable capacitor. Complete capacitance-voltage curves are measured in less than a millisecond, with a measurement accuracy well below 1%.

15:00 – 15:20 Break

SESSION 8: Matching

15:20 – 16:20

Co-Chairs: Larg H. Wieland, *PDF Solutions, USA*
Kiyoshi Takeuchi, *NEC Electronics, Japan*

15:20 8.1 Methodology to evaluate the impact of segmentation on MOSFET matching 176

Hans Tuinhout, Nicole Wils, Maurice Meijer, Pietro Andricciola, *NXP Semiconductors, Netherlands*

This paper summarizes an experimental study on matching of long NMOS transistors and the effects of splitting-up long transistors into series of short transistors. For this purpose, a dedicated set of matched pair test structures were designed and manufactured in a 45 nm CMOS technology. This study is used to evaluate relative threshold voltage matching performance degradations that are observed for long channel devices in such technologies.

15:40 8.2 Influence of metal coverage on transistor mismatch and variability in copper damascene based CMOS technologies 182

Nicole Wils, Hans Tuinhout and Maurice Meijer, *NXP Semiconductors, Netherlands*

This paper summarizes a comprehensive study on the effect of asymmetrical metal coverage on matching

performance for a 45 nm copper damascene based CMOS process. We demonstrate that random mismatch fluctuations are not affected by metal layout asymmetries and we provide valuable new insights about the magnitude of systematic mismatches that can be expected due to asymmetrical layouts and CMP tiling. For the first time we also present results on the impact of temperature increases on both systematic as well as random drain current mismatches.

16:00 8.3 Test Structures to Quantify Contact Placement-Impacted Drain Current Variations 188

Rasit Onur Topaloglu, Zhi-Yuan (Joanne) Wu and Ali B. Icel, *Globalfoundries, USA*

The difference in the number of contacts across different transistors and standard cells results in current variations across the channel. In this work, we present test structures to target this effect and characterize and quantify the impact on 45 nm SOI silicon. After comparing the impact of contact resistance between 65 nm and 45 nm silicon, we provide and analyze our 45 nm test structure results and provide a means to extract mean contact resistance from our test structures. We observe that impact due to contact resistance can be up to 10% for 45 nm, while it could have been of less importance (less than 4%) for 65 nm technology. Such test structures and methodology help us provide intrinsic device models in 45 nm without inaccuracies or resistive double counting that may be introduced due to placement-impacted contact resistance variations.

17:00 End of Exhibition

18:45 Embarkation on Cruising Boat "Ginga (Galaxy)" from Hiroshima Ujina Port.

Thursday, March 25

8:30 – 11:00 Registration

SESSION 9: Parameter Extraction and RF

9:00 – 10:20

Co-Chairs: Kevin Mccarthy, *University College,Ireland*
Greg Yeric, *ARM, USA*

9:00 A Global Parameter Extraction Procedure for
9.1 Multi-gate MOSFETs 194

Shijing Yao[1], Tanvir H. Morshed[1], Darsen D. Lu[1], Sriramkumar Venugopalan[1], Wsize Xiong[2],Ali M. Niknejad[1] and Chenming Hu[1],
[1]*University of California, Berkeley, USA*
[2]*Texas Instruments, USA*

A global I-V parameter extraction methodology for multi-gate MOSFET compact model is presented for the first time. New L-dependent properties are proposed to enable the accurate modeling of transistors over a wide range of gate length using a single set of model parameters. The results are verified with FinFET experimental data with effective channel lengths from 30nm to 10um. For both n and p type devices, excellent agreement between the data and the model has been demonstrated.

9:20 Compact Models of Parasitic Resistance of Resistors
9.2 for Analog Circuits 198

Kenta Yamada, *NEC Electronics, Japan*

Accurate and useful compact models of parasitic resistance of resistors for analog circuits are proposed. The model is applicable to any layout patterns and topologies normally used in analog circuits. In addition, test structures to measure the parasitic resistance correctly are shown and the models are validated for a 40nm CMOS technology.

9:40 Comprehensive Quality Assurance Methodology for
9.3 BSIM4.5 Corner Parameter Extraction 204

[1]Hiroo Masuda, [2]Satoshi Itoh, [3]Hiroshi Koike, [4]Naoki Wakita and [5]Ryosuke Inagaki, [1]*Renesas Technology,* [2]*Seiko-Epson,* [3]*Semiconductor Technology Academic Research Center,* [4]*Toshiba,* [5]*Rohm, Japan*

Quality assurance of shipped compact model parameters is one of the crucial problems for circuit designers as well as parameter providers in process foundries. However, very few reports have been published on this issue and it is virtually veiled so far. In this paper, we firstly propose a comprehensive methodology focused on corner parameter assessment for compact MOS models. Key technologies are: (1) rational target description of corner performances, (2) a new quantitative error definition of target performances, and (3) quality assurance strategy which can leads to a standardization scheme in parameter extraction framework. The new QA technology was verified with 90nm BSIM4.5 corner MOS model parameters. This activity has been supported by five companies who applied to STARC corner-parameter extraction contest using identical I-V and C-V experimental

data and corner-performance specifications. The result shows significant features that the quality of the corner-parameters is widely spread in terms of accuracy. Our new definition of allover RMS error is found to range 1.32% to 11.18% depending on the corner-parameters from contest applicants. Note that this work will give a new quantitative flow and algorithm for comprehensive corner parameter assessment.

10:00 9.4 Characterization & Modeling of Gate-Induced-Drain-Leakage with complete overlap and fringing model 210

D. Rideau[1], V. Quenette[1], D. Garetto[2], E. Dornel[2], M. Weybright[2], J.P Manceau[2], O. Saxod[1], C. Tavernier[1], H. Jaouen[1],
[1]*STMicroelectronics, France,* [2]*IBM France*

This paper investigates and models Gate Induced Drain Leakage (GIDL) for a wide variety of high voltage devices with different low doped drain (LDD) structures. Based on TCAD simulations, we propose semi-analytical a pseudo-2D model for Gate induced Drain leakage. This model includes a complete modeling of the overlap region accounting for technological process and bulk bias dependency through detailed electric field description.

10:20 – 10:40 Break

SESSION 10: Devices

10:40 – 12:00

Co-Chairs: Antoine Cros, *STMicroelectronics, France*
Bill Verzi, *Agilent Technologies, USA*

10:40 10.1 A Universal Structure for SRAM Cell Characterization 216

Xiaowei Deng, Theodore W. Houston, Anhkim Duong, Wah Kit Loh, *Texas Instruments,USA*

A universal test structure (UTS) for SRAM cell characterization is proposed and implemented in 65nm - 28nm technologies. The structure allows, for the first time, measurement of nearly all transistor and cell characteristics of an SRAM cell on silicon. It hence enables direct correlation among various measured transistor and cell characteristics, collection of intra-bit transistor mismatch data, and assessment of wafer level V_{min} sensitivity on transistor characteristics. Measured data are presented.

11:00 10.2 A unique and accurate extraction technique of the asymmetric bottom-pillar resistance for the vertical MOSFET 220

Koji Sakui and Tetsuo Endoh, *Tohoku University, Japan*

The concept of the measurement technique is to separate the paths by at least two directions; one is the current path, where the drain current flows, and the other is the noncurrent path, where the voltage is measured with the connection to the high-Z gate of the monitor circuit. The proposed measurement technique has been validated by HSPICE simulation.

11:20 10.3 Combined test structure for systematic and stochastic Mosfets and gate resistance process variation assessment 226

L. Bortesi, L. Vendrame, and G. Fontana, *Numonyx, Italy*

A powerful and compact test structure based on the combination of mosfet and resistor mismatch-like configurations is presented. This new combined solution helps to assess not only the systematic and stochastic mosfet and gate resistance electrical performance and their process variations but also the dependencies on the environment and the impact of different layout solutions.

11:40 10.4 On-chip In-situ Measurements of Vth and AC Gain of Differential Pair Transistors 232

Yoji Bando[1], Satoshi Takaya[1], Toru Ohkawa[2], Toshiharu Takaramoto[2], Toshio Yamada[2], Masaaki Souda[2], Shigetaka Kumashiro[2], Makoto Nagata[1]

[1]*Kobe University, Japan,* [2]*MIRAI-Selete, Japan*

In-situ DC measurements of individual transistors in a differential pair of an analog amplifier derive threshold voltage, V_{th}, of 1.0-V transistors in a 90-nm CMOS technology. On-chip continuous time waveform monitoring is used to evaluate AC response of the same amplifier. The distribution of AC gain versus V_{th} of transistors within amplifiers is captured. The degradation of common-mode rejection property is observed for an amplifier with intentionally introduced mismatches to the pair of transistors.

12:00 Best Paper Announcement
Closing Remarks

12:05 End of Conference

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Michael W. Cresswell	Natl. Inst. Stds & Tech.	USA
Loren Linholm		USA
Hans P. Tuinhout	Philips Research	The Netherlands
Anthony J. Walton	University of Edinburgh	Scotland

Technical Committee:

Richard Allen	NIST	USA
Robert Ashton	White Mountain Labs	USA
Antoine Cros	STMicroelectronics	France
Steve S. Chung	National Chiao Tung Univ.	Taiwan
Michael W. Cresswell	Natl. Inst. Stds & Tech.	USA
Kelvin Yih-Yuh Doong	TSMC	Taiwan
Satoshi Habu	Agilent Technologies Japan, Inc.	Japan
Michael Han	Qualcomm	USA
Christopher Hess	PDF Solutions Inc.	USA
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Chang Yong Kang	SEMATECH	USA
Choongho Lee	Samsung Electronics	Korea
Hi-Deok Lee	Chungnam Nat. Univ.	Korea
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Colin McAndrew	Freescale Semiconductor	USA
Kevin McCarthy	University College Cork	Ireland
Yoshio Mita	University of Tokyo	Japan
Shinichi Ogawa	SELETE	Japan
Tatsuya Ohguro	Toshiba Corp.	Japan
Luigi Pantisano	IMEC	Belgium
Mark Poulter	National Semiconductor	USA
Willy Sansen	Katholieke Univ. Leuven	Belgium
Ulrich Schaper	Infineon Tech. AG	Germany
Jurriaan Schmitz	Univ. of Twente	The Netherlands
Dieter Schroder	Arizona State Univ.	USA
Franz Sischka	Agilent Home Office	Germany
Brad Smith	Freescale Semiconductor	USA
Giovanni Soncini	IRST	Italy
Lee Stauffer	Keithley Instruments, Inc.	USA
Kiyoshi Takeuchi	NEC Corp.	Japan
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Kazuo Terada	Hiroshima City University	Japan
Hans P. Tuinhout	Philips Research	The Netherlands
Bill Verzi	Agilent Technologies	USA
Anthony J. Walton	University of Edinburgh	UK
Larg H. Wieland	PDF Solutions Inc.	USA
G.reg M. Yeric	ARM	USA

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ICMTS2010 Condensed Program

Monday March 22	Tuesday March 23	Wednesday March 24	Thursday March 25
8:15 Registration	8:30 Registration	8:30 Registration	8:30 Registration
8:50 Welcome	9:00 Opening Remarks	9:00 Session5: Circuit	9:00 Session9: Parameter Extraction and RF
9:00 Introduction to Microelectronic Test Structures	9:10 Session1: Sensors	10:20 Break	10:20 Break
10:10 Origin of Advanced MOSFET Characteristics Important for Circuit Design	10:30 Exhibition and Break	10:50 Session6: Process Characterization II	10:40 Session10: Devices
11:20 Variability in Scaled MOS Devices	11:00 Session2: Process Characterization I	12:10 Lunch	Best Paper Announcement
12:40 Lunch	12:20 Lunch	13:30 ICMTS 2011 Presentation	Closing Remarks and End of Conference
14:00 Test Structures for Millimeter-Wave CMOS Circuit Design	13:50 Session3: Nano/MEMS	13:40 Session7: Capacitance	Lunch (For excursion attendee only)
15:10 MEMS Test Structures and Methods	15:10 Break	15:00 Break	Excursion “*Hiroshima Afternoon*”
16:20 Introduction to Test Methods	15:40 Session 4: Poster	15:20 Session 8: Matching	
17:30 Wrap-Up and Conclusion		18:45 Embarkation on cruse ship “Galaxy” at Ujina Port	
18:00 Conference Welcome Reception			