2009 CONFERENCE COMMITTEE

Chair:
Greg Yeric
ARM, Ltd.

Technical Program Chair:
Richard Allen
NIST.

Tutorial Chair:
Mark Ketchen
IBM

Exhibit Chair:
Lee Stauffer
Keithley Instruments

U.S. Representative:
Loren Linholm

Asian Representative:
Kunihiro Asada
University of Tokyo

European Representative
Anthony A.J. Walton
University of Edinburgh

TECHNICAL PROGRAM COMMITTEE

Richard Allen, NIST
Hugues Brut, STMicroelectronics
Steve S. Chung, National Chiao Tung University
Michael W. Cresswell, NIST
Kelvin Y.-Y. Doong, TSMC
Satpshi Habu, Agilent Technologies, Japan
Michael Han, Qualcomm
Christopher Hess, PDF Solutions
Kjell O. Jeppson, Chalmers University of Technology
Chang Yong Kang, SEMATECH
Choongho Lee, Samsung Electronics Co.
Hi-Deok Lee, Chungnam National University
Loren Linholm
Emilio Lora-Tamayo, Universidad Autonoma de Barcelona
Alan Mathewson, NMRC
Colin McAndrew, Motorola
Kevin McCarthy, University College, Ireland
Yoshio Mita, University of Tokyo
Shinichi Ogawa, Selete
Tatsuya Ohguro, Toshiba Corp.
Takashi Ohzone, Okayama Prefectural University
Luigi Pantisano, IMEC
Mark Poulter, National Semiconductor Corp.
Willy Sansen, Katholieke University
Ulrich Schaper, ***Infineon Technologies***
Jurriaan Schmitz, University of Entwente
Dieter K. Schroder, Arizona State University
Franz Sischka, Agilent Technologies
Brad Smith, Freescale Semiconductor
Giovanni Soncini, University of Trento/IRST
Lee Stauffer, Keithley Instruments, Inc.
Kiyoshi Takeuchi, NEC
Yoichi Tamaki, Hitachi, Ltd.
Motoaki Tanizawa, Renesas
Kazuo Terada, Hiroshima University
Hans Tuinhout, NXP Semiconductors
Bill Verzi, Agilent Technologies
A.J. Walton, University Edinburgh
Larg Weiland, PDF Solutions
G.M. Yeric, ARM, Ltd.

GENERAL INFORMATION

The 2009 IEEE ICMTS will be held at the Embassy Suites Mandalay Beach Resort in Oxnard, California. The Conference headquarters hotel will provide guest accommodations as well as meeting facilities for all attendees. The technical program, consisting of ten sessions of contributed papers will be held March 31-April 2. A tutorial short course will be offered on Monday, March 30.

CONFERENCE REGISTRATION

Payment of the TECHNICAL SESSION registration fee entitles the registrant to one copy of the Technical Digest, entrance to all technical sessions and the exhibit hall, and all social events.

Payment of the SHORT COURSE registration fee entitles the registrant to one copy of the Short Course Workbook and luncheon. Short Course participants must register in advance.

For **Advance Registration,** complete the Registration Form and mail the form with payment to the Conference Headquarters. Advance registration forms must be received by the Conference Headquarters NO LATER THAN March 9, 2009 in order to receive the reduced registration fee. Registrations received after March 9 will be charged the late registration fee. Short Course participants should register in advance to guarantee a space at the course. On-site short course registration will only be accepted based on space availability.

If you fax your registration form, you must include credit card information and a 5% processing fees for the credit card transactions

Mail or fax your conference registration form and remittance to:

2009 ICMTS Conference
19803 Laurel Valley Place
Montgomery Village, MD 20886
1-301-527-0900 x104 • Fax: 1-301-527-0994
Email: wendyw@widerkehr.com

CANCELLATIONS: Refund requests must be received, in writing, by March 20 in order to receive a full refund, less a $25.00 processing fee. Due to financial commitments, refund requests received after February 21 cannot be guaranteed.

IEEE Members: In order to qualify for the member fees, you must list your IEEE membership number.

	ADVANCE (by March 9)	REGULAR (after March 9 and on-site)
Technical Session		
IEEE Member	$475	$525
Non-Member	$525	$575
Student	$275	$330
Short Course (ADVANCE Registration Only)		
IEEE Member	$300	$320
Non-Member	$340	$360
Student	$140	$140

HOTEL RESERVATIONS

DEADLINE: FEB. 27, 2009

A block of rooms has been reserved at the Embassy Suites Mandalay Beach Resort in Oxnard, CA. To make a reservation, call the hotel or go to the ICMTS on-line reservation page. Our Group Name is IEEE-ICMTS and the Group Code is IEE.

Embassy Suites Mandalay Beach Resort
2101 Mandalay Beach Road
Oxnard, CA 93035
Reservations: +1-800-368-2779
On-line: http://embassysuites.hilton.com/en/es/groups/personalized/OXNCAES-IEE-20090329/index.jhtml
Tele: 805-760-9041

Rates: $169 + tax single/double

HOTEL RESERVATIONS MUST BE RECEIVED BY FRIDAY, FEBRUARY 27 to guarantee the conference rate.

All changes and cancellations should be made directly with the hotel. It is the responsibility of each participant to make changes or cancellations no later than 48 hours prior to scheduled arrival. Room reservations will be held until 6:00 p.m. unless a later time is guaranteed by a credit card. Rooms are generally not available for check-in until 3:00 p.m. on the day of arrival.

TECHNICAL SESSION INFORMATION

The Technical Sessions will be held in the Embassy Ballroom at the hotel.

EQUIPMENT EXHIBITS: ICMTS vendor exhibits will be displayed in the Mandalay Ballroom AB on Monday, March 30 from 6:00 p.m. and will remain on display until 3:10 p.m. on Wednesday, April 1. A Welcoming Reception will be in the hall on Monday evening.

If you would like to exhibit at the conference, please contact Wendy Walker at the Conference Headquarters, 301-527-0900 x104; wendyw@widerkehr.com. Past exhibitors have included: HPL Technologies, Reedholm Instruments, Keithley Instruments, Silvaco, Sandia National Laboratories, TestChip Technologies, Cadence, Avanti!, Cascade Microtech, Agilent Technologies, QualiTau, Lucas/Signatone Corp. and BTA Technology.

TECHNICAL DIGEST

Extra copies of the Technical Digest can be purchased at the conference or through Advance Registration at a cost of $75.00. After the conference, digests will be available through the IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08855.

SOCIAL EVENTS

The hotel provides a full complimentary breakfast to their guests. The conference will host luncheons on Tuesday and Wednesday.

The Conference Banquet will be held on Wednesday, April 1 at the Ronald Reagan Presidential Library. Round trip bus transportation will be provided. Buses will depart from the front of the hotel starting at 4:30 p.m. One ticket is included with the registration fee, additional guest tickets may be purchased for $75.00.

An opening reception will be held in the Exhibit Hall on Monday evening 5:00 p.m. – 6:30 p.m.

TRANSPORTATION

By Air: Oxnard is located about 75 minutes north of Los Angeles Airport (LAX), 50 minutes from Burbank Airport (BUR), and 60 minutes south of Santa Barbara Airport (SBA). Or fly directly into Oxnard by regional carriers (United Express) and pick up a rental car -- the Oxnard Airport (OXR) offers daily connections through LAX to Oxnard (www.iflyoxnard.com). There is shuttle service available from LAX to Oxnard at an approximate cost of $65.00 one-way.

AIRPORT SHUTTLES:

The following shuttles provide service to and from LAX:
Roadrunner Shuttle 800.247.7919
Amadeuz Limousine & Shuttle 805.486.1873
Ventura County Airporter & Limousine 805.650.6600

By Car: Driving from L.A. to Oxnard, you can travel north along Highway 1 (along the coast) or take Highway 101. To drive north along the coast, take the Santa Monica Freeway (I10) west to Highway 1 (Pacific Coast Highway) then take PCH north. The drive takes about an hour (depending on traffic). To take freeways all the way from LAX, take the 405 north; exit the 405 onto the 101 west and continue north to Oxnard. Follow 101 west past the Oxnard exits to the Seaward Avenue exit. Turn left at Harbor Boulevard. Turn right on Costa de Oro. The hotel is directly ahead at the end of Cost de Oro. Travel time is approximately 90 minutes, depending on traffic.

WEATHER

The weather in Oxnard should average 67°F high / 50°F low. The chance of rain is slight, averaging less than an inch during the time we are there.

OXNARD AREA ATTRACTIONS

A little over an hour northwest of Los Angeles, Oxnard stands as the entrance to California's Central Coast and represents all that the Central Coast has to offer-a progressive cultural diversity wrapped in historic California-style. Oxnard prides itself on its diversity and nowhere is this more evident than in our offerings of things to do. Sample a glass of kosher red wine. Visit our Historic District. Celebrate at one of our cultural events. Visit the Henry T. Oxnard National Historic District and Heritage Square for a peek into early-20th century homes. Steel magnate and philanthropist Andrew Carnegie was one of the first to recognize the value of our city when in 1906 he donated money to build a city library. The library is now the Carnegie Art Museum, brimming with fine 20th century California art.

Perhaps Oxnard's best asset is our seven miles of uncrowded, white sandy beaches that offer surfers and sun-lovers a real haven. Oxnard is also a departure point for the Channel Islands National Park and Marine Sanctuary. Only 11 miles off the coast, this remote park comprised of five of the eight-island archipelago, has been called "America's Galápagos."

The Channel Islands Harbor, two miles from our historic downtown offers kayaking, electric boat rentals, private yacht and sailing charters, sport-fishing and scuba diving are just a few of Oxnard's outdoors adventures. And, for those who prefer land to sea, our nearly year-round sunny weather makes Oxnard an ideal venue for golf, biking, hiking and sightseeing. Pick your adventure and discover Oxnard's hidden treasures.

TOUR PROGRAM

Thursday, April 2
1:30p.m. – 5:30 p.m.
Cost: $65.00

A wine tour of the Santa Ynez Valley - tour two wineries and sample local wines. You'll learn about the viticulture of the area, the basics of wine production and "proper" tasting techniques. Get a first-hand look at some of our award-winning wineries and vineyards with a knowledgeable tour guide to lead the way! You'll enjoy a behind the scenes, not available to the general public, production tour that will highlight the production process from the grape in the vineyard to the final bottled product. You'll take part in interactive tasting demonstrations and have a chance to learn about the wines and about production.

MONDAY, MARCH 30

Tutorial Short Course

8:30 Registration

9:00 Opening Remarks: Richard Allen, Technical Chair
Mark Ketchen, Tutorials Chair

9:05 Challenges and Opportunities in Technology Characterization in the Sub-Wavelength CMOS Technology Era, *Kelvin Y.Y. Doong, Department Manager, Advanced Technology Product Engineering Division, TSMC*

Kelvin Yih-Yuh Doong received the B.S.E.E. degree from National Taiwan University, Taipei, Taiwan, in 1990, and the M.E.E.E. degree from Cornell University, Ithaca, NY, in 1995, and the Ph.D. degree in electronics engineering from National Tsing-Hua University, Taiwan, in 2002.

After two-years military service as an lieutenant, he joined the electrical engineering department, National Taiwan University, from 1992 to 1993 as teaching assistant and research assistant at IAMS, Academia, Sinica, from 1993 to 1994. He was a Rotary Ambassador Scholar from 1994 to 1995. He was an assistant manager of the material analysis laboratory, quality engineering division, United Microelectronics Corporation (UMC), from 1995 to 1997. In 1997, he worked for a joint-venture project between Toshiba Corporation and Worldwide Semiconductor Manufacturing Corporation (WSMC), where he was involved in developing test structure for process development and yield modeling. He joined Alogic-1, Logic Technology Division, Taiwan Semiconductor Manufacturing Corporation (TSMC), Hsinchu, Taiwan, in 1999. He has published more than 30 technical papers, holds 27 patents, and has four patents in pending. He has involved in CMOS technology development and designed 50s technology development vehicles from 0.25 um to 32-nm node. He presently is a department manager of technology deployment infrastructure program, advanced technology product engineering division, TSMC, and is working on design-for-manufacturability methodology and process characterization. His research interests include sub wave-length process integration, test vehicle design, electrical characterization, and modeling of layout dependence in CMOS, BEOL R/C modeling, and design-for-manufacturability.

Dr. Doong is a member of EDS, IEEE. He has served as a technical committee member of the IEEE International Conference on Microelectronic Test Structures since 2003. In 1996, he received “Engineer of the year” from UMC for contribution in developing focused ion beam microscopy and material analysis. In 2006, he received “R&D Innovation Award” from TSMC for recognition of developing test vehicle design platform and test structure design automation.

9:50 Coffee Break

10:05 Product Representative At Speed Test Structures for CMOS Performance and Variability Characterization, *Manjul Bhushan, STSM, IBM Systems and Technology Group*

Manjul Bhushan received a Ph.D. in physics from Clemson University. She has over 30 years of experience in basic and applied research, development, and design. Prior to joining IBM in 1997 she held university, government laboratory, and industrial positions in the areas of compound semiconductor thin-film photovoltaic cells and fabrication technology for superconducting devices used in magnetic field detection and for microwave and digital applications. She now works as a Senior Technical Staff Member in IBM’s Systems and Technology Group. Her work focuses on CMOS technology performance characterization and evaluation, and the design of test structures for process monitoring, model build, and product performance evaluation. In the area of novel test structure designs and model-to-hardware correlation she has over 20 publications and over 10 issued or pending patents.

11:05 Introduction to Spintronics - *Stuart Parkin, IBM Fellow*

Dr. Stuart Parkin is an IBM Fellow (IBM's highest technical honor) and Manager of the Magnetoelectronics group at the IBM Almaden Research Center, San Jose, California and a consulting professor in the Department of Applied Physics at Stanford University. He is also director of the IBM–Stanford Spintronic Science and Applications Center. Parkin is a Fellow of the Royal Society, the American Physical Society, the Materials Research Society, the Institute of Physics (London), the Institute of Electrical and Electronics Engineers, and the American Association for the Advancement of Science and in April, 2008 was elected a member of the National Academy of Sciences. Parkin is the recipient of numerous awards and honors including 2 honorary Ph.Ds. and Distinguished Visiting Professorships at 6 universities in Europe, Singapore and Taiwan. Most recently Parkin received the 2008 IEEE Daniel E. Noble Award for his work on MRAM and the 2008 IEEE Distinguished Lecturer Award. In July 2009 Parkin will receive the 2009 IUPAP Magnetism Prize and Neel Medal, for outstanding contributions to the science of magnetism. Parkin has authored ~360 papers and has ~70 issued patents.

12:00 Lunch

1:15 Design for Ultra-low-k1 Patterning and Manufacturing, *Dr. Puneet Gupta, UCLA*

Puneet Gupta is currently a faculty member of the Electrical Engineering Department at UCLA. He received the B.Tech degree in Electrical Engineering from Indian Institute of Technology, Delhi in 2000 and Ph.D. in 2007 from University of California, San Diego. He co-founded Blaze DFM Inc. in 2004 and served as its product architect. He has authored over 50 papers and a book chapter. He is a recipient of IBM Ph.D. fellowship and European Design Automation Association Outstanding Dissertation Award. He holds four US patents and has 9 pending. Dr. Puneet Gupta has given tutorial talks at DAC, ICCAD, WesCon, CMP-MIC and SPIE Advanced Lithography Symposium. He has served on the Technical Program Committee of ICCAD, ASPDAC, ISQED, ICCD, SLIP, DFM & Y and VLSI Design. Dr. Gupta's research has focused on building high-value bridges between physical design and semiconductor manufacturing for lowered cost, increased yield and improved predictability of integrated circuits.

2:50 Coffee Break

3:10 Optimization of Test Hardware, Test Design, and Test Structures, *TBA, Keithley Instruments*
(details not finalized)

4:05 Statistical Design: Overview and Test Structure Needs and Opportunities, *TBA*
(details not finalized)

5:00 Adjourn

6:00 Conference Reception

TUESDAY, MARCH 31

8:00 Registration

9:00 Opening Remarks: General Chair: Greg Yeric, ARM, Ltd.
Technical Chair: Richard Allen, NIST

SESSION 1: Device Characterization
Co-chairs: Michael Cresswell, NIST
and Colin McAndrew, Freescale Semiconductor

9:10 1.1 **Using High Precision On-Wafer Backend Capacitor Mismatch Measurements using a Benchtop Semiconductor Characterization System,** *H. Tuinhout and F. van Rossem*, NXP-TSMC Research Center, Eindhoven, The Netherlands and *University of Twente, Enschede, The Netherlands*

This paper describes a benchtop semiconductor characterization system based measurement solution for direct on-wafer mismatch characterization of pairs of pF range backend capacitors. By using abundant averaging and DUT-1-2-1-2 se-quencing through prober subsite stepping, the system reaches sub-10 ppm STR levels. To our knowledge this is the best reported value for on-wafer statistical capacitance mismatch measurements.

9:30 1.2 **Static Noise Margin Evaluation Method Based on Direct Polynomial-Curve-Fitting with Universal SRAM Cell Inverter TEG Measurement,** *K. Nakamura, K. Noda and H. Koike*, Kyushu Institute of Technology, and *Fukuoka Industry, Science & Technology Foundation, Japan*

A new method to evaluate the Static Noise Margin (SNM) for leading-edge CMOS SRAM development is proposed. This method includes: (1) direct measurement of the inverter DC transfer curves using a "Universal SRAM Cell Inverter TEG (USCIT)" with arbitrary transistor ratios, (2) curve-fitting of the measured data to polynomial functions in a 45-degree rotated space, and (3) a database of the polynomial coefficients to evaluate and optimize the SNM by a simple algebraic operation. The SNM values obtained using this method are in good agreement with the measured SRAM operations.

9:50 1.3 **Addressable Arrays Implemented with One Metal Level for MOSFET and Resistor Variability Characterization,** *M.B. Ketchen, M. Bhushan* and G. Costrini*, IBM Research, T.J. Watson Research Center, Yorktown Heights, NY and *IBM Systems and Technology Group, Hopewell Junction, NY*

Addressable array test structures for rapid collection of statistical distributions of MOSFET parameters and parasitic resistances are described. A unique feature of these designs is that they require only one level of metal, yet are compact for placement in the scribe line for early process learning. MOSFET measurements are made over full range of I-V characteristics including leakage currents of individual devices in the subthreshold region. A modular approach for test structure integration and parallel testability enables high efficiency in design and data acquisition.

10:10 1.4 **Accurate Time Constant of Random Telegraph Signal Extracted by a Sufficient Long Time Measurement in Very Large-Scale Array TEG,** *T. Fujisawa, K. Abe, S. Watabe, N. Miyamoto, A. Teramoto, S. Sugawa, and T. Ohmi, Tohoku University, Japan*

For the development of processes suppressing RTS noise, it is required the exact phenomena of RTS are understood. The statistical extraction of the accurate time constant in Random Telegraph Signal noise (RTS) is useful to obtain the energy level and/or distance between traps and Si/SiO2 interface. In this paper, we demonstrated the statistical and accurate measurement method of the time constant of RTS by a sufficient long time measurement in very large-scale array TEG, and also demonstrated the relationship of $\langle \tau_c \rangle / \langle \tau_e \rangle$ and amplitude of RTS for changing of some temperature or drain current by using developed method.

.

10:30 **BREAK**

SESSION 2: MEMS/Sensors
Co-chairs: Yoshio Mita, University of Tokyo
and Anthony Walton, University of Edinburgh

11:00 2.1 **Extracting Resistances of Carbon Nanostructures in Vias,** *W. Wu, S. Krishnan, K. Li, X. Sun, R. Wu and C.Y. Yang, Santa Clara University, Santa Clara, CA*

This paper presents a currentsensing technique to extract the resistances of carbon nanostructures in via interconnects. Test structures designed and fabricated for via applications contain carbon nanofiber (CNF)-metal composites encapsulated in SiO2. Electrical characterization of single CNFs

is performed using an atomic force microscope (AFM). This technique yields a metal-CNF contact resistance of 6.4 kΩ and a lowest CNF resistivity of 1.89e-4 Ω-cm.

11:20 2.2 **Demonstration of a Submicron Damascene Cu/Low-k Mechanical Sensor to Monitor Stress in BEOL Metallisation,** *C.J. Wilson, K. Croes*, Z. Tokei*, G.P. Beyer*, A.B. Horsfall, and A.G. O'Neill, Newcastle University, Newcastle, United Kingdom and *IMEC, Leuven, Belgium*

This work reports the results of a mechanical sensor to monitor stress in 100nm critical dimension Cu interconnects. Existing methodology developed for larger scale Al sensors is discussed and evaluated for relevant Cu/SiO2 and Cu/Low-k integration schemes. New sensor release methods are then developed and the Cu sensor demonstrated in single and dual damascene technology for the first time.

11:40 2.3 **Test Structure to Extract Circuit Models of Nanostructures Operating at High Frequencies,** *F.R. Madriz, S. Krishnan, X. Sun, and C.Y. Yang, Santa Clara University, Santa Clara, CA*

We describe a method for obtaining equivalent circuit models to characterize the high-frequency electrical transport of 1-D nanoscale systems. This method utilizes a ground-signal-ground, GSG, test structure whose scattering parameters (S-parameters) are determined using a simple lumped-element circuit model. The open test structure exhibits lower transmission characteristics than previously reported structures, allowing detection of coupling capacitance values smaller than 1 fF.

12:00 2.4 **Test Chip to Evaluate Measurement Methods for Small Capacitances,** *J.J. Kopanski, M. Yaqub Afridi, C. Jiang, and C.A. Richter, National Institute of Standards and Technology, Gaithersburg, MD*

We designed and fabricated a test chip to help us evaluate the performance of new approaches to measurement of small capacitances (femto-Farads to atto-Farads range). The test chip consists of an array of metal-oxide-semiconductor capacitors, metal-insulator-metal capacitors, and series of systematically varying capacitance structures directly accessible by an atomic force microscope probe. Nominal capacitances of the test devices range from 0.3 fF (10-15 F) to 1.2 pF (10-12 F). Measurement of the complete array of capacitances using an automatic probe station produces a “fingerprint” of capacitance values from which, after correcting for pad and other stray capacitances, the relative accuracy and sensitivity of a capacitance measurement instrument or circuit can be evaluated.

12:20 ICMTS LUNCHEON

SESSION 3: Matching

Co-chairs: Hans Tuinhout, NXP
and Mark Poulter, National Semiconductor Corp.

1:30 3.1 **An Enhanced Model for Thin Film Resistor Matching,** *T.G. O'Dwyer and M.P. Kennedy*, Analog Devices B.V., Limerick, Ireland and *University College, Cork, Ireland*

The standard model to estimate the required thin film resistor geometry to achieve a particular matching target has been based on an assumed linear relationship between the variance of the mismatch and the reciprocal of the resistor area (ignoring distance effects). This paper examines a particular resistor process and demonstrates that, while the standard model gives a reasonable first order approximation, it can be improved upon. An improved model is derived based on a random variables approach to the three-dimensional geometry factors involved. Measured data confirms the superiority of the new model and provides insights into the underlying error sources.

1:50 3.2 **Application of Matching Structures to Identify the Source of Systematic Dimensional Offsets in GHOST Proximity Corrected Photomasks,** *S. Smith, A. Tsiamis, M. McCallum*, A.C. Hourd**, J.T.M. Stevenson, and A.J. Walton, The University of Edinburgh, Edinburgh, United Kingdom, *Nikon Precision Europe, Livingston, United Kingdom and **Compugraphics International Ltd., Glenrothes, United Kingdom*

The effects of the GHOST proximity correction process on chrome-on-quartz photomasks can prove difficult to quantify and so they are not routinely characterised. This paper presents a methodology for addressing this issue using electrical test structures designed to measure dimensional mismatch. In the past these have been used successfully to characterise standard GHOSTed photomasks, which displayed systematic offsets that were not seen on an unGHOSTed mask using the same design. In order to investigate this further, a second mask was fabricated

using a variation of the GHOST process which increased the resolution of the secondary exposure to be the same as the primary pattern. This enabled the source of the previously observed systematic offset to be determined as test structures on the new mask did not show the same overall dimensional bias. However, the range of mismatch in some of the structures was increased as a result of the new process.

2:10 3.3 **An Analysis of Temperature Impact on MOPSFET Mismatch,** *S. Mennillo, A. Spessot, L. Vendrame, and L. Bortesi, Numonyx, Agrate Brianza, Italy*
Summarizing the results collected on several technologies, we have studied the impact of temperature on MOSFET mismatch, highlighting the improvement of current gain matching properties with temperature, suggesting a possible physical explanation to this phenomenon and proposing a BSIM3 model implementation for Monte Carlo mismatch simulations.

2:30 3.4 **MOSFET Mismatch Measure Improvement Using Kelvin Test Structures,** *C.M. Mezzomo, M. Marin and G. Ghibaudo*, STMicroelectronics, Crolles, France and *IMEP-LAHC, Grenoble, France*
A mismatch test structure in standard pair configuration using Kelvin method is introduced to better estimate MOSFET local electrical fluctuations. The impact of extern access connections on Vth, b and Id mismatch extraction is investigated. We conclude that the variability of access connections does not impact Vth mismatch whereas drain current matching is underestimated without Kelvin method.

SESSION 4: Poster Presentations
2:50 p.m. - 3:30 p.m.
Co-chairs: Willie Sansen, KU Leuvenp
and Richard Allen, NIST

4.1 **Characterization of a 65nm CMOS Technology for Microprocessor Development using Produce Embedded Test Structures,** *S. Sundararajan, S. Alam*, B. Ho, S. Venkaktkrishnan, M. Weling**, and P. Dixit, Sun Microsystems, CA, *AMD, TX, and **Cadence Design Systems, CA*
Product yield enhancement and reliability development for semiconductor technologies are closely linked to the use of process diagnostic test vehicles to characterize product relevant technology features. Aggressive scaling of microprocessor CMOS technologies has led to a separate discipline related to the design of product embeddable test and characterization testchips termed PCMs (process control monitor) for improving yield, performance, and power during multiple stages of the product lifecycle. In this article we will present an implementation of such a testchip to characterize an advanced microprocessor class 65nm CMOS technology at the product level. Additionally we were also demonstrate the correlation obtained for DC and AC characteristics of transistors and interconnect monitoring test structures placed on this test vehicle and their use in analyzing performance, power characteristics of a 65nm high performance microprocessor.

4.2 **A Test Structure for Spectrum Analysis of Hot-Carrier-Induced Photoemission from Scaled MOSFETs under DC and AC Operations,** *T. Matsuda, T. Maezawa, H. Iwata, and T. Ohzone*, Toyama Prefectural University and *Dawn Enterprise, Japan*
A test structure with a wide channel width for analysis of hot-carrier-induced photoemission is presented and spectrum changes for 90 nm MOSFETs under DC (direct current) and AC (alternating current) operation are discussed. Comparing with DC operation, photon counts for higher photon energy increase under AC operation, and spectrum curves change with rise and fall time of gate pulse. The overshoots of drain voltage at the transition timing generate hot carriers with higher energy due to large electric field near drain region, which raise a possibility of a reliability issue related to hot carrier effects in LSIs.

4.3 **Application of a Micromechanical Test Structure to the Measurement of Stress in an Electroplated Permalloy Film,** *S. Smith, N. Brockie, J.G. Terry, A.B. Horsfall*, G. Pringle**, A. O'Hara**, and A.J. Walton, The University of Edinburgh, Edinburgh, United Kingdom, *Newcastle University, Newcastle, United Kingdom and **Memsstar Technology, Livingston, United Kingdom*
Suspended microrotating test structures designed to measure the stress in thin, surface micromachined films have been applied to the production of thick layers of electroplated permalloy (NiFe alloy). This process has particular application in the production of magnetic MEMS components and devices. It is extremely important to characterise the stress in such materials, especially where these films are to be used on wafers with underlying integrated circuitry as it is

well known that the matching of transistors can be affected by mechanical strains induced by interconnect features passing above.

4.4 **Measurement of MOSFET C-V Curve Variation using CBCM Method,** *K. Tsuji, K. Terada, T. Tsunomura*, and A. Nishida*, Hiroshima City University, Hiroshima, Japan and *MIRAI-Selete, Tsukuba, Japan*
The test circuit, in which the cells including CBCMs (Charge-Based Capacitance Measurements) are arrayed in matrix shape, is developed to measure MOSFET capacitance variation. By adjusting the bias condition of the test circuit, it is able to obtain C-V curves for many MOSFETs. In addition to measuring MOSFET capacitance variation, an extraction of threshold voltage variation is attempted and then, it presents an availability of this circuit.

4.5 **Array Test Structure for Ultra-Thin Gate Oxide Degradation Issues,** *K.M. Hafkemeyer, A. Domdey, D. Schroeder and W.H. Krautschneider, Hamburg University of Technology, Hamburg, Germany*
An array test structure for highly parallelized measurements of ultra-thin MOS gate oxide failures caused by degradation is presented. The test structure allows for voltage stress tests of several thousand NMOS devices under test (DUTs) in parallel to provide a large and significant statistical base regarding soft as well as hard breakdown and stress induced degradation of transistor parameters. The array has been fabricated in a standard 130 nm CMOS technology. As mixed-mode technologies provide thin as well as thick oxide MOS transistors, different gate oxide thicknesses have been chosen for DUTs and digital control logic which gives the possibility to stress the DUTs with high gate voltages.

4.6 **Non-Contact, Pad-less Measurement Technology and Test Structures for Characterization of Cross-Wafer and In-Die Product Variability,** *G. Steinbrueck, J.S. Vickers, M. Babazadeh, M. Pelella, and N. Pakdaman, tau-Metryx, Inc., Santa Clara, USA*
Monitoring and controlling cross-wafer and in-die variability have been recognized as the dominant and escalating factors for the successful commercialization of modern-day integrated circuit products utilizing advanced semiconductor manufacturing. In this paper we present a performance based metrology (PBM) and measurement technology to further close the information gap that currently exists between the design, process integration, and manufacturing to control variability.

4.7 **Test Structure for High-Voltage LD-MOSFET Mismatch Characterization in 0.35 um HV-CMOS Technology,** *W. Posch, M. Christian and E. Seebacher, austriamicrosystems AG, Unterpremstatten, Austria*
A characterization setup for high voltage (HV) LD-MOSFET mismatch determination is presented. The according test chip was successfully realized in 0.35 um HV-CMOS technology. Devices are aligned in rows and columns for gate and drain bias multiplexing and special HV-switches for voltages up to 50V are controlled by externally generated digital signals. Automatic DC measurements can be performed on up to 4992 HV-NMOSFETs, providing data for both, short and long distance matching characterization.

4.8 **Automated Test Structure Generation for Characterizing Plasma-Induced Damage in MOSFET Devices,** *T. Zwingman, A.J. West and A. Gabrys, National Semiconductor Corp., Santa Clara, CA*
Test structures used to study the effects of plasma induced damage are complex and time intensive to design; performance problems due to poorly designed components of the structure often confound the desired result. This paper presents a parameterized and hierarchical antenna test structure template that enables the user to characterize the test structure performance and identify safe design guidelines early in process development. The template is implemented in a system that automates structure generation, placement, routing, and test plan development.

3:30 - 4:00 **Exhibitor Presentations**

4:00 - 6:00 **Poster Session**

WEDNESDAY, APRIL 1

8:00 **Registration**

SESSION 5: Process Characterization I
Co-chairs: Christopher Hess, PDF Solutions
and Kelvin Doong, TSMC

8:30 5.1 **Advanced Method for Measuring Ultra-Low Contact Resistivity between Silicide and Silicon based on Cross-Bridge Kelvin Resistor,** *T. Isogai, H. Tanaka, A. Teramoto, T. Goto, S. Sugawa, and T. Ohmi, Tohoku University, Sendai, Japan*
In order to evaluate low contact resistivity precisely, we have developed a new test structure based on Cross-Bridge Kelvin Resistor. In this structure, the misalignment margin, which has been reported to limit lower-detectable values of contact resistivity because of lateral current crowding effect, can be as small as possible. Furthermore, we had successively derived the theoretical expressions to ensure the validity of the newly developed method and compared them to the experimental values. This method will enable us to evaluate the contact resistivity in the sub-10^{-8} Ωcm^2 region.

8:50 5.2 **A Test Structure for Statistical Evaluation of Characteristics Variability in a Very Large Number of MOSFETs,** *S. Watabe, S. Sugawa, K. Abe, T. Fujisawa, N. Miyamoto, A. Teramoto, and T. Ohmi, Tohoku University, Sendai, Japan*
In this paper, we have proposed and developed a test structure for evaluating electrical characteristics variability of large number of MOSFETs in very short time, though the test structure is very simple circuit. We demonstrated that the electrical characteristics in over one million MOSFETs such as threshold voltages, subthreshold swings (S-Factor), random telegraph signal noise, and so on, are measured, and that the measured results are very efficient in developing processes, process equipments and device structure which suppress variability.

9:10 5.3 **Estimating MOSFET Leakage from Low-cost, Low-resolution fast Parametric Test,** *T. Uezono, R. Lindley, A. Swimmer, S. Winters, R. Vallishayee, S. Saxena, PDF Solutions, Richardson, TX*
A method of estimating MOSFET off-state current (I_{off}) using low-cost, low-resolution fast parallel parametric test is introduced. The method relies on measuring subthreshold slope and using it to estimate I_{off}. Measurement results of individual transistors show very good agreement between measured I_{off} and I_{off} estimated using our approach. For transistor array test structures, where unselected devices can add additional noise in subthreshold measurement, the estimated off current has very high correlation with the measured I_{off} providing a good indicator of I_{off} even though it does not match the exact I_{off}. The high correlation is used to derive calibration factors which are then used to estimate individual transistor I_{off} from array test structures. This allows statistical characterization of transistor off-state current, which can be utilized for IDDQ estimation and yield improvement.

9:30 5.4 **Test Structures Utilizing High-Precision Fast Testing for 32nm Yield Enhancement** *M. Karthikeyan, L. Medina and E. Shiling, IBM Systems and Technology Group, Hopewell Junction, NY*
We describe the development and use of various test structures for 32nm yield enhancement. These DC test structures are tested in parallel mode on a functional tester using a special Pico-Amp measurement card. This new test method provides a measurement accuracy of up to ±10 pA along with a 9x reduction in test time over conventional parametric testing. The large critical area enables reliable estimation of defect densities by failure mechanism.

9:50 BREAK

SESSION 6: Parameter Extraction
Co-chairs: Larg Weiland, PDF Solutions
and Hi-Deok Lee, Chungham National University

10:20 6.1 **Efficient Characterization Methodology of Gate-Bulk Leakage and Capacitance for Ultra-Thin Oxide Partially-Depleted (PD) SOI Floating Body CMOS,** *D. Chen, R. Lee, U.C. Liu, G.S. Lin, M.C. Tang, C.S. Yeh, and S.C. Chien, United Microelectronics Corp., Hsinchu, Taiwan,*
For the first time, an efficient methodology to accurately characterize the gate-bulk leakage current (Igb) and gate capacitance (Cgg) of PD SOI floating body (FB) devices was proposed and demonstrated in 40-nm PD SOI devices with ultra-thin oxide EOT 12A. By applying the RF testing skill for the proposed SOI test patterns, we can eliminate properly the parasitic elements due to the opposite poly gate type co-existence in the SOI T-shape body-tied (BT) device and accurately

characterize and model SOI FB Igb and Cgg behavior for BSIMSOI4.0 model setup. Igb impact on the history effect was analyzed by BSIMSOI4.0 model. Improvement of more than 3% simulation accuracy for history effect was demonstrated.

10:40 6.2 **Parameter Extraction for the PSP MOSFET Model by the Combination of Genetic and Levenberg-Marquardt Algorithms,** *Q. Zhou, W. Yao, W. Wu, X. Li, Z. Zhu, and G. Gildenblat, Arizona State University, Tempe, AZ*

Based on the combination of the genetic and Levenberg-Marquardt algorithms, a method is developed to perform both local and global parameter extraction for the industry standard PSP compact MOSET model. This technique advances the earlier version of the automatic parameter extraction method by increasing computational efficiency by an order of magnitude. With the parameters extracted by this technique, the PSP compact model is shown to provide good fit for the 65 nm technology mode.

11:00 6.3 **Characterization and Modeling of Mechanical Stress in Silicon-based Devices,** *A. Spessot, A. Colombi, G.P. Carnevale, and P. Fantini, Numonyx, Agrate Brianza, Italy*

In this paper we show a self-consistent methodology to characterize the stress-induced mobility variation in silicon-based devices. The synergy among different experimental techniques (the application of an external mechanical stress and the measure of the process-induced stress), theoretical calculations (based on the finite elements method and the band structure calculation), and silicon validation (given by particular sets of test structures) is the strength of the characterization tool we propose.

11:20 6.4 **Improved Parameter Extraction Procedure for PSP-Based MOS Varactor Model,** *Z. Zhu, J. Victory*, S. Chaudhry**, L. Dong**, Z. Yan**, J. Zheng**, W. Wu, X. Li, Q. Zhou, P. Kolev^, C. McAndrew^^, and G. Gildenblat, Arizona State University, Tempe, AZ, *Sentinel IC Technologies, Irvine, CA, **Jazz Semiconductor, Newport Beach, CA, ^formerly with RFMD, San Diego, CA and ^^Freescale Semiconductor, Tempe, AZ*

We present an improved approach for extracting parameters for the CMC standard MOS varactor model MOSVAR. This submission advances previous work which made several simplifying assumptions affecting the resulting model accuracy. The new technique is verified with silicon data for three technology nodes (180nm, 130nm and 65nm) and is also used to validate the P-gate/P-well tunneling current sub-model.

11:40 CONFERENCE LUNCH

SESSION 7: CD Metrology

Co-chairs: Loren Linholm
and Dieter Schroder, Arizona State University

1:30 ICMTS 2010 Presentation

1:40 7.1 **Nanomechanical Test Structure for Optimal Alignment in Stencil-Based Lithography,** *M. Sansa, J. Arcamone, J. Verd*, A. Uranga*, G. Abadal*, E. Lora-Tamayo, N. Barniol*, M.A.F. van den Boogaart**, J. Brugger**, and F. Perez-Murano, Institute de Microelectronica de Barcelona CNM-IMB, Barcelona, Spain, *ETSE-UAB, Barcelona, Spain and **EPFL, Lausanne, Switzerland*

Shadow masking (also known as nanostencil lithography, SL) is a well known technique to fabricate patterns on a surface. It is a versatile method that can be used in a variety of applications. There has been recently a strong interest regarding the use of shadow masks, mostly related to combinatorial materials science, organic based device fabrication, as well as rapid prototyping of nanoscale structures, using dynamic or quasi-dynamic stencil deposition.

2:00 7.2 **Electrical Test Structures for Investigating the Effects of Optical Proximity Correction,** *A. Tsiamis, S. Smith, M. McCallum*, A.C. Hourd**, J.T.M. Stevenson, and A.J. Walton, The University of Edinburgh, Edinburgh, United Kingdom, *Nikon Precision Europe, Livingston, United Kingdom and **Compugraphics International Ltd., Glenrothes, United Kingdom*

Electrical test structures have been designed which allow the characterisation of corner serif forms of optical proximity correction. The structures measure the resistance of a conducting track with a right angled corner. Varying amounts of OPC can be applied to the outer and inner corners of the feature and the effect on the resistance of the track can be investigated. A prototype test mask has

been fabricated which contains test structures suitable for on-mask electrical measurement. The same mask was used to print the structures using a step and scan lithography tool so that they can be measured on-wafer. Results from the structures at wafer level will provide a great deal of information about the effects of OPC and the impact it has on the final printed features.

2:20 7.3 **Mapping the Edge-Roughness of Test Structure Features for Nanometer-Level CD Reference-Materials,** *M.W. Cresswell, M. Davidson*, R.A. Allen, W.F. Guthrie, M. Bishop**, and G.I. Mijares, National Institute of Standards and Technology, Gaithersburg, MD, *Special Research Corp., Palo Alto, Ca and **SEMATECH, Austin, TX*

The motivation for this work was reducing the uncertainties attributed to the traceable linewidths of CD reference features embedded in multi-CD test structures to below 1nm. The problem to date has been accumulating CD measurements at rates sufficient to enable meaningful fabrication-process optimization. The new approach reported here is demonstrating state-of-art SEM image-analysis software to the characterization of as-fabricated reference-material test-structure samples.

2:40 BREAK

SESSION 8: RF

Co-chairs: Franz Sischka, Agilent Technologies
and Kevin McCarthy, University College, Cork

3:10 8.1 **S-Parameter-based Modal Decomposition of Multiconductor Transmission Lines and its Application to De-Embedding,** *S. Amakawa, K. Yamanaga, H. Itoh, T. Sato, N. Ishihara, and K. Masu, Tokyo Institute of Technology, Yokohama, Japan*

Theory and numerical experiments are presented of modal decomposition of scattering matrices of multiconductor transmission lines (TLs). In effect, *n* coupled TLs are decomposed into *n* independent ones. Its use is demonstrated by applying it to thru-only de-embedding of 4 coupled TLs (synthesized data) and 2 coupled TLs (measurement data from a 0.18 *μ*m-CMOS chip). The proposed de-embedding method could, among others, greatly facilitate accurate characterization of on-chip or on-board bus lines.

3:30 8.2 **Characterization and Model Parameter Extraction of Symmetrical Centre Tapped Inductor using Build in Mixed Mode and Pure Differential S-Parameters,** *F. Gianesello, Y. Morandini, S. Boret, and D. Gloria, STMicroelectronics, Crolles, France*

In this paper, we report for the first time a comparison between true balanced and build-in mixed mode measurements of symmetrical centre tapped inductor in RF CMOS 130 nm technology. To achieve this comparison, dedicated differential test structures and de-embedding methodology are proposed. We highlight that with linear assumption, a single-ended characterization which combines the mathematically results is sufficient to obtain balanced response. Moreover, the build-in mixed parameters allows extracting a scalable model more easily than with single ended parameters, giving access to new parameter such as mutual inductance (which was not determine experimentally up to now). We discuss here the extracting methodology and the potentiality for passive components advanced modeling.

3:50 8.3 **In-Situ Silicon Integrated Tuner for Automated on-Wafer MMW Noise Parameters Extraction of Si HBT and MOSFET in the Range of 60 - 110GHz,** *Y. Tagro, D. Gloria, S. Boret, Y. Monandini, and G. Dambrine*, STMicroelectronics, Crolles, France, and *IEMN, Villeneuve d'ascq, France*

In this paper, for the first time, Silicon integrated tuner is presented aiming silicon transistor (HBT, MOSFET) MilliMeter Wave (MMW) noise parameters (NFmin, Rn, Gopt) extraction through multi-impedance method. This Tuner is directly integrated in On-wafer tested transistor test structure. Design, electrical simulation and MMW measurement of the Tuner are described showing capability from 60GHz up to 110GHz for CMOS and BiCMOS sub 65nm technologies characterization. [Γ] of 0.88 have been achieved at the DUT input in the considered frequency range and Tuner insertion losses are less than 20 dB.

Conference Banquet at the Ronald Reagan Presidential Library

@4:40 p.m. Buses load in front of the hotel

5:00 p.m. Tour of Library, Air Force One and Banquet

THURSDAY, APRIL 2

8:30 Registration

SESSION 9: Process Characterization II
Co-chairs: Brad Smith, Freescale Semiconductor
and Hughes Brut, STMicroelectronics

9:00 9.1 Four Point Probe Structures with Buried Electrodes for the Electrical Characterization of Ultrathin Conducting Films, *A.W. Groenland and. R.A.M. Wolters, A.Y. Kovalgin, and J. Schmitz, University of Twente, Enschede, The Netherlands and *NXP-TSMC, Eindhoven, The Netherlands*
Test structures for the electrical characterization of ultrathin conductive (ALD) films are presented based on buried electrodes on which the ultrathin film is deposited. The work presented here includes test structure design and fabrication, as well as the electrical characterization of ALD TiN films down to 4 nm. It is shown that these structures can be used successfully to characterize sub 10 nm films.

9:20 9.2 Metal and Dielectric Thickness: A Comprehensive Methodology for Back-End Electrical Characterization, *L. Bortesi and L. Vendrame, Numonyx, Agrate Brianza Agrate, Italy*
Process variation including interconnect is becoming more and more important since technology is scaling down and increases its complexity. Capacitances and resistances are strongly dependent on the geometrical configuration so it is really important to have an accurate description and monitoring of the technology for what concern the metal and dielectric thickness. Interconnect parasitic modelling by means of LPE tool or semi-analytic approximation can't neglect the impact of metal (dielectric) thickness variations. The focus of this work is to provide a methodology to electrically measure metal and dielectric thicknesses, mandatory for a useful characterization and control of a technology. Furthermore, due to silicon cost constraints, particular attention has been taken to develop a system compatible with a saw-line insertion, easy to characterize at parametric testing and portable across technology nodes.

9:40 9.3 A Test Structure for Assessing Individual Contact Resistance, *F. Liu and K. Agarwal, IBM Austin Research Lab., Austin, TX*
This paper presents a scalable contact resistance measurement structure. The structure has modest pin requirement and can easily accommodate tens of thousands of DUTs. The measurement results from a 65nm CMOS technology are also been presented.

10:00 9.4 Fast Embedded Characterization of FEOL Variations in MOS Devices, *F. Rigaud, STMicroelectronics, Rousset, France*
The objective of this paper is to present a test chip based on embedded Ring Oscillators (RO) measurement with its associated extraction algorithm to characterize length and width variations and to discriminate them from other FEOL variations. A brief overview of the structure, designed in a ST-Microelectronics 90nm technology, is given with emphasis on the ROs geometry with their biasing conditions and the measurement circuit. Comparison of simulated values versus estimated ones is given and confirms the ability of the structure to characterize FEOL variations. MOS width and length are well estimated regardless the other FEOL deviation that can be also detected.

10:20 BREAK

SESSION 10: Capacitance
Lee Stauffer, Keithley Instruments
and Satoshi Habu, Agilent Technologies Japan, Ltd.

10:50 10.1 Benefit of Direct Charge Measurement on Interconnect Capacitance Measurement, *Y. Miyake and M. Goto, Agilent Technologies International Japan, Ltd., Tokyo, Japan*
This paper discusses application of direct charge measurement (DCM) on characterizing on-chip interconnect capacitance. Measurement equipment and techniques are leveraged from Flat Panel Display testing. On-chip active device is not an essential necessity for DCM test structure. With DCM, it is easy to implement parallel measurements. Femto-Farad measurement sensitivity without having on-chip active device is achieved. Measurement results of silicon and glass substrates, including parallel measurements, are presented.

11:10 4K-cells Resistive and Charge-Base-Capacitive Measurement Test Structure Array
10.2 (R-CBCM-TSA) for CMOS Logic Process Development, Monitor and Model, *K.Y.Y. Doong, L.J. Hung, S.-C. Lin, H.C. Tseng, A. Dagonis, and S. Pan, Taiwan Semiconductor Manufacturing Co., Hsinchu, Taiwan*

To maximize the design efficiency of the test chip area and maintain the high accuracy measurement requirement of resistors and capacitors, a 4K-cells resistive and charge-base capacitive test structure array is designed for CMOS logic process development, monitor and model.

10:30 Practical Considerations for Measurements of Test Structures for Dielectric
10.3 Characterization, *W. Chen, K.G. McCarthy, and A. Mathewson, University College, Cork, Ireland*

This paper presents a method for measuring the complex permittivity of dielectric material on a dielectric/metal stack. A series of circular capacitor and transmission line test structures are designed and fabricated. The methodology has been verified by measuring the dielectric constant of a known SiO_2 layer using Capacitance-Voltage (C-V) measurement and scattering parameter (S-parameter) measurements. The combination of C-V measurement and S-parameter measurement is shown to be suitable for characterization of dielectric material on the complex cross-sections

11:50 Test Structure Design, Extraction, and Impact Study of FEOL Capacitance
10.4 Parameters in Advanced 45nm Technology, *S. Ekbote, P. Sadagopan, W. Sy, R. Zhang, Y. Chen, and M. Han, Qualcomm, Inc., San Diego, CA*

In this paper we describe test structure designed to extract the key transistor capacitances which have significant impact on circuit performance in state-of-the-art low power technology nodes. We present extracted capacitance correlation to SPICE simulation results which show excellent matching. Further we extend this analysis to correlate transistor capacitance data to actual circuit delay. This paper clearly establishes that accurate modeling of transistor parasitic is essential in predicting circuit performance.

12:10 CLOSING REMARKS