ICMTS 98 Tutorial and Technical Program

March 23-26, 1998

Kanazawa Citymonde Hotel

Kanazawa, Japan

CONTENTS

CHAIRMAN'S LETTER

On behalf of all the committee members, I would like to invite you to the 1998 International Conference on Microelectronic Test Structures (ICMTS1998) in Japan. The conference is sponsored by IEEE Electron Device Society in cooperation with Institute of Electronics, Information and Communication Engineers of Japan and Applied Physics Society of Japan. This is the 11th ICMTS as an international conference and the third one to be held in Japan.

The purpose of the conference is to bring together researchers and engineers for discussing microelectronic test structures and their applications for characterization of device matching, critical dimension, parameter extraction, yield, reliability, interconnection and so on.

The technical program consists of 7 sessions containing 41 contributed papers including 16 posters, 1 session for exhibitors' presentations and 3 sessions dedicated for invited papers. The details will be found in the program booklet. The conference starts on March 24, preceded by a one-day Tutorial Short Course on March 23. The tutorial course will be the best place for young researchers to learn fundamentals on microelectronic test structures so as to catch up advanced topics in this field. There is also an equipment exhibition relating to advanced test structure measurements.

Special features of ICMTS 1998 are invited papers to review and forecast the current and future status of developing the next generation wafer and lithography technologies in Japan and overseas.

The conference will be held at Kanazawa Citymonde Hotel in Kanazawa. Kanazawa is one of the most beautiful cities in Japan, originally established as a castle town of Maeda, and feudal load, in 16th Century. The castle park, Kenroku-en, and many other historical spots are within a walking distance from the hotel. Kanazawa is an exceptional city, cultural and historical values of which prevented the U. S. military from bombing it in the World War II. Thanks to the thoughtful decision, many old structures have been preserved in Kanazawa, as they were.

I am sure that ICMTS 1998 at Kanazawa will give all the attendees significant technical experiences. It will give a real understanding about the Japanese classic cultures, especially to foreign attendees as well. We are looking forward to seeing you at Kanazawa!

Sincerely,

Kunihiro Asada

General Chairman

GENERAL INFORMATION

Conference Information

The IEEE Electron Devices Society is sponsoring the 1998 International Conference on Microelectronic Test Structures to be held in cooperation with The Institute of Electronics, Information and Communication Engineers (IEICE), and The Japan Society of Applied Physics (JSAP). The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The Conference will be preceded by a one-day Tutorial Short Course on Microelectronic Test Structures.

Presentation

The official language of the conference is English and it will be used for all presentations, printed materials, slides and OHP transparencies. A overhead projector and 35mm slide projector for 50mm x 50mm mount will be available for use at the presentation. All speakers are requested to report to the speaker's registration desk located in front of the conference room to arrange their slides in the carousels and preview them.

Best Paper Award

One paper presented will be selected for the Best Paper Award. Presentation of the award will be made at the ICMTS 1999.

Conference Proceedings

The IEEE ICMTS 1998 will publish a proceedings. One copy of the proceedings is included in the registration fee. Additional copies will be available at the Conference for 5,000yen per copy for members of the IEEE or IEICE or JSAP, 7,000yen per copy for non-members, or from the IEEE after the conference.

On-site registration schedule

On-site registration for the conference will be conducted in the Lobby (1st floor) at Kanazawa Citymonde Hotel as follows:

Monday,	March 23	9:00 - 17:30
Tuesday,	March 24	8:15 - 17:30
Wednesday,	March 25	8:30 - 17:30
Thursday,	March 26	8:50 - 11:00

Conference registration fees

A registration form is included in the center of this booklet. Below are the conference fees for early, late, and on-site registrants.

Early Registration:(Postmarked by February 1, 1998)

	Member*	Non Member	Student**
Tutorial	18,000yen	21,000yen	8,000yen
Technical Sessions	35,000yen	43,000yen	25,000yen

Late Registration: (Registered after February 1, 1998)

Tutorial	25,000yen	28,000yen	10,000yen
Technical Sessions	38,000yen	46,000yen	26,000yen

On-site Registration: (Registration at the Conference)

Tutorial	31,000yen	34,000yen	13,000yen
Technical Sessions	40,000yen	48,000yen	28,000yen

* Must be a member of the IEEE or IEICE or JSAP.

**To qualify for reduced student rates, you must be a Student Member, full-time student, not be self-employed, nor working part or full time at a facility or corporation.

Registration fees include admittance to technical sessions, equipment exhibits, morning and afternoon coffee breaks, reception, conference banquet, one copy of the proceedings.

Payment of the registration fees

Registration fees should be payable to the ICMTS 1998 and must be in **Japanese Yen only.**

(1) Bank Transfer in Yen to "ICMTS 1998". Account at the Tokyo Mitsubishi Bank, Toyonaka Branch A/C No. 0550612

(2) Bank Check in Yen payable to the order of "ICMTS 1998. Personal Checks are not acceptable.

(3) Credit Card in Yen: MasterCard, VISA, Diner's Club, American Express**

(4) Cash in Yen at the conference registration desk.

**For credit card payments of registration fees, add 5% to the registration fee for handling charges.

Cancellation

Due to advance financial commitments, refunds of registration fees requested after March 1, 1998, cannot be guaranteed. 5,000yen processing fee will be withheld from all refunds. Requests for refunds of registrations canceled after March 1 will be considered after the conference.

Messages

If you need to be contacted during the Conference Sessions, a message can be left at +81-762-24-5555 (Ext. ICMTS Secretariat) between the hours of 9:00am and 6:00pm, March 23, 24, 25, and from 9:00am to 12:00pm on March 26. Messages will be placed on a Message Board beside the registration desk.

Banquet

The conference banquet will be held on Wednesday evening, March 25 at 7:00pm. Conference registration fees include one banquet ticket. Guest ticket will be available for sale at the registration desk.

Kanazawa Information

Kanazawa is one of Japan's foremost castle towns. The city boasts many places of historic and aesthetic interest, such as the splendid Kenrokuen, known as one of the three most beautiful gardens in Japan, and Ishikawa-mon, the commanding gate to the old castle grounds. Since the city has been completely untouched by war and thus retains much of its historic beauty. While preserving its precious heritage, Kanazawa has developed into a thoroughly charming modern city.

Climate and Clothing

The temperature in Kanazawa during the conference period will range between 8^{o}C (46^{o}F) at night and 18^{o}C (64^{o}F) during the day. The weather is, however, often unpredictable during this season. The average humidity is 63%, so light clothing and a sweater or light coat is recommended. Hotels and buildings are fully air-conditioned.

Transportation

From Kansai Int'l Airport

1. Kansai Airport — JR Haruka 50min. — Shin-Osaka Station — JR Raicho (Express) 180min. — Kanazawa Station

Total: 3hr.50min.
Fare: 10,000yen

From Narita Airport

1. Narita Airport — Airport Limousine Bus 75min. — Haneda Airport — Air Plane 60min. — Komatsu Airport — Airpor Limousine Bus 50min. — Kanazawa Station

Total: 3hr.05min.
Fare: 20,000yen

2. Narita Airport — JR Narita Express 60min. — Tokyo Station — JR Shinkansen (Joetsu Line) 80min. — Echigoyuzawa Station — JR Hakutaka (Express) 150min. — Kanazawa Station

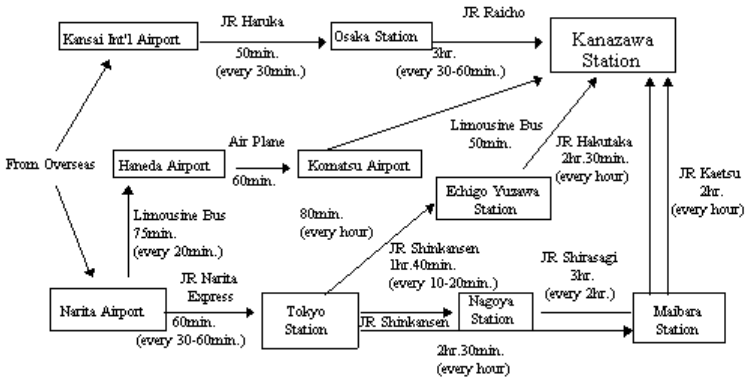
Total: 4hr.50min.
Fare: 15,000yen

3. Narita Airport — JR Narita Express 60min. — Tokyo Station — JR Shinkansen (Tokaido Line) 150min. — Maibara Station — JR Kaetsu (Express) 120min. — Kanazawa Station

Total: 5hr30min.
Fare: 18,000yen

3. Narita Airport — JR Narita Express 60min. — Tokyo Station — JR Shinkansen (Tokaido Line) 100min. — Nagoya Station — JR Shirasagi (Express) 180min. — Kanazawa Station

Total: 5hr.40min.
Fare: 18,000yen



Time table for Haneda to Komatsu Airport

JAL	141	B4	0750	->	0850
JAS	261	A3	0815	->	0915
ANA	751	B6	0845	->	0945
ANA	753	B4	0955	->	1055
JAS	263	A3	1055	->	1155
ANA	757	B4	1510	->	1610
JAS	265	A3	1715	->	1815
JAL	147	B4	1805	->	1905
ANA	759	B4	1930	->	2030

Access to Kanazawa Citymonde Hotel

From JR Kanazawa Station

Round Bus: take a bus No.11 or 12 and should get off at "Hashiba-cho", fare is 200yen.

Taxi: takes about 10minutes, and about 1,000yen.

Hotel Accommodations

The Japan Travel Bureau, Inc. (JTB) has been appointed the Official Travel Agent for ICMTS and will handle all travel arrangements to and within Japan. Please address all inquiries and application forms for hotel accommodation to:

Japan Travel Bureau, Inc. (JTB)

Tours & Convention Division, Kansai District

Nittochi-Dojima Bldg.

1-4-19 Dojimahama, Kita-ku

Osaka 530, Japan

Phone: +81-6-345-3979 Fax: +81-6-345-0910

Japan Travel Bureau (JTB) has reserved a sufficient number of rooms at the following hotels for the conference participants at special discount rates.

Those who wish to apply for hotel reservation are requested to complete the centerfolded application form, and return it to JTB before March 7, 1998 with the necessary deposit (10,000yen per room).

Hotel Assignment will be made on a first-come, first-served bases.

Daily room charges are as follows:

Name of Hotel	Room Rate	(per person)
Kanazawa Citymonde Hotel	Single	9,240
	Twin	8,085
	Deluxe Single*	10,290

*(Single occupancy of twin room)

Note:

1) Above rate includes breakfast, service charge and tax.

2) The deposit of 10,000yen will be deducted from the balance of the hotel bill upon check-out.

Cancellation

In case of hotel cancellation, written notification should be sent directly to JTB. Deposit will be refunded after deducting the following cancellation charges, when notification is received by JTB.

Up to 9 days before the first night of stay 1,000yen per room

8-2 days before 20% of the daily room charge

One day before 80% of the daily room charge

On day, or no notice given 100% of the daily room charge

Equipment Exhibition

An equipment exhibition will be held in front of the Citymonde Hall during the Conference to display equipment closely paralleling the nature of this meeting. This equipment exhibition will permit one-on-one discussions between exhibitors and conference attendees on the latest test equipment. Exhibits will be open as follows.

March 23, 25	9:00am - 5:00pm
March 24	9:00am - 6:00pm
March 26	9:00am - 12:00pm

The exhibitors list is attached at the end of this booklet.

For information contact:

Satoshi Habu, Equipment Chairman

Hewlett-Packard Japan, Ltd.

9-1 Takakura-cho, Hachioji, Tokyo 192, Japan

Phone: +81-426-60-2168 Fax: +81-426-60-8430

E-mail: satoshi_habu@om.jpn.hp.com

TUTORIAL SHORT COURSE

An Introduction to the Design, Measurement, and Analysis of Microelectronic Test Structures

The ICMTS Tutorial is a one-day short course that is intended to provide the non-expert with the fundamentals associated with microelectronic test structures. The course strive to provide good design, test, and analysis guidelines so that superior test-structure practice will be followed, thus paving the way for improved process control, higher yield product, and rapid product introduction. The course instructors, chosen by Dr. Buehler and Dr. Sasaki for this year's tutorial have many years of experience in the field of test structures. The format will be interactive with emphasis on the practical use of microelectronic test structures.

TUTORIAL SCHEDULE

Monday, March 23, 1998

9:00 am REGISTRATION

10:00 am 1. Welcome - Nobuo Sasaki, Fujitsu Labs.

10:05 am 2. Fundamentals of Microelectronic Test Structures - Anthony J. Walton, Univ. of Edinburgh

- History of Microelectronic Test Structures
- Motivation for using Test Structures
- Proper Test Structure Design
- Basic Measurement Techniques

10:50 am 3. Electrical Linewidth and Overlay - Loren W. Linholm, NIST

- Introduction
- Electrical Linewidth

  Background

  Electrical Structure: Cross-Bridge Resistor

  Measurement Results and Comparisons

  Enhancements

  Future Applications
- Electrical Overlay

  Background

  Electrical Structures: van der Pauw, Sliding Wire, MOATS

  Measurement Results and Comparisons

  Future Applications
- Summary

11:35 am 4. Reliability - Katsuhiko Kubota, Hitachi

- Oxide Breakdown
- Hot Carrier
- Electromigration

12:20 pm HOSTED LUNCH

1:50 pm 5. Capacitance Measurement Techniques on Wafer - Satoshi Habu, HP Japan

- Basic Measurement Technique of Capacitance Measurement
- Error Source of Capacitance Measurement
- Error Reduction Technique
- Actual Solutions for Measurement on Wafer

2:35 pm 6. Transistor Matching - Hans Tuinhout, Philips Research

- Introduction

  (motivation, terminology, orders of magnitude, mismatch effects)

- Matching Measurement Techniques

  (hardware considerations, measurement methods, statistical techniques)

- Matching Test Structure Design Considerations
- Summary and Literature

3:20 pm 7. Application of Test Structure in DRAMs - Naoki Kasai, NEC

- Background / Trend in DRAM Technology
- Test Structures for DRAM Development

  Memory cell components

  Sense amplifier

  Soft error

- Failure Analysis of Memory Cell Array

  Retention time

  Diagnostic system

4:05 pm BREAK

4:30 pm 8. Application of Test Structure in Flash Memories - Hiroaki Hazama, Toshiba

- Introduction
- Overview of Flash Memory

  Array Structure and Operation Principle

  Reliability Problems

- Test Structure for Flash Device Development

  MOS Capacitor

  Array Test Structure Design

- Reliability Analysis by Test Structure

  Endurance Problem

  Over Erase Problem

  Disturb Problem

- Conclusion

5:15 pm 9. Test Structures for TFT Liquid Crystal Displays - Katsuhiro Kawai, Sharp

- Introduction :Principle and Structure of TFT-LCDs
- TFT-LCD Process(TFT array process / LC Cell process)
- Industrial Requirements for TFT Array Process
- Test Structures for TFT Devices
- Methods to Test TFT Array

6:00 pm 10. Tutorial Conclusion - Nobuo Sasaki, Fujitsu Labs.

TUTORIAL SHORT COURSE INSTRUCTORS

Anthony J. Walton - Fundamentals of Microelectronic Test Structures

Anthony J. Walton has been a member of the Electrical Engineering Department at the University of Edinburgh for the past 15 years. During that time he has been involved with the microelectronics industry in a number of areas which include silicon processing, yield improvement, Design for Manufacturability (DFM), Technology Computer Aided Design (TCAD) and microelectronic test structures. His present interests also include the optimisation of semiconductor processes through the integration of experimental design and TCAD simulation tools. He has published widely and in 1990 won the best paper award for the IEEE Transactions on Semiconductor Manufacturing.

Loren W. Linholm - Electrical Linewidth and Overlay

Loren W. Linholm received the B. S. degree in Electrical Engineering from the University of California, Berkeley, in 1968, and the M. S. degree in Electrical Engineering from the University of Maryland, College Park, Maryland, in 1973. He has been employed by the Naval Missile Center, Point Mugu, California, and the Department of Defense, Ft. Meade, Maryland, and since 1978, the Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, Maryland. He heads the Integrated Circuits Technology Group, which is responsible for designing, developing, and evaluating measurements methods for evaluating silicon integrated circuits, manufacturing tools, and processes with emphasis on test structures, associated data analysis techniques, novel sensors, and advanced microelectromechanical systems. Mr. Linholm is a member of the IEEE Electron Devices Society and a co-founder of the International Conference on Microelectronic Test Structures.

Katsuhiko Kubota - Reliability

Katsuhiko Kubota received the B.S. degree from Shizuoka University and the M.S. degree from the University of Tokyo, in 1977 and 1979, respectively. Since he joined Hitachi Ltd. in 1979, he has been involved in the development and reliability study of various LSIs such as DRAM, SRAM, non-volatile memory, high-speed logic, ferroelectric, and anti-fuse FPGA. From 1983 to 1984, he was a visiting researcher at Cornell University where he studied SOI. He is now responsible for reliability modeling and analysis of deep submicron devices covering oxide integrity, hot carrier, electromigration and ESD. Currently he is interested in oxide leak mechanisms.

Satoshi Habu - Capacitance Measurement Techniques on Wafer

Satoshi Habu received the B.S. and M.S. degree in Electrical Engineering from Ibaraki University in 1981 and 1983, respectively. In 1983 he joined Hewlett-Packard Japan, Ltd as R&D engineer and he has been working for developing instruments for semiconductor parameter measurements. He is currently heading group for developing instruments.

Hans Tuinhout - Transistor Matching

Hans Tuinhout received his MSEE degree from Delft University of Technology (NL) in 1980. Since then he worked on process and device characterization for CMOS and BiCMOS processes at Philips' Research Laboratories in Eindhoven, the Netherlands.

His current research activities are focused on very accurate DC device measurements for characterization and improvement of matching performance of mixed-signal IC processes.

Naoki Kasai - Application of Test Structure in DRAMs

Naoki Kasai received his B.S. and M.S. degrees in applied chemistry from Waseda University, Tokyo, Japan, in 1980 and 1982, respectively. In 1982, he joined NEC Corporation where he engaged in the research and development of CMOS process technology. From August 1988 to August 1989, he studied MOS device technology at Stanford University under Prof. K. C. Saraswat, as a visiting researcher. Since 1989 he has been engaged in the research and development of 64Mbit-, 256Mbit-, and 4Gbit-DRAM prototype chips. He has authored and co-authored over 30 papers, including 3 papers presented at ICMTS. Mr. Kasai is a member of the IEEE Electron Devices Society.

Hiroaki Hazama - Application of Test Structure in Flash Memories

Hiroaki Hazama was born in Kochi Prefecture, Japan, on October 1, 1959. He received the B.S. and M.S. degrees in electronic engineering from Osaka University, Osaka, Japan, in 1983 and 1985, respectively. In 1985, he jointed the Toshiba Research and Development Center, Toshiba Corporation, Kawasaki, Japan. He was engaged in SOI device technology, in small-featured-size MOS device technology and in reliability on thin gate dielectric from 1985 to 1993 in the Process Research Department of Toshiba ULSI Research Center. Since 1994, he has been engaged in the development of nonvolatile memory in the Microelectronics Engineering Laboratory, Toshiba Corporation. He has been especially concerning the reliability issue of the nonvolatile memory. Mr. Hazama is a member of the Japan Society of Applied Physics.

Katsuhiro Kawai - Test Structures for TFT Liquid Crystal Displays

Katsuhiro Kawai received the B.S. and M.S. degrees in chemical engineering from Osaka University, Japan, in 1987 and 1989 respectively. He joined Sharp Corp. Japan, in 1989 where he has been engaged in the TFT development center liquid crystal group. He has developed the TFT array process for large area TFT-LCDs.

TECHNICAL PROGRAM

The Technical Program consists of eleven sessions of contributed papers, equipment presentation, and exhibition.

Papers that are judged by the reviewers to be appropriate for visual presentation (papers primarily concerned with data summaries, mathematical derivations, or demonstrations) will be displayed as posters during the Conference. A dedicated two-hour Poster Session will be held in which authors will be given five minutes for oral presentations to the general audience. In addition, a five-minute talk will be given by each exhibiting company during the equipment exhibit.

All sessions will be in Citymonde Hall.

TECHNICAL PROGRAM SCHEDULE

TUESDAY, MARCH 24, 1998

8:15 am Registration

9:30 am Opening Remarks

Kunihiro Asada, General Chairman

Hiroshi Koyama, Technical Chairman

SESSION I

INVITED PAPER

Co-Chairmen: Hiroshi Koyama, Mitsubishi, Japan

Alan Mathewson, NMRC, Ireland

9:40 am

300mm Evaluation Activities in Selete

Keiji Fujiwara

Semiconductor Leading Edge Technologies, Inc., Japan

10:20 am Break

SESSION II

MATCHING

Co-Chairmen: **Robert Ashton,** Lucent Tech., Bell Labs., USA

Yoshiaki Hagiwara, Sony, Japan

11:00 am

Measurement of Lithographical Proximity Effects on Matching of Bipolar Transistors

H. P. Tuinhout and W. C. M. Peters* Philips Research and Philips Semiconductors**, The Netherlands

This paper describes a measurement approach that is used for very accurate BJT matching measurements down to the sub 25$\mu V \sigma_{\Delta Vbe}$ region. This is demonstrated with the analysis of lithographical proximity effects on matching of NPN and lateral PNP BJTs.

11:20 am

New Method for Monitoring of Analogue Processes - Evaluation of the Impact of Metallization on the Performance of Precise Analogue Resistors

A. Pergoot, P. Cox, P. Vercruysse*, I. Wuyts and P. Raes*

Alcatel Mietec and Campus BME - CTL*, Belgium

By using a new test structure and method we are able to characterize the dependence of the high-ohmic polycrystalline (HIPO) resistor parameters on process changes and topology as it appears in the real ASIC's. In this paper we report the most important impact we have discovered, that of metal lines placed in parallel with the HIPO resistors. Different metallization schemes are compared concerning the effect on the analog characteristics of the HIPO resistor.

11:40 am

A High Density Integrated Test Matrix of MOS Transistors for Matching Study

L. Portmann, C. Lallement and F. Krummenacher

Swiss Federal Institute of Technology (EPFL), Switzerland

A circuit that allows the measurement of 480 or more MOS transistors on a single 1.5mm^2 die with a 4 channels semiconductor analyzer is described. It has been integrated on a fully depleted SOI process and on a standard bulk process. Extraction methodology as well as matching properties of SOI transistors are discussed.

12:00 pm Lunch

SESSION III

INVITED PAPER

Co-Chairmen: **Hiroshi Koyama,** Mitsubishi , Japan

Alan Mathewson, NMRC, Ireland

1:20 pm

Requirements and Challenges for Lithography: Beyond 193-nm Optics

John T. Canning

SEMATECH, USA

SESSION IV

CD METROLOGY

Co-Chairmen: **Lawrence Bair,** DEC, USA

Yukinori Kuroki, Kyushu Univ., Japan

2:00 pm

Extraction of Sheet-Resistance from van-der-Pauw Resistors Replicated in Monocrystalline Films Having Non-Planar Geometries

M. W. Cresswell, N. M. P. Guillaume, R. A. Allen*, W. F. Guthrie and

L. W. Linholm

National Institute of Standards & Technology, USA and Ecole National Supérieure d'Electrotechnique Electronique Informatique Hydraulique de Toulouse*, France

Linewidth values obtained in electrical test-structure metrology are directly proportional to available estimates of the local sheet resistance whose reliability is thus of leading importance in obtaining the correct electrical linewidth. However, in the case of a new type of electrically-certifiable CD test structures fabricated from monocrystalline SOI films, the van-der-Pauw resistors used for sheet-resistance extraction are fabricated with three-dimensional, instead of planar, geometries. This abstract presents a new algorithm for sheet-resistance extraction from van-der-Pauw resistors replicated in such films and shows examples of supporting experimental data and their comparison with current-flow analyses.

2:20 pm

Test Structures to Characterise a Novel Circuit Fabrication Technique that uses Offset Lithography

A. J. Walton, J. T. M. Stevenson, M. Fallon*, P. S. A. Evans**,

B. J. Ramsey** and D. Harrison**

University of Edinburgh, National Semiconductor* and Brunel University**, UK

This paper reports on the use of microelectronic test structures to characterise a novel fabrication technique for thin-film electronic circuit boards. In this technology circuit tracks are formed on paper-like substrates by depositing films of a metal-loaded ink via a standard lithographic printing process. Sheet resistance and linewidth are electrically evaluated and these compared with optical and surface profiling measurements.

2:40 pm

A New Method for Electrical Extraction of Spacer Width, Poly Sheet Rho, and Poly CD in Salicide Process

G. A. Rezvani, S. Bothra, X. W. Lin and A. Ho VLSI Technology Inc., USA

In this abstract a new method for extraction of poly CD and sheet rho for narrow poly lines is presented, which is useful in salicide processes where the standard method of electrical extraction of poly sheet rho and CD is not applicable anymore. In addition this new method allows for electrical extraction of spacer width. This method is applied to a salicided 0.25μm technology, and the results are discussed and compared with the standard method.

3:00 pm

Monitoring of SRAM Gate Patterns in KrF Lithography by Ellipsometry

H. Arimoto, S. Nakamura, S. Miyata* and K. Nakagawa* Fujitsu Laboratories Ltd. and Fujitsu Ltd.*, Japan

This paper reports on the ellipsometric monitoring of SRAM gate patterns in KrF lithography. A multivariable regression analysis was applied to predict gate lengths by using six ellipsometric parameters which, were obtained by employing different measurement conditions such as laser incidence angles, directions, and samples without patterns. A good agreement (3σ=8.7nm) between the measured CD-SEM values and the predicted values was achieved.

3:20 pm

Effect of Temperature on the Electrical Properties of CD Test-structure Features Replicated in Monocrystalline Films

R. A. Allen, O. Oyebanjo*, M. W. Cresswell and L. W. Linholm

National Institute of Standards & Technology, George Washington University*, USA

Test structures fabricated in monocrystalline SOI films have physical properties that are highly desirable for reference features in CD calibration artifacts. In addition, reference-feature linewidth measurement by electrical testing can be conducted at significantly lower cost than by alternative methods. However, it is not yet clear how well electrical testing can serve as a reference to more fundamental CD-certification measures such as lattice-plane counting. Monitoring variations with temperature of electrically-measured CD (ECD) and sheet resistance of electrical test structures replicated in monocrystalline materials such as silicon offer an important opportunity for CD certification assurance because the pertinent physics of these materials is well established.

3:40 pm Break

SESSION V

EXHIBITION PRESENTATION

Chairman: **Satoshi Habu**, Hewlett-Packard, Japan

Alan Mathewson, NMRC, Ireland

3:50 pm Exhibition Presentation

6:00 pm End of Exhibition

WEDNESDAY, MARCH 25, 1998

8:30 Registration

8:50 ICMTS 1999

SESSION VI

INVITED PAPER

Co-Chairmen: **Hiroshi Koyama**, Mitsubishi, Japan

Alan Mathewson, NMRC, Ireland

9:00 am

Current Status and Issues of X-ray Mask

Shingo Uchiyama

NTT System Electronics Laboratories, Japan

9:40 am Break

SESSION VII

PARAMETER EXTRACTION

Co-Chairmen: **Hans P. Tuinhout,** Philips, The Netherlands

Loren W. Linholm, NIST, USA

10:20 am

A Novel Method for Base and Emitter Resistance Extraction in Bipolar Junction Transistors from Static and Low Frequency Noise Measurements

P. Llinares*, **, G. Ghibaudo***, N. Gambetta**, Y. Mourier****,

A. Monroy**, G. Lecoy**** and J. A. Chroboczek*

France Telecom*, SGS-THOMSON Microelectronics**, Laboratoire de Physique des Composants à Semiconducteurs*** and Centre d'Electronique de Montpellier II****, France

A novel method of extraction of emitter and base resistances of bipolar junction transistors, BJTs, involving both static characteristics and low frequency noise data is proposed and tested on quasi self-aligned BJTs. The method requires no special test structures and is applied to transistors working in the normal operation regime, thus it may be readily applied to test procedures for various types of BJTs.

10:40 am

Evaluation of the Scaling Limit of Narrow U-groove Isolation Structure by Using Test Structures

Y. Tamaki and T. Hashimoto

Hitachi Ltd., Japan

This paper describes the scaling limit of the width and the structure of narrow isolation U-grooves by using new test structures for evaluating isolation capacitance and isolation breakdown voltage. It is concluded that the minimum width of the isolation U-groove will be limited by the increase in isolation capacitance, and an effective method is proposed to overcome the problem. Future SOI structure is also discussed.

11:00 am

Anomalous Geometry Dependence of Source/Drain Resistance in Narrow-width MOSFETs

A. J. Scholten and D. B. M. Klaassen Philips Research Laboratories, The Netherlands

The geometrical scaling of the intrinsic source/drain resistance (R_{SD}) of MOSFETs is investigated using a large selection of transistor geometries in 0.5μm CMOS technology. It is shown both experimentally and theoretically that for narrow-width MOSFETs with dogbone layouts R_{SD} is no longer inversely proportional to the channel width. A new scaling rule for R_{SD} and thus for the mobility reduction parameter q_1 of MOS Model 9 leads to a considerably improved modeling accuracy in both the linear and saturation regime.

11:20 am

Direct Extraction of SPICE Gummel-Poon Parameters for High Frequency Modeling

J. W. Breti, J. D. Kendall and L. Nathawad*

Gennum Corp. and Simon Fraser University*, Canada

A method to directly extract the DC and AC SPICE Gummel-Poon parameters without optimization is presented. The DC extraction uses linear or explicit extraction equations. The AC extraction involves obtaining the SPICE AC equivalent circuit from measured S-parameter data, and then extracting the SPICE parameters from the bias dependence of the AC equivalent circuit elements. By comparing measured and simulated S-parameters it is verified that the resulting parameter set provides accurate modeling across frequency and bias, making accurate circuit simulation and statistical studies possible.

11:40 am

Advanced Characterization Method for Sub-micron DRAM Cell Transistors

I. Kurachi

Oki Electric Industry Co., Ltd., Japan

Advanced characterization method for sub-micron DRAM cell transistors has been proposed for analysis of transistor test structures with actual memory cell patterns. In this method, new transistor parameters, Vgoff and Vgsat, have been considered for transistors' off-leakage and full writing to storage node, respectively. These parameters are found to be good monitoring parameters for DRAM failures such as bit failures.

12:00 Lunch

SESSION VIII

YIELD AND RELIABILITY

Co-Chairmen: **Andreas Preussger,** HL ZUV, Germany

Jun Kudo, Sharp, Japan

1:20 pm

Detailed Observation of Small Leak Current in Flash Memories with Thin Tunnel Oxides

Y. Manabe, K. Okuyama, K. Kubota, A. Nozoe, T. Karashima, K. Ujiie*, H. Kanno*, M. Nakashima** and N. Ajika**

Hitachi Ltd., Hitachi ULSI Engineering Corp.*, Mitsubishi Electric Corp.**, Japan

This paper describes a method for measuring the small current through the oxides on the order of 10^{-20} A or less using a floating gate MOSFET and the application results on flash memories with thin tunnel oxides. We found some abnormal phenomena which cannot be obtained from SILC measurements using large capacitors. We also discuss possible mechanisms to explain the phenomena.

1:40 pm

Wafer Level Defect Density Distribution Using Checkerboard Test Structures

C. Hess and L. H. Weiland

University of Karlsruhe, Germany

Defect parameter extraction plays an important role in process control and yield prediction. A methodology of evaluating wafer level defect density distributions will be presented. For that, imaginary wafermaps are generated for a variety of different chip areas to calculate a yield-to-area dependency. Based on these calculations a Micro Density Distribution (MDD) will be determined for each wafer.

2:00 pm

Monitoring Method of the Tunnel Oxide Degradation by MOS Capacitor

H. Hazama

Toshiba Corp., Japan

The tunnel oxide degradation monitoring method by simple MOS capacitor has been examined. It was found that the tolerance of the tunnel oxide for NAND type EEPROM operation could be monitored by MOS capacitor applying the bi-polarity FN injection method. Using improved experimental setup, bi-polarity FN injection could be performed for simple MOS capacitor without source junction.

2:20 pm

New Characterization Methodology for Flash Memory Cell Using CAST Structure

M. Fan, U. C. Liu, J. C. Guo, M. H. Chou, M. T. Wang and F. Shone

Macronix International Co., Ltd., Taiwan, R.O.C.

The hole trapping occurred during P/E operation in Flash EEPROM. To our knowledge, there still no effective method to characterize the endurance performance of Flash EEPROM in the test key level. In this paper, we propose a simple and fast method to evaluate the endurance performance on a 12K bits test Flash EEPROM Cell Array Stress Test (CAST) array. Base on this method, we can easily detect the subtle defects as well as the effectiveness of hole detrapping method to suppress the tail-bits.

2:40 pm Break

SESSION IX

POSTER SESSION

Co-Chairmen: **Anthony Walton,** Univ. of Edinburgh, UK

Takashi Ohzone, Toyama Prefectural Univ., Japan

3:20 pm

Using Test Structures to Asses the Impact of Critical Process Steps on MOS Transistor Matching

H. Elzinga Philips Semiconductors, The Netherlands

This paper demonstrates the use of test structures to asses the impact of critical process steps on MOS transistor matching performance. The results of this assessment are used to improve the critical process steps, resulting in optimum MOS transistor matching performance.

3:25 pm

A New Variational Method to Determine Effective Channel Length and Series Resistance of MOSFET's

K. Yamaguchi, H. Amishiro, M. Yamawaki and S. Asai Mitsubishi Electric Corp., Japan

A new variational method to determine the effective channel length and the series resistance of MOSFET's has been proposed. In the resistant based method, it is only possible to determine the effective channel length at Vgs = Vth. The new method yields constant effective channel length in the neighborhood of Vgs = Vth and series resistance dependent on gate voltage. The new method is well-defined and gives accurate and consistent effective channel length and series resistance.

3:30 pm

Statistical Characterization of 0.18μm Low-power CMOS Process using Efficient Parameter Extraction

K. G. McCarthy, E. V. Saavedra Diaz, D. B. M. Klaassen* and A. Mathewson

National Microelectronics Research Centre, Ireland and Philips Research Laboratories*, The Netherlands

This paper presents a statistical analysis of a 0.18μm CMOS technology by means of efficient parameter extraction techniques applied to MOS Model 9 which allow all model parameters to be obtained from only 50 measurements. The statistical analysis demonstrates that both parameter spreads and correlations can be considered during circuit simulation.

3:35 pm

Electrical Characteristics of 0^{o} /$\pm45^{o}$ /90^{o} -Orientation CMOSFET with Source/Drain Fabricated by Various Ion-Implantation Methods

T. Ohzone, M. Okina, T. Matsuda

Toyama Prefectural University, Japan

Electrical characteristics of $0^{o}/\pm45^{o}/90^{o}$ -orientation 0.5 μm CMOSFETs with source/drain regions fabricated by three ion-implantation methods were discussed. For asymmetrical one-sided 7^{o} -implantation method, large device orientation dependence was observed in (I_D and I_B of both n- and p-MOSFETs/V_T of p-MOSFETs). However, almost comparable data were obtained for symmetrical 0^{o} -implantation and 7^{o}x4-implantation methods.

3:40 pm

Hot Carrier Degradation in Matched Transistor Pairs: A New High Resolution Measurement Technique

R. Dreesen, W. De Ceuninck, L. De Schepper and A. Pergoot*

Limburgs Universitair Centrum and Alcatel Mietec*, Belgium

A new measurement methodology has been developed in order to perform high-resolution measurements on the hot carrier degradation of MOSFET's. With this methodology, degradations as low as 0.01% can be measured accurately. The high resolution measurements are necessary for measuring hot carrier degradation in matched transistor pairs. This is demonstrated by comparing the degradation at different stress conditions. The low-percentage region shows a behavior different from the high-percentage region liner extrapolation model.

3:45 pm

Study of Low Frequency Noise in Scaled down Silicon CMOS Transistors

T. Boutchacha, G. Ghibaudo* and B. Belmekki

Institut d'Electronique, USTO, Algérie and Laboratoire de Physique des Composants à Semiconducteurs, URA CNRS*, France

A detailed investigation of the low frequency (LF) noise in 025μm N and P MOS devices is carried out. A theoretical analysis of the drain current noise and the gate voltage noise characteristics is developed in the framework of carrier number fluctuation model as well as corrected mobility fluctuations. The scattering parameter is found to be lower for N MOS transistors, while the value of P MOS is relatively high in agreement with static mobility data. This justifies the enhancement of the correlated mobility noise for P MOS devices.

3:50 pm

Strategy to Disentangle Multiple Faults to Identify Random Defects within Test Structures

C. Hess and L. H. Weiland University of Karlsruhe, Germany

Defect inspection is required for process control and to enhance chip yield. Electrical measurements at test structures are commonly used to detect faults. This paper presents a strategy to analyze single and multiple faults to precisely determine the number, layer and location of randomly distributed defects within a test structure layout. For that we first discuss the possibilities to analyze faults within known test structure layouts. Then, we present modified test structure layouts to improve the analysis of multiple faults. Finally we introduce a methodology to disentangle multiple faults by calculating and comparing the probability of possible defect locations within large test structure layout areas.

3:55 pm

Prediction of AC Performance of Double-polysilicon Bipolar Transistors from E-Test Parameters: An Experiment

S. C. Kelly, E. C. Griffith, J. A. Power and M. O'Neill

Analog Devices, Ireland

AC characterisation of silicon bipolar processes for RF applications is necessary because of the ever increasing speed of operation of the bipolar devices. The data acquisition and parameter extraction is a time consuming and tedious task which cannot easily be implemented as part of standard process monitor measurements. This paper will discuss a methodology for relating the readily available E-test parameter database to the AC parameters which are more difficult to obtain. The work was done on a 0.6μm BiCMOS process which is suited to mixed mode RF chip designs.

4:00 pm

Measurement of "1/f " Noise in Narrow Polysilicon Emitter Bipolar Transistor Structures

S. D. Connor

G. E. C. Plessey Semiconductors, UK

We present here our initial findings on low frequency noise measurements for shallow emitter, poly-silicon contacted transistors. Structures from two particular GEC Plessey Semiconductors technologies were selected for measurement to assess the change in low frequency noise performance and modeling issues as bipolar technologies move to even shallower emitter junctions and smaller emitter windows. We also demonstrate an alternative approach to the problem of identifying the intrinsic corner frequency and the extraction of SPICE noise parameters. Details of our measurement technique are given along with the results of some simulations based on SPICE coefficients extracted from these measurements.

4:05 pm

A New Direct Extraction Algorithm for Intrinsic Gummel-Poon BJT Model Parameters

F. Ingvarson and K. O. Jeppson

Chalmers University of Technology, Sweden

A new two-step direct extraction algorithm for the intrinsic Gummel-Poon BJT model parameters is presented. Both original and SPICE Gummel-Poon Early effect parameters are extracted in a coupled and consistent manner. This ensures proper extraction of the Early voltages which is a necessary precursor to accurate determination of the remaining parameters. All parameters are determined from linear systems of equations using traditional least square techniques.

4:10 pm

A Prediction Method of Oxide Breakdown Caused by Defects in SiO_2 Films

H. Uchida and N. Hirashita

Oki Electric Industry Co., Ltd., Japan

A new prediction method of so-called B mode failure in TZDB tests, oxide breakdown at lower electric field, has been investigated. Two assumptions are made in this model, which are the defect-invisible region and the defect growth during gate oxidation. B mode failure distribution calculated using this method agrees well with measured TZDB data for oxide thickness ranged from 6.1nm to 14.8nm. This method is useful to interpret dependence of B mode failure distribution on oxide thickness and gate area.

4:15 pm

Analysis of a New Test Pattern for Measuring the Carrier-Carrier Scattering Mobilities versus the Injection Level in Silicon

S. Bellone and G. V. Persiano University of Salerno, Italy

The operation of a recently proposed technique for determining the injection-dependent mobility of electron and hole in silicon is explored. For an accurate monitoring of the injection level, a simple approach to measure the carrier density injected from a generic surface p-n junction is presented. By adding the above feature to the basic test pattern, the carrier mobilities can be accurately estimated without involving any critical parameter.

4:20 pm

On the Use of Test Structures for the Electro-Mechanical Characterization of a CMOS Compatible MEMS Technology

L. Latorre, Y. Bertrand and P. Nouet

LIRMM, France

In this paper we discuss about the use of test structures to characterize a microsystem technology. Using simple devices and elementary mechanical relations, we determine all the properties of sensor parts, i.e. the piezoresistive factor of polysilicon and a complete set of electro-mechanical relations.

4:25 pm

Test Structures for MCM-D Technology Characterization

M. Lozano, J. Santander, E. Cabruja, C. Perelló*, M. Ullán and E. Lora-Tamayo

CMM, Spain and IMEC*, Belgium

In a Multichip Module technology (MCM) a silicon chip is used as a substrate on which other commercial chips are flipped and soldered by a screen-printing method. This complex technology has specific test problems. In this paper we present a set of classic and novel test structures addressed to the full characterization of a MCM, flip-chip, ball grid array, silicon substrate technology. We specially focus on the measurement of the ball chip to chip contact resistance, and on the electrical influence of near chips, placed on top of circuits on the substrate.

4:30 pm

Characterization and Application of Interconnect Process Parameters

A. Chou, K.-J. Chang, R. Mathews, K.Wong, T. Wang*,

Y.-H. Wei*, K. C. Su** and P. Hsue**

Frequency Tech., Inc., S3 Inc.*, USA and United Microelectronics Corp.**, Taiwan, R.O.C.

Interconnect process parameters of a 0.35μm process were fully characterized with large numbers of electrical measurements. The characterized parameters were then used with a TCAD tool to calculate capacitances of complicated test structures that mimic signal nets in real designs. The excellent agreement between calculation results and electrical measurements of the structures demonstrates that combination of TCAD tool and fully characterized interconnect process parameters can provide accurate prediction of interconnect circuit performance.

4:35 pm

A Novel Unified Transient Enhanced Diffusion Model on the Basis of RSF with Process Database

H. Sato, K. Tsuneno and H. Masuda

Hitachi Ltd., Japan

A novel unified TED (Transient Enhanced Diffusion) model for RTA and furnace processes is proposed on the basis of the vacancy-assisted diffusion model. The effective diffusivity is described by a RSF (Response Surface Function) based on relaxation-time approximation of point defects, which depends on the annealing temperature and implant dose. The parameters were calibrated with a set of experimental database of test structures.

6:00 pm End of Poster

7:00 pm Banquet

9:00 pm End of Banquet

THURSDAY, MARCH 26, 1998

SESSION X

RELIABILITY

Co-Chairmen: **Christopher Hess,** Univ. of Karlsruhe, Germany

Masakazu Shimaya, NTT, Japan

9:00 am

A New Test Structure for Evaluation of Extrinsic Oxide Breakdown

K. Shiga, J. Komori, M. Katsumata, A. Teramoto and M. Sekine

Mitsubishi Electric Corp., Japan

A new test structure for evaluating extrinsic oxide breakdown is proposed. The active gate area which is needed to predict reliability will be shown. And by using this new test structure, activation energy not only for the intrinsic breakdown but also for the extrinsic breakdown are obtained.

9:20 am

Extraction of the Si-SiO_2 Interface Trap Layer Parameters in MOS Transistors Using a New Charge Pumping Analysis

Y. Maneglia and D. Bauza

LPCS, ENSERG/INPG, France

Using an in-depth approach of the Si-SiO_2 interface, the parameters of the Si-SiO_2 interface trap layer are extracted. Trap depth concentration profiles are found of the form $N_t(X)=N_{ts}\exp(-x/d)+N_{to}$. The first term corresponds to the Si-Sio_2 interface traps and the second one is the trap density in the oxide strained layer. N_{ts}/N_{to} is around 100 in state-of-the-art MOS devices. This is achieved using a new charge pumping analysis. The distortions introduced on the profiles by the near source and drain regions of the devices, where the doping concentration is not that in the channel, are evaluated. The case of RTCVD oxynitride as gate films is also considered.

9:40 am

The Influence of SiN Films on Negative Bias Temperature Instability and Characteristics in MOSFETs

K. Sasada, M. Arimoto, H. Nagasawa, A. Nishida, H. Aoe, T. Dan,

S. Fujiwara and Y. Matsushita

SANYO Electric Co., Ltd., Japan

We propose a method of suppressing both water diffusion and mechanical stress for MOSFETs, using test structures which are constructed by several designs with SiN films. It is found that SiN films with a thickness of 7nm can suppress both the diffusion and the stress. The same effect can also be obtained when SiN films with a thickness of 20nm are patterned to cover the active area, which is decided by taking only the water diffusion into account.

10:00 am

An Analysis of Hot-Carrier-Induced Photoemission Profiles in n-MOSFETs

T. Ohzone, N. Matsuyama, N. Hosoi and T. Matsuda

Toyama Prefectural University, Japan

Hot-electron induced photoemission peaks in n-MOSFETs specially designed for the photoemission analysis with L=0.35~2.0 μm were measured using a high resolution photoemission microscope. The peak at n^+-drain edge and the peak shift from LDD-drain edge toward n^+-drain edge were observed for $L\geq 0.40$ and L=0.35 μm devices, respectively. The peak due to p-n junction breakdown was located at n^+-drain edge.

10:20 am Break

SESSION XI

INTERCONNECTS AND CAPACITANCE MEASUREMENTS

Co-Chairmen: **Alfred C. Ipri**, David Sarnoff Res. Ctr., USA

Toshiharu Watanabe, Toshiba, Japan

11:00 am

TEST Structure for Characterizing Capacitance Matrix of Multi-layer interconnections in VLSI

T. Mido, H. Ito and K. Asada

University of Tokyo, Japan

Extraction of capacitances in multi-layer interconnections has many problems. Because of a large number of typical cases of capacitances, it needs a lot of conductors and test pads to extract parameters. Therefore it needs large area for test element groups (TEGs) and time consuming extraction process for characterizing capacitance matrix. This paper describes a new test structure for characterizing the capacitance matrix of the multi-layer interconnections, along with a calculating method of the capacitance matrix where the capacitance dependence of bias conditions, positions and geometries are evaluated.

11:20 am

A New Characterization Method for Accurate Capacitor Matching Measurements Using Pseudo-Floating Gate Test Structures in Submicron CMOS and BICMOS Technologies

O. Roux dit Buisson, G. Morin, F. Paillardet and E. Mazaleyrat

SGS-THOMSON Microelectronics, France

In deep submicron CMOS and BICMOS technologies, antenna effects affect floating gate charge of usual floating gate test structures, dedicated to accurate capacitor matching measurement. In this paper a new pseudo-floating gate test structure is designed. After test structure and modeling presentation, testing method and results are given for several capacitor layouts (poly-poly and metal-metal).

11:40 am

A New Method for Extracting the Capacitance Coupling Coefficients of Sub-0.5-μm Flash Memory Cells in the Negative Gate Bias Mode

K. Haraguchi, H. Kume, M. Ushiyama and M. Ohkura

Hitachi Ltd., Japan

A method for extracting the capacitance coupling coefficients of sub-0.5μm flash memory cells under the negative gate bias condition is proposed. This method can extract the coefficients from only the gate and drain electric characteristics. Since it is not affected by source profiles, it can be applied to short-channel flash memory cells. These results show that the coefficients can be varied in the programming mode.

12:00 am

Benchmark Methodology of Interconnect Capacitance Simulation Using Inter-digitated Capacitors

O. S. Nakagawa, S.-Y. Oh, T. Hsu and S. Habu*

Hewlett-Packard Laboratories, USA and Hachioji Semiconductor Test Division*, Hewlett-Packard, Japan

High-frequency capacitance measurement of inter-digitated metal-oxide-metal capacitors is used to benchmark interconnect capacitance simulation results. Total capacitance, layer-to-layer capacitance and line-to-line capacitance are measured from a single test structure for the benchmark. Metal width, metal height and dielectric thickness of the capacitors are locally characterized to generate an input file for simulations. The simulation results are then compared with the measured data.

12:20 am Best Paper Announcement and Closing Remarks

12:30 am End of Conference

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Open: March 23, 25 AM 9:00 - PM 5:00 and March 24 AM 9:00 - PM 6:00 and

March 26 AM 9:00 - AM 12:00 in front of the Citymonde Hall

Hakuto Corp. LTD.

Product Description:

Electromigration test system, TDDB test system AETRIUM

The Micromanipulator Co., Inc.

1-1-13 Shinjuku Shinjuku-ku Tokyo 160, Japan

Phone: +81-3-3225-8940 FAX: +81-3-3225-9009

Contact: Morihiko Imanaka

Vector Semiconductor Co., Ltd.

Product Description:

Probing System

1-9-3 Kita-kase Saiwai-ku Kawasaki Kanagawa 211, Japan

Phone: +81-44-587-8201 FAX: +81-44-587-8204

Contact: Akira Morii

Cascade Microtech Japan, Inc.

Product Description:

PS21 Parametric Series Auto Prober

Sumitomo Aobadai Hills Bldg. 7-7 Aobadai 4-chome Meguro-ku, Tokyo

153, Japan

Phone: +81-3-5478-6100 FAX: +81-3-5478-6105

Contact: Junko Nakaya

Hewlett-Packard Japan, Ltd.

Product Description:

HP 4156B Precision Semiconductor Parameter Analyzer

HP E5250A Low Leakage Switch Mainframe

9-1, Takakura-cho, Hachioji-shi, Tokyo 192, Japan

Phone: +81-426-60-8698 FAX: +81-426-60-8430

Contact: Narito Nakazawa

NTT Advanced Technology Corp.

Product Description:

BTABERT (Circuit Reliability Simulator) and BSIMPro (SPICE Model Parameter Extract)

Hakuei Bldg, 2-4-15 Naka-machi Musashino-shi Tokyo 180, Japan

Phone: +81-422-37-0805 FAX: +81-422-60-4810

Contact: Katsuhiko Daido