

1988 IEEE PROCEEDINGS ON MICROELECTRONIC TEST STRUCTURES

February 1988 Volume - 1 CH2560-01

Library of Congress No. 87-83668

1988 IEEE INTERNATIONAL CONFERENCE ON MICROELECTRONIC TEST STRUCTURES (ICMTS)

Long Beach Hyatt Regency, Long Beach, California

February 22 - 23, 1988

	PAGE
CHAIRMAN'S LETTER	1
1988 ICMTS CONFERENCE COMMITTEE	2
1988 ICMTS TECHNICAL PROGRAM COMMITTEE	3
PROGRAM SESSIONS AND CHAIRMEN	4
AUTHORS INDEX	5
1989 ANNOUNCEMENT	7

SESSION I

MATERIAL AND PROCESS CHARACTERIZATION	8
AN ELECTRICAL TEST STRUCTURE FOR MEASURING CONTACT SIZE ... G. Freeman and W. Lukaszek, Stanford University	9
EXPERIENCES IN EXTRACTION OF CONTACT PARAMETERS FROM PROCESS EVALUATION TEST-STRUCTURES ... U. Lieneweg, Jet Propulsion Laboratory	15
SOURCES OF ERROR IN EXTRACTING THE SPECIFIC CONTACT RESISTANCE FROM KELVIN DEVICE MEASUREMENTS ... W.J.C. Alexander and A.J. Walton, University of Edinburgh	17
COMB/SERPENTINE/CROSS-BRIDGE TEST STRUCTURE FOR FABRICATION PROCESS EVALUATION ... H.R. Sayah and M.G. Buehler, Jet Propulsion Laboratory	23

AN OBJECTIVE METHOD OF ASSESSING METAL PATTERNING QUALITY	
... <i>T. Stevenson, J. Gow and J. Serack, University of Edinburgh</i>	29
A MICROELECTRONIC TEST-STRUCTURE FOR THICKNESS DETERMINATION OF HOMOGENEOUS CONDUCTING THIN FILMS IN VLSI PROCESSING	
... <i>J.S. Kim, L.W. Linholm, and B.L. Barley, National Bureau of Standards, M.H. Hanes, and M.W. Cresswell, Westinghouse</i>	34
INTERCONNECT CAPACITANCE CHARACTERIZATION FOR MOS-IC PROCESS AND CIRCUIT DESIGN	
... <i>C. Kortekaas, Philips Research Laboratories</i>	39
A DIRECT METHOD FOR MEASURING THE GATE OXIDE CAPACITANCES OF MOSFETs	
... <i>R.A. Allen, C.A. Piña*, and Martin G. Buehler, Jet Propulsion Laboratory and *USC/ISI</i>	45

SESSION II

DEVICE AND CIRCUIT CHARACTERIZATION	49
IMPACT OF THE SELF HEATING EFFECT ON CIRCUIT PERFORMANCE ESTIMATION USING DC MODEL PARAMETERS	
... <i>D. Takacs, J. Trager, and D. Schmitt-Landsiedel, Siemens AG</i>	50
RING OSCILLATOR STRUCTURE FOR REALISTIC DYNAMIC STRESS OF MOSFETs AND INTERCONNECTS	
... <i>J. Winnerl, F. Neppel, A. Lill, G. Roska, and W. Zatsch, Siemens AG</i>	56
TOTAL DOSE RADIATION RESPONSE OF TEST STRUCTURES AND VLSI LOGIC DEVICES: AN ANALYTICAL AND EXPERIMENTAL CORRELATION	
... <i>D.M. Newberry and B. E. Peters, Control Data Corporation</i>	61
A NOVEL DEVICE STRUCTURE FOR STUDYING GATE AND CHANNEL EDGE EFFECTS OF IGFET's	
... <i>J.A. Serack, A.J. Walton, and J.M. Robertson, University of Edinburgh</i>	67
DETERMINATION OF PROCESS-DEPENDENT CRITICAL SPICE PARAMETERS FOR APPLICATION-SPECIFIC ICs	
... <i>B.J. Sheu, C-C. Shih, M-C. Hsu, C-P. Wan and W-J. Hsu, University of Southern California</i>	73
A FULLY ANALYTICAL MOSFET MODEL PARAMETER EXTRACTION APPROACH	
... <i>H.P. Tuinhout, S. Swaving, and J.J.M. Joosten, Philips Research Laboratories</i>	79

ΔL EXTRACTION USING PARASITIC BIPOLAR TRANSISTORS	
... <i>D. Wilson, A.J. Walton, J.M. Robertson, and R.J. Holwill, University of Edinburgh</i>	85
COMPARISON OF RESULTS FROM SIMPLE EXPRESSIONS FOR MOSFET PARAMETER EXTRACTION	
... <i>M.G. Buehler and Y-S. Lin, Jet Propulsion Laboratory</i>	90
DETERMINATION OF THE HF MODEL PARAMETERS OF THE MOS TRANSISTOR BY USING STANDARD DROPIN TEST STRUCTURES	
... <i>P. Vandeloo* and W. Sansen, *IMEC and Katholieke University</i>	97

SESSION III

YIELD AND RELIABILITY	102
DEFECT DIAGNOSTIC MATRIX – A DEFECT LEARNING VEHICLE FOR SUBMICRON TECHNOLOGIES	
... <i>E.J. Sprogis and R.E. Newhart, IBM</i>	103
STATISTICAL SIGNIFICANCE OF DEFECT DENSITY ESTIMATES	
... <i>U. Kaempt, Hewlett Packard Corporation</i>	107
STANDARD DEFECT MONITOR	
... <i>C. Weber, Hewlett Packard Corporation</i>	114
GUIDELINES FOR LATCH-UP CHARACTERIZATION TECHNIQUES	
... <i>W. Reczek, Siemens AG</i>	120
TEST CIRCUIT STRUCTURES FOR CHARACTERIZING THE EFFECTS OF LOCALIZED HOT-CARRIER-INDUCED CHARGE IN VLSI SWITCHING CIRCUITS	
... <i>J.S. Suehle and K.F. Galloway, National Bureau of Standards and University of Arizona</i>	126
THERMAL INTERACTIONS BETWEEN ELECTROMIGRATION TEST STRUCTURES	
... <i>H.A. Schafft and J. Albers, National Bureau of Standards</i>	132
TEMPERATURE CONTROL IN WAFER LEVEL TESTING OF LARGE MULTI- SEGMENT ELECTROMIGRATION TEST STRUCTURES	
... <i>N. Zamani and Y-S. Lin, Jet Propulsion Laboratory</i>	138

SPATIALLY NON-UNIFORM, TIME VARYING THERMAL CHARACTERIZATION OF VLSI CHIPS

... B.J. Cooke, J.L. Prince, Z.J. Staszak, D. Shope, and W.J. Fahey,
University of Arizona 143

SESSION IV

TEST STRUCTURES DATA ANALYSIS AND MANAGEMENT149

TEST VEHICLE FOR THE MEASUREMENT OF CHARGE COLLECTION
AND SOFT ERROR RATE PREDICTION IN HIGH-DENSITY MEMORIES
DUE TO α -PARTICLE STRIKES

... P. Oldiges, T. Furuyama, and J. Frey, Cornell University150

EVALUATING INTEGRATED CIRCUIT TECHNOLOGIES FOR SPACE
APPLICATION - THE GVSC TEST CHIP

... K. Wilson, T. Zietlow, T. Morse, T. Tsubota, J. Rollins, The Aerospace
Corporation and R. Herndon, Air Force Space Technology Center 154

A DEVELOPMENTAL EXPERT SYSTEM FOR TEST STRUCTURE
DATA EVALUATION

... L.W. Linholm, D. Khera, and C.P. Reeve, National Bureau
of Standards and M.W. Cresswell, Westinghouse160

CMOS PROCESS MONITOR

... M.G. Buehler, L.W. Linholm**, V.C. Tyree*, R.A. Allen, B.R. Blaes,
K.A. Hicks, and G.A. Jennings, Jet Propulsion Laboratory, University of
Southern California/ISI*, National Bureau of Standards**. 164

EXPERT SYSTEM FOR TEST STRUCTURE DATA INTERPRETATION

... F.N.H. Montijn-Dorgelo, and H.J. ter Horst, Philips Research Laboratories 169

INTERPRETATION OF CAPACITANCE VOLTAGE CURVES FOR
PROCESS FAULT DIAGNOSIS: A MACHINE LEARNING EXPERT
SYSTEMS APPROACH

... J.A. Walls, A.J. Walton, J.M. Robertson, and T.M. Crawford*, University
of Edinburgh and Hewlett Packard*174

POSTER SESSION	179
MOS-IC PROCESS AND DEVICE CHARACTERIZATION WITHIN PHILIPS	
... <i>S. Swaving, A. Ketting, and A. Trip, Philips Research Laboratories</i>	180
THE DESIGN AND CALIBRATION OF A SEMICONDUCTOR STRAIN GAUGE ARRAY	
... <i>V.R. Akylas, S.A. Gee, and W.F. van den Bogert, Philips Research Laboratories</i>	185
AUTOMATIC TEST STRUCTURE MODIFICATION	
... <i>K. Golshan, S.S.Mahant Shetti, and M. Harward, Texas Instruments</i>	192
MEASUREMENT OF STATIC NOISE IMMUNITY FOR STL AND ISL BIPOLAR LOGICS	
... <i>J.M. Chateau and M. Depey, Thomson Semiconducteurs</i>	195
METHOD FOR ACCURATE DETERMINATION OF THE INTRINSIC CUT-OFF FREQUENCY OF IC BIPOLAR TRANSISTORS	
... <i>D. Celi, Thomson Semiconducteurs</i>	200
A TEST STRUCTURE TO MEASURE THE MISALIGNMENT BETWEEN POLY-SI AND DIFFUSION LAYERS	
... <i>M. Jian, Tianjin University</i>	204